Trimmed Offset Voltage:

TLC277 . . . 500 μV Max at 25°C, $V_{DD} = 5 V$

- Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over **Specified Temperature Range:**

 0° C to 70° C . . . 3 V to 16 V -40°C to 85°C . . . 4 V to 16 V -55°C to 125°C . . . 4 V to 16 V

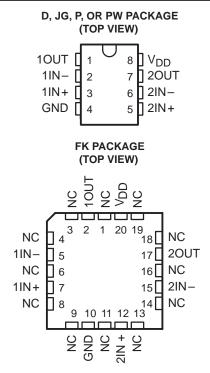
- Single-Supply Operation
- **Common-Mode Input Voltage Range** Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz
- **Output Voltage Range Includes Negative** Rail
- High Input impedance . . . $10^{12} \Omega$ Typ
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also** Available in Tape and Reel
- **Designed-in Latch-Up Immunity**

description

The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

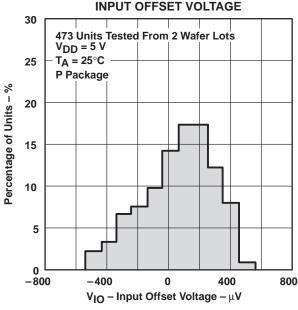
These devices use Texas instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these costeffective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the



NC - No internal connection

DISTRIBUTION OF TLC277



low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

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AVAILABLE OPTIONS

			PAC	KAGED DEVIC	CES		CHIP
TA	V _{IO} max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	FORM (Y)
0°C to 70°c	500 μV 2 mV 5 mV 10mV	TLC277CD TLC272BCD TLC272ACD TLC272CD	_ _ _ _	_ _ _ _	TLC277CP TLC272BCP TLC272ACP TLC272CP	 TLC272CPW	— — — TLC272Y
-40°C to 85°C	500 μV 2 mV 5 mV 10 mV	TLC277ID TLC272BID TLC272AID TLC272ID	1111	 - - -	TLC277IP TLC272BIP TLC272AIP TLC272IP	1111	 - -
-55°C to 125°C	500 μV 10 mV	TLC277MD TLC272MD	TLC277MFK TLC272MFK	TLC277MJG TLC272MJG	TLC277MP TLC272MP	_ _	_

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

description (continued)

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

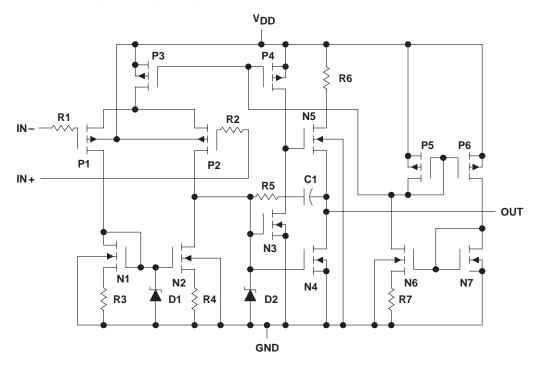
The device inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0° C to 70° C. The I-suffix devices are characterized for operation from -40° C to 85° C. The M-suffix devices are characterized for operation over the full military temperature range of -55° C to 125° C.

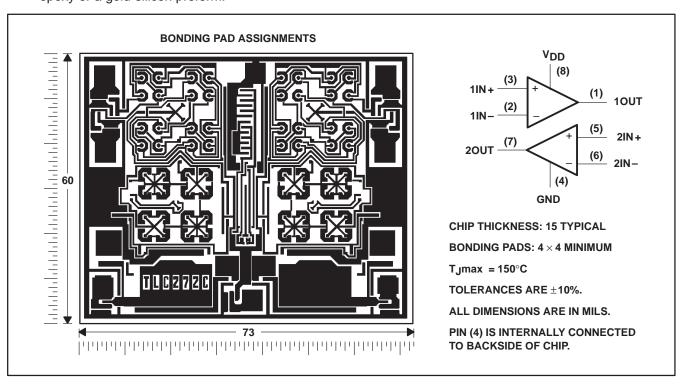


equivalent schematic (each amplifier)



TLC272Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC272C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{DD} (see Note 1)	18 V
Differential input voltage, V _{ID} (see Note 2)	±V _{DD}
Input voltage range, V _I (any input)	0.3 V to V _{DD}
Input current, I ₁	
output current, IO (each output)	±30 mA
Total current into V _{DD}	
Total current out of GND	45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature, T _A : C suffix	0°C to 70°C
I suffix	40°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW p	backage 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at IN+ with respect to IN-.
 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
PW	525 mW	4.2 mW/°C	336 mW	N/A	N/A

recommended operating conditions

		C SU	FFIX	I SUF	FIX	M SU	FFIX	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V _{DD}		3	16	4	16	4	16	V
Common mode input valtage V.	V _{DD} = 5 V	-0.2	3.5	-0.2	3.5	0	3.5	V
Common-mode input voltage, V _{IC}	V _{DD} = 10 V	-0.2	8.5	-0.2	8.5	0	8.5	V
Operating free-air temperature, TA		0	70	-40	85	-55	125	°C



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electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	T _A †	TLC272 TLC272			UNIT
						MIN	TYP	MAX	
		TLC272C	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		TLCZ/ZC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			12	mV
		TLC272AC	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.9	5	IIIV
\/.a	Input offset voltage	TLCZTZAC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			6.5	
VIO	Input offset voltage	TLC272BC	V _O = 1.4 V,	V _{IC} = 0,	25°C		230	2000	
		TLCZ/ZBC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			3000	\/
		TLC277C	V _O = 1.4 V,	V _{IC} = 0,	25°C		200	500	μV
		TLCZITC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			1500	
α_{VIO}	Temperature coefficient of input	offeet voltage			25°C to		1.8		μV/°C
ωVIO	- Temperature coemicient of input	onset voltage			70°C				μν/Ο
lio	Input offset current (see Note 4)		V _O = 2.5 V,	V _{IC} = 2.5 V	25°C		0.1		pА
.10	input one of current (coo rector)		VO = 2.0 V,	10-2.01	70°C		7	300	Ρ, ,
I _{IB}	Input bias current (see Note 4)		V _O = 2.5 V,	V _{IC} = 2.5 V	25°C		0.6		pА
'ID	input bias current (see Note 4)		V() = 2.0 V,	VIC - 2.0 V	70°C		40	600	P
						-0.2	-0.3		
	O				25°C	to 4	to 4.2		V
VICR	Common-mode input voltage rar (see Note 5)	nge				-0.2	4.2		
	(655):1515-57				Full range	to			V
						3.5			
					25°C	3.2	3.8		
∨он	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	0°C	3	3.8		V
					70°C	3	3.8		
					25°C		0	50	
V_{OL}	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C		0	50	mV
					70°C		0	50	
					25°C	5	23		
A _{VD}	Large-signal differential voltage a	amplification	$V_0 = 0.25 \text{ V to 2 V},$	$R_L = 10 \text{ k}\Omega$	0°C	4	27		V/mV
					70°C	4	20		
					25°C	65	80		
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		0°C	60	84		dB
					70°C	60	85		
					25°C	65	95		
ksvr	Supply-voltage rejection ratio		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	0°C	60	94		dB
	$(\Delta V_{DD}/\Delta V_{IO})$			-	70°C	60	96		
					25°C		1.4	3.2	
I _{DD}	Supply current (two amplifiers)		$V_0 = 2.5 \text{ V},$	$V_{IC} = 5 V$,	0°C		1.6	3.6	mA
			No load		70°C		1.2	2.6	
	' 000 1 7000								

[†]Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

Vo		PARAMETER		TEST CONDI	TIONS	T _A †	TLC272 TLC272			UNIT
$V_{VO} = V_{VO} = V$							MIN	TYP	MAX	
No			TI C272C			25°C		1.1	10	
No			1202720	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			12	m\/
Vio Input offset voltage Rg = 50 \(\) Vio = 1.4 \(\) Vio C = 0, \(\) Rg = 50 \(\) Vio C = 0, \(\) Rg = 50 \(\) Vio C = 0, \(\) Rg = 50 \(\) Vio C = 0, \(\) Rg = 50 \(\) Vio C = 0, \(\) Rg = 50 \(\) Vio C = 0, \(\) Rg = 50 \(\) Vio C = 0, \(\) Rg = 10 \(\) KD Full range 3000 25°C 250 800 2000 Full range 1900 25°C 25			TI C272AC	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.9	5	IIIV
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	\/\c	Input offset voltage	TLUZIZAU	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			6.5	
1100 - 100 -	VIO	input onset voitage	TI C272BC	V _O = 1.4 V,	V _{IC} = 0,	25°C		290	2000	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			TLCZ7ZBC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			3000	\/
RS = 50 LI, RL = 10 KD Full range 1900			TI C277C	V _O = 1.4 V,	V _{IC} = 0,	25°C		250	800	μν
Input offset current (see Note 4) V _O = 5 V, V _{IC} = 5 V 25°C 0.1 70°C 7 300 70°C 70°C 7 300			TLGZITG	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			1900	
Input offset current (see Note 4)	α_{VIO}	Temperature coefficient of input of	ffset voltage					2		μV/°C
IIB Input bias current (see Note 4) VO = 5 V, VIC = 5 V 25°C 0.7 70°C 50 600 PA	lio.	Input offset current (see Note 4)		V0 - 5 V	\/10 = 5 \/	25°C		0.1		nΛ
In	IIO	input onset current (see Note 4)		VO = 5 V	AIC = 2A	70°C		7	300	PΑ
$V_{ICR} = \begin{array}{c} & 70^{\circ}\text{C} & 50 & 600 \\ & & -0.2 & -0.3 \\ & & \text{to} & \text{to} & \text{to} \\ & & 9 & 9.2 \\ & & -0.2 \\ & & \text{Full range} & \text{to} \\ & & 8.5 \\ & & & $	1	Input bigg gurrent (age Note 4)		V- 5.V	\/ F\/	25°C		0.7		π Λ
VICR Common-mode input voltage range (see Note 5) V	IIВ	input bias current (see Note 4)		VO = 2V	AIC = 2 A	70°C		50	600	рА
VICR Common-mode input voltage range (see Note 5)							-0.2	-0.3		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C				V
$V_{OH} \text{High-level output voltage} V_{ID} = 100 \text{mV}, R_L = 10 \text{k}\Omega \frac{25^\circ \text{C}}{70^\circ \text{C}} \frac{8}{7.8} \frac{8.5}{8.5} V$ $V_{OL} \text{Low-level output voltage} V_{ID} = -100 \text{mV}, I_{OL} = 0 \frac{25^\circ \text{C}}{70^\circ \text{C}} \frac{8}{7.8} \frac{8.5}{8.5} V$ $V_{OL} \text{Low-level output voltage} V_{ID} = -100 \text{mV}, I_{OL} = 0 \frac{25^\circ \text{C}}{70^\circ \text{C}} \frac{0}{50} \frac{50}{50} \text{mV}$ $V_{O} = 1 \text{V to 6 V}, R_L = 10 \text{k}\Omega \frac{0^\circ \text{C}}{70^\circ \text{C}} \frac{36}{10} \frac{10}{36} V_{ID} = \frac{100 \text{mV}}{100^\circ \text{C}} \frac{10}{70^\circ \text{C}} \frac{36}{100^\circ \text{C}} \frac{10}{100^\circ \text{C}} \frac{36}{100^\circ \text{C}} \frac{10}{100^\circ \text{C}} \frac{36}{100^\circ \text{C}} \frac{10}{100^\circ \text{C}} \frac{36}{100^\circ \text{C}} \frac{10}{100^\circ \text{C}} \frac{10}{$	VICR		ge					9.2		
$V_{OH} \text{High-level output voltage} \qquad V_{ID} = 100 \text{mV}, R_{L} = 10 \text{k}\Omega \qquad \frac{25^{\circ}\text{C}}{70^{\circ}\text{C}} \qquad \frac{8.8.5}{7.8} \qquad V$ $V_{OL} \text{Low-level output voltage} \qquad V_{ID} = -100 \text{mV}, I_{OL} = 0 \qquad \frac{25^{\circ}\text{C}}{70^{\circ}\text{C}} \qquad 0 \qquad 50}{70^{\circ}\text{C}} \qquad 0 \qquad 50} \text{mV}$ $A_{VD} \text{Large-signal differential voltage amplification} \qquad V_{O} = 1 \text{V to 6 V}, R_{L} = 10 \text{k}\Omega \qquad \frac{25^{\circ}\text{C}}{70^{\circ}\text{C}} \qquad 0 \qquad 50}{70^{\circ}\text{C}} \qquad 0 \qquad 50} \text{mV}$ $CMRR \text{Common-mode rejection ratio} \qquad V_{IC} = V_{ICR} \text{min} \qquad \frac{25^{\circ}\text{C}}{70^{\circ}\text{C}} \qquad 60 \qquad 88}{70^{\circ}\text{C}} \qquad 60 \qquad 88} \qquad \text{dB}$ $K_{SVR} \frac{\text{Supply-voltage rejection ratio}}{(\Delta V_{DD}/\Delta V_{IO})} \qquad V_{DD} = 5 \text{V to 10 V}, V_{O} = 1.4 \text{V}$ $V_{DD} = 5 \text{V to 10 V}, V_{O} = 1.4 \text{V}$ $V_{O} = 2.5 \text{V}, V_{IC} = 5 \text{V}, V_{IC} = 5 \text{V}, O_{\circ}^{\circ}\text{C} \qquad 2.3 \qquad 4.4 \text{mA}$		(see Note 5)				Full range	ı			V
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$						i un range				ľ
$V_{OL} \text{Low-level output voltage} \qquad V_{ID} = -100 \text{mV}, I_{OL} = 0 \qquad \begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C	8	8.5		
$V_{OL} \text{Low-level output voltage} \qquad V_{ID} = -100 \text{mV}, I_{OL} = 0 \qquad \begin{array}{c} 70^{\circ}\text{C} & 7.8 & 8.4 \\ 25^{\circ}\text{C} & 0 & 50 \\ 70^{\circ}\text{C} & 0 & 50 \\ \hline 70^{\circ}\text{C} & 10 & 36 \\ \hline 70^{\circ}\text{C} & 7.5 & 42 \\ \hline 70^{\circ}\text{C} & 7.5 & 32 \\ \hline \text{CMRR} \text{Common-mode rejection ratio} \qquad V_{IC} = V_{ICR} \text{min} \qquad \begin{array}{c} 25^{\circ}\text{C} & 65 & 85 \\ \hline 70^{\circ}\text{C} & 60 & 88 \\ \hline 70^{\circ}\text{C} & 60 & 88 \\ \hline 70^{\circ}\text{C} & 60 & 88 \\ \hline 70^{\circ}\text{C} & 60 & 94 \\ \hline 70^{\circ}\text{C} & 60 & 96 \\ \hline \end{array} \text{dB}$ $V_{DD} = 5 \text{V to 10 V}, V_{O} = 1.4 \text{V} \qquad \begin{array}{c} 25^{\circ}\text{C} & 65 & 95 \\ \hline 70^{\circ}\text{C} & 60 & 94 \\ \hline 70^{\circ}\text{C} & 60 & 96 \\ \hline \end{array} \text{dB}$ $V_{DD} = 5 \text{V to 10 V}, V_{D} = 1.4 \text{V} \qquad \begin{array}{c} 25^{\circ}\text{C} & 60 & 94 \\ \hline 70^{\circ}\text{C} & 60 & 96 \\ \hline \end{array} \text{dB}$ $V_{DD} = 5 \text{V to 10 V}, V_{D} = 1.4 \text{V} \qquad \begin{array}{c} 25^{\circ}\text{C} & 1.9 & 4 \\ \hline 70^{\circ}\text{C} & 60 & 96 \\ \hline \end{array} \text{dB}$ $V_{DD} = 5 \text{V to 10 V}, V_{D} = 5 \text{V} \text{No load} \qquad V_{DC} = 5 \text{V}, V_{D} = 2.5 $	Vон	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \text{ k}\Omega$	0°C	7.8	8.5		V
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$						70°C	7.8	8.4		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C		0	50	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C		0	50	mV
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						70°C		0	50	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C	10	36		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	AVD	Large-signal differential voltage a	mplification	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	0°C	7.5	42		V/mV
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						70°C	7.5	32		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C	65	85		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min			60	88		dB
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						70°C	60	88		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$							_			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	ksvr			$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	0°C	60	94		dB
$V_{O} = 2.5 \text{ V},$ $V_{IC} = 5 \text{ V},$ $V_{$		(ΦΛΟΟ/ΦΛΙΟ)			-	70°C	60	96		
$V_O = 2.5 \text{ V},$ $V_{IC} = 5 \text{ V},$ 0°C 2.3 4.4 mA						25°C		1.9	4	
No load	I _{DD}	Supply current (two amplifiers)			$V_{IC} = 5 V$,			-	4.4	mA
		, ,		INU IUAU		70°C		1.6	3.4	

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	ΤΑ [†]		2I, TLC2 2BI, TLC		UNIT
						MIN	TYP	MAX	
		TLC272I	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		TLOZIZI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			13	mV
		TLC272AI	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.9	5	IIIV
\/.a	Input offset voltage	TLOZIZAI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			7	
VIO	input onset voltage	TLC272BI	V _O = 1.4 V,	$V_{IC} = 0$,	25°C		230	2000	
		TLOZIZBI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			3500	μV
		TLC277I	V _O = 1.4 V,	V _{IC} = 0,	25°C		200	500	μν
		TLOZITI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			2000	
α_{VIO}	Temperature coefficient of input of	offset voltage			25°C to 85°C		1.8		μV/°C
l.o	Input offset ourrent (see Note 4)		Va - 2 5 V	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	25°C		0.1		n /
lιο	Input offset current (see Note 4)		V _O = 2.5 V,	$V_{IC} = 2.5 V$	85°C		24	15	pΑ
	land bin a summer (and Nata A)		V 05V	V 0.5.V	25°C		0.6		А
lΒ	Input bias current (see Note 4)		$V_0 = 2.5 V$,	$V_{IC} = 2.5 V$	85°C		200	35	pΑ
						-0.2	-0.3		
					25°C	to	to		V
VICR	Common-mode input voltage ran	ge				4	4.2		
	(see Note 5)				Full range	-0.2 to			V
					i uli range	3.5			V
					25°C	3.2	3.8		
VOH	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \text{ k}\Omega$	-40°C	3	3.8		V
			.5	_	85°C	3	3.8		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C		0	50	mV
			-		85°C		0	50	
					25°C	5	23		
AVD	Large-signal differential voltage a	amplification	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	-40°C	3.5	32		V/mV
					85°C	3.5	19		
					25°C	65	80		
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		-40°C	60	81		dB
					85°C	60	86		
					25°C	65	95		
kSVR	Supply-voltage rejection ratio		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	-40°C	60	92		dB
	$(\Delta V_{DD}/\Delta V_{IO})$				85°C	60	96		
				.,,	25°C		1.4	3.2	
I _{DD}	Supply current (two amplifiers)		$V_O = 5 V$, $V_{IC} =$ No load	$V_{IC} = 5 V$,	-40°C		1.9	4.4	mA
					85°C		1.1	2.4	

[†] Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

No		PARAMETER		TEST CONDI	TIONS	T _A †		2I, TLC2 2BI, TL0		UNIT
No. 1 No.							MIN	TYP	MAX	
No N			TI C2721	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
No N			TLOZIZI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			13	m\/
No			TI C272A1	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.9	5	IIIV
TLC272Bl Rs = 50 Ω Rl = 10 kΩ Full range Secondary Full range Secondary Rl = 10 kΩ Full r	\/\c	Input offeet voltage	TLOZIZAI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			7	
No continue	VIO	input onset voltage	TI COZORI	V _O = 1.4 V,	V _{IC} = 0,	25°C		290	2000	
TLC2771 NG = 1.4 V, RS = 50 Ω, RL = 10 kΩ Full range RS = 50 Ω, RL = 10 kΩ Full range RS = 50 Ω, RL = 10 kΩ Full range RS = 50 Ω, RL = 10 kΩ Full range RS = 50 Ω, RL = 10 kΩ Full range RS = 50 Ω, RL = 10 kΩ Full range RS = 50 Ω, RL = 10 kΩ RS = 50 Ω, RL = 10 kΩ Full range RS = 50 Ω, RL = 10 kΩ RS = 50 Ω			TLOZIZBI		$R_L = 10 \text{ k}\Omega$	Full range			3500	\/
NS = 50 11, RL = 10 kΩ Full range 2900 NS = 50 11, RL = 10 kΩ Full range 25°C to 25°C			TI C2771	V _O = 1.4 V,	V _{IC} = 0,	25°C		250	800	μν
No Imput offset current (see Note 4) VO = 5 V. VIC = 5 V VIC = 5 V 25°C 0.1			TLOZITI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			2900	
Input offset current (see Note 4)	α_{VIO}	Temperature coefficient of input of	offset voltage					2		μV/°C
No	li o	Input offset ourrent (see Note 4)		Va - 5 V	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	25°C		0.1		- Λ
No	IIO	input onset current (see Note 4)		VO = 2V	AIC = 2 A	85°C		26	1000	рA
V _{ICR} Common-mode input voltage range (see Note 5) V _{ID} = 100 mV, R _L = 10 kΩ 25°C 10 36 10 10 10 10 10 10 10 1	1	January biogramment (see Note 4)		V- 5V	V:- 5.V	25°C		0.7		A
$ V_{ICR} = \begin{array}{c} Common-mode input voltage range \\ (see Note 5) \\ \hline \\ V_{OH} = 0 \\ V_{ID} = 0 \\$	ΙΊΒ	input bias current (see Note 4)		VO = 2 V	AIC = 2 A	85°C		220	2000	рA
Vocation							-0.2	-0.3		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C				V
Voh High-level output voltage ViD = 100 mV, RL = 10 kΩ 25°C 8 8.5 ViD = 100 mV, RL = 10 kΩ 25°C 8 8.5 ViD = 100 mV, RL = 10 kΩ 25°C 7.8 8.5 ViD = 100 mV, RL = 10 kΩ 25°C 7.8 8.5 ViD = 100 mV, RL = 10 kΩ 25°C 0 50 50 7.8 8.5 ViD = 100 mV, RL = 10 kΩ 25°C 0 50 50 7.8 8.5 ViD = 100 mV, RL = 10 kΩ 25°C 10 36 ViD = 100 mV, RL = 10 kΩ 25°C 10 36 ViD = 100 mV, RL = 10 kΩ 25°C 10 36 ViD = 100 mV, RL = 10 kΩ 25°C 10 36 ViD = 100 mV, RL = 10 kΩ 25°C 10 36 ViD = 100 mV, ViD = 100 mV, RL = 10 kΩ 25°C 10 36 ViD = 100 mV, ViD = 100 mV	VICR		ge					9.2		
No		(see Note 5)				Full range				\/
$\begin{array}{c} V_{OH} \\ V_{OL} \\ V_{OL$						i uli range				v
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C	8	8.5		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	VOH	High-level output voltage		V _{ID} = 100 mV,	$R_I = 10 \text{ k}\Omega$	-40°C	7.8	8.5		V
$ \begin{array}{c} V_{OL} \mbox{Low-level output voltage} \\ V_{ID} = -100 \ mV, I_{OL} = 0 \\ \hline \\ 85^{\circ}C \\ \hline \\ 0 50 \\ \hline \\ 85^{\circ}C \\ \hline \\ 0 50 \\ \hline \\ mV \\ \hline \\ 85^{\circ}C \\ \hline \\ 10 36 \\ \hline \\ -40^{\circ}C \\ \hline \\ 7 46 \\ \hline \\ 7 31 \\ \hline \\ 25^{\circ}C \\ \hline \\ 65 85 \\ \hline \\ 7 31 \\ \hline \\ 25^{\circ}C \\ \hline \\ 65 85 \\ \hline \\ 60 87 \\ \hline \\ 85^{\circ}C \\ \hline \\ 60 87 \\ \hline \\ 85^{\circ}C \\ \hline \\ 60 88 \\ \hline \\ 85^{\circ}C \\ \hline \\ 60 88 \\ \hline \\ 60 92 \\ \hline \\ 1_{DD} \\ \\ 1_{DD} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ $	"				_	85°C	7.8	8.5		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C		0	50	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	-40°C		0	50	mV
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						85°C		0	50	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C	10	36		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	AVD	Large-signal differential voltage a	amplification	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	-40°C	7	46		V/mV
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						85°C	7	31		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						25°C	65	85		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		-40°C	60	87		dB
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						85°C	60	88		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$										
	ksvr			$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	-40°C	60	92		dB
$V_O = 5 \text{ V},$ $V_{IC} = 5 \text{ V},$ $V_{IC} = 5 \text{ V},$ No load $V_{IC} = 5 \text{ V},$		(ΦΛΟΟ/ΦΛΙΟ)			-	85°C	60	96		
IDD Supply current (two amplifiers) No load No load						25°C		1.4	4	
110 1040	I _{DD}	Supply current (two amplifiers)			$V_{IC} = 5 V$,	-40°C		2.8	5	mA
				I NO IOAU		85°C		1.5	3.2	

[†]Full range is -40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	DADAMETED		TEOT 0011D	ITIONIO	- +	TLC27	2M, TLC	277M	
	PARAMETER		TEST COND	ITIONS	T _A †	MIN	TYP	MAX	UNIT
		TLC272M	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	mV
1//0	Input offset voltage	TLC272IVI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			12	IIIV
VIO	input onset voltage	TLC277M	V _O = 1.4 V,	V _{IC} = 0,	25°C		200	500	μV
		TLOZITIVI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			3750	μν
αVIO	Temperature coefficient of input cooltage	ffset			25°C to 125°C		2.1		μV/°C
l.o	Input offset current (see Note 4)		V _O = 2.5 V	V _{IC} = 2.5 V	25°C		0.1		pА
lio	input offset current (see Note 4)		V() = 2.5 V	VIC = 2.5 V	125°C		1.4	15	nA
lin	Input bias current (see Note 4)		V _O = 2.5 V	V _{IC} = 2.5 V	25°C		0.6		pА
IB	input bias current (see Note 4)		V() = 2.5 V	vIC = 2.5 v	125°C		9	35	nA
	Common-mode input voltage ran	ae			25°C	0 to 4	-0.3 to 4.2		V
VICR	(see Note 5)	9-			Full range	0 to 3.5			V
					25°C	3.2	3.8		
VOH	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	−55°C	3	3.8		V
					125°C	3	3.8		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C		0	50	mV
					125°C		0	50	
					25°C	5	23		
A _{VD}	Large-signal differential voltage a	mplification	$V_0 = 0.25 \text{ V to 2 V}$	$R_L = 10 \text{ k}\Omega$	−55°C	3.5	35		V/mV
					125°C	3.5	16		
					25°C	65	80		
CMRR	Common-mode rejection ratio		VIC = VICRmin		−55°C	60	81		dB
					125°C	60	84		
	Supply voltage rejection ratio				25°C	65	95		
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 V$	−55°C	60	90		dB
					125°C	60	97		
			Vo = 25 V	V10 = 25 V	25°C		1.4	3.2	
IDD	Supply current (two amplifiers)	arei	$V_O = 2.5 \text{ V},$ $V_{IC} = 1.5 \text{ V}$	$V_{IC} = 2.5 V,$	−55°C		2	5	mA
					125°C		1	2.2	

[†] Full range is –55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	DARAMETER		TEOT 00110	ITIONS	- +	TLC27	2M, TLC	277M	
	PARAMETER		TEST COND	ITIONS	T _A †	MIN	TYP	MAX	UNIT
		TLC272M	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	ma\/
VIO	Input offset voltage	TLC272IVI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			12	mV
VIO	input onset voltage	TLC277M	V _O = 1.4 V,	$V_{IC} = 0$,	25°C		250	800	μV
		TLOZITIVI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			4300	μν
αΝΙΟ	Temperature coefficient of input voltage	offset			25°C to 125°C		2.2		μV/°C
li o	Input offeet ourrent (con Note 4)		V _O = 5 V,	V _{IC} = 5 V	25°C		0.1		pA
ΙΙΟ	Input offset current (see Note 4)		νO = 5 ν,	AIC = 2 A	125°C		1.8	15	nA
lin.	Input bias current (see Note 4)		V _O = 5 V,	V _{IC} = 5 V	25°C		0.7		pА
IВ	input bias current (see Note 4)		ν _O = 3 ν,	AIC = 2 A	125°C		10	35	nA
	Common-mode input voltage ra	nge			25°C	0 to 9	-0.3 to 9.2		٧
VICR	(see Note 5)				Full range	0 to 8.5			V
					25°C	8	8.5		
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	−55°C	7.8	8.5		V
					125°C	7.8	8.4		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	IOT = 0	−55°C		0	50	mV
					125°C		0	50	
	Lorgo cianal differential valtega				25°C	10	36		
A_{VD}	Large-signal differential voltage amplification		$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	−55°C	7	50		V/mV
					125°C	7	27		
					25°C	65	85		
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		−55°C	60	87		dB
					125°C	60	86		
	Cupply valtage rejection				25°C	65	95		
ksvr	Supply-voltage rejection ratio (ΔVDD/ΔVIO)		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	−55°C	60	90		dB
					125°C	60	97		
			V _O = 5 V,	V _{IC} = 5 V,	25°C		1.9	4	
I_{DD}	Supply current (two amplifiers)		VO = 5 V, No load	ν IC = ο ν,	−55°C		3	6	mA
					125°C		1.3	2.8	

[†] Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

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electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

	DADAMETED	TEST CONF	DITIONS	Т	LC272Y		LINUT
	PARAMETER	TEST CONE	OHIONS	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	$V_{O} = 1.4 \text{ V},$ $R_{S} = 50 \Omega,$	$V_{IC} = 0,$ $R_L = 10 \text{ k}\Omega$		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage				1.8		μV/°C
lio	Input offset current (see Note 4)	V _O = 2.5 V,	V _{IC} = 2.5 V		0.1		pА
I _{IB}	Input bias current (see Note 4)	V _O = 2.5 V,	V _{IC} = 2.5 V		0.6		pА
VICR	Common-mode input voltage range (see Note 5)			-0.2 to 4	-0.3 to 4.2		V
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$	R _L = 10 kΩ	3.2	3.8		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	I _{OL} = 0		0	50	mV
AVD	Large-signal differential voltage amplification	$V_0 = 0.25 \text{ V to 2 V}$	$R_L = 10 \text{ k}\Omega$	5	23		V/mV
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min		65	80		dB
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	65	95		dB
I _{DD}	Supply current (two amplifiers)	V _O = 2.5 V, No load	V _{IC} = 2.5 V,		1.4	3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

	DADAMETED	TEST CONI	OITIONS	Т	LC272Y		UNIT
	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	UNII
VIO	Input offset voltage	$V_{O} = 1.4 \text{ V},$ $R_{S} = 50 \Omega,$	$V_{IC} = 0,$ $R_L = 10 \text{ k}\Omega$		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage				1.8		μV/°C
IIO	Input offset current (see Note 4)	V _O = 5 V,	V _{IC} = 5 V		0.1		pА
I _{IB}	Input bias current (see Note 4)	V _O = 5 V,	V _{IC} = 5 V		0.7		pА
VICR	Common-mode input voltage range (see Note 5)			-0.2 to 9	-0.3 to 9.2		V
Vон	High-level output voltage	V _{ID} = 100 mV,	R _L = 10 kΩ	8	8.5		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	IOL = 0		0	50	mV
AVD	Large-signal differential voltage amplification	$V_0 = 1 \ V \ to \ 6 \ V,$	$R_L = 10 \text{ k}\Omega$	10	36		V/mV
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min		65	85		dB
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	65	95		dB
I _{DD}	Supply current (two amplifiers)	V _O = 5 V, No load	V _{IC} = 5 V,		1.9	4	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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operating characteristics at specified free-air temperature, $V_{DD} = 5 V$

	PARAMETER		NDITIONS	TA	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT				
				,	MIN	TYP	MAX					
				25°C		3.6						
			V _{IPP} = 1 V	0°C		4						
SR	Slew rate at unity gain	$R_L = 10 \text{ k}\Omega$	[70°C		3		\//uo				
	Siew rate at unity gain	C _L = 20 pF, See Figure 1			25°C		2.9		V/μs			
		occ rigure r		0°C		3.1						
					70°C		2.5					
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz				
			_	25°C		320						
Вом	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,	C _L = 20 pF, See Figure 1	0°C		340		kHz				
		$R_{\perp} = 10 \text{ Ksz},$		70°C		260						
				25°C		1.7						
B ₁	Unity-gain bandwidth	nity-gain bandwidth $V_{I} = 10 \text{ mV}, C_{L} = 20 \text{ pF},$ See Figure 3	0°C		2		MHz					
		See rigure 3		70°C		1.3						
		V 40V	(5	25°C		46°						
φm	Phase margin	$V_{\parallel} = 10 \text{ mV},$	$V_I = 10 \text{ mV},$ $C_L = 20 \text{ pF},$	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF}$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	f = B ₁ , See Figure 3	0°C	47°		
			cooguro o	70°C		43°						

operating characteristics at specified free-air temperature, $V_{DD} = 10 \text{ V}$

	PARAMETER	TEST CO	TEST CONDITIONS		TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT				
				TA	MIN	TYP	MAX					
				25°C		5.3						
			V _{IPP} = 1 V	0°C		5.9						
SR	Slew rate at unity gain	$R_L = 10 kΩ,$ $C_L = 20 pF,$		70°C		4.3		V/μs				
	Siew rate at unity gain	See Figure 1		25°C		4.6		ν/μδ				
		V _{IPP} = 5.5 V	0°C		5.1		1 1					
					70°C		3.8					
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz				
			_	25°C		200						
Вом	Maximum output-swing bandwidth	V _O = V _{OH} ,	C _L = 20 pF, See Figure 1	0°C		220		kHz				
			See rigure r	70°C		140						
				25°C		2.2						
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	0°C		2.5		MHz				
		Gee rigure 3		70°C		1.8						
)/ 40 m)/	, ,	25°C		49°						
φm	Phase margin	$V_{I} = 10 \text{ mV},$	$V_{I} = 10 \text{ mV},$	$V_{\parallel} = 10 \text{ mV},$ $C_{\perp} = 20 \text{ pF},$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ nF}$	$V_{ } = 10 \text{ mV},$	f = B ₁ , See Figure 3	0°C	50°		
		OL - 20 pr,	CCC 1 Iguro 0	70°C		46°						

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operating characteristics at specified free-air temperature, $V_{DD} = 5 V$

	PARAMETER		TEST CONDITIONS		TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT		
				T _A	MIN	TYP	MAX			
				25°C		3.6				
			V _{IPP} = 1 V	-40°C		4.5				
SR	Slow rate at unity gain	$R_L = 10 \text{ k}\Omega$, $C_L = 20 \text{ pF}$,		85°C		2.8		\//uo		
SK	Slew rate at unity gain	See Figure 1		25°C		2.9		V/μs		
				V _{IPP} = 2.5 V	-40°C		3.5			
				85°C		2.3				
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz		
				25°C		320				
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_I = 10 \text{ k}\Omega$,	C _L = 20 pF,	−40°C		380		kHz		
			See rigure r	85°C		250				
				25°C		1.7				
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	-40°C		2.6		MHz		
		See rigure 3		85°C		1.2				
)/ ₁ 40 m)/	4 D	25°C		46°				
φm	Phase margin	$V_1 = 10 \text{ mV},$	$V_1 = 10 \text{ mV},$	$V_I = 10 \text{ mV},$ $C_L = 20 \text{ pF},$	f = B ₁ , See Figure 3	-40°C		49°		
		OL = 20 β1,	occ i igule o	85°C		43°				

operating characteristics at specified free-air temperature, $V_{DD} = 10 \text{ V}$

PARAMETER		TEST CO	NDITIONS	TA	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT				
					MIN	TYP	MAX					
				25°C		5.3						
	$V_{IPP} = 1 V$ $-40^{\circ}C$	6.8										
SR	Slow rate of unity gain	$R_L = 10 \text{ k}\Omega$, $C_L = 20 \text{ pF}$,		85°C		4		\//uo				
SK	Slew rate at unity gain	See Figure 1		25°C		4.6		V/μs				
			V _{IPP} = 5.5 V	-40°C		5.8						
				85°C		3.5						
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz				
				25°C		200						
ВОМ	Maximum output-swing bandwidth	Maximum output-swing bandwidth $V_O = V_{OH}$, $C_L = R_L = 10 \text{ k}\Omega$, See	$C_L = 20 \text{ pF},$	-40°C		260		kHz				
		$ \mathcal{R} = 10 \text{ Ksz},$	See Figure 1	85°C		130						
				25°C		2.2						
B ₁	Unity-gain bandwidth		$V_I = 10 \text{ mV}, \qquad C_L = 20 \text{ pF},$ See Figure 3			3.1		MHz				
		See rigure 3				1.7						
		V 40 V	. 5	25°C		49°						
φm	Phase margin		$V_1 = 10 \text{ mV},$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	$V_{\parallel} = 10 \text{ mV},$	$V_1 = 10 \text{ mV},$	f = B ₁ , See Figure 3	-40°C		52°		
	- -		See Figure 3	85°C		46°						

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operating characteristics at specified free-air temperature, $V_{DD} = 5 V$

	DADAMETED	TEST CO	NDITIONS	т.	TLC272M, TLC277M			LINIT		
	PARAMETER	TEST CO	NDITIONS	TA	MIN	TYP	MAX	UNIT		
				25°C		3.6				
			V _{IPP} = 1 V	−55°C		4.7				
SR	Slow rate at unity gain	$R_L = 10 \text{ k}\Omega$, $C_L = 20 \text{ pF}$,		125°C		2.3		\//u0		
SK	Slew rate at unity gain	See Figure 1		25°C		2.9		V/μs		
			V _{IPP} = 2.5 V	−55°C		3.7				
				125°C		2				
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz		
				25°C		320				
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,	$C_L = 20 \text{ pF},$	−55°C		400		kHz		
			See rigure r	125°C		230				
				25°C		1.7				
B ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	−55°C		2.9		MHz		
		Gee rigure 3		125°C		1.1				
)/ 40 m)/	, ,	25°C		46°				
φm	Phase margin	$V_{I} = 10 \text{ mV},$	$V_{\parallel} = 10 \text{ mV},$ $C_{\parallel} = 20 \text{ pF},$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	T = B ₁ , See Figure 3	−55°C		49°	
		oL _0 pi,	eeegaro o	125°C		41°	·			

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	DADAMETED	TEST CO.	TEST CONDITIONS		TLC272M, TLC277M			LINUT					
	PARAMETER	TEST CO	NDITIONS	TA	MIN	TYP	MAX	UNIT					
				25°C		5.3							
		4010	V _{IPP} = 1 V	−55°C		7.1							
SR	Slew rate at unity gain	$R_L = 10 \text{ k}\Omega$, $C_L = 20 \text{ pF}$,		125°C		3.1		V/μs					
SK	Siew rate at unity gain	See Figure 1		25°C		4.6		ν/μδ					
		V _{IPP} = 5.5 V	−55°C		6.1								
					125°C		2.7						
V _n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz					
		., .,		25°C		200							
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$	C _L = 20 pF, See Figure 1	−55°C		280	kHz						
		10 10 132,	occ rigure r	125°C		110							
				25°C		2.2							
В ₁	Unity-gain bandwidth $V_{\parallel} = 10 \text{ mV},$ See Figure 3	$C_L = 20 pF$,	−55°C		3.4		MHz						
		Jee Figure 3	See Figure 3	Jee Figure 3	Joee rigule 3		125°C		1.6				
			, D	25°C		49°							
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	$V_1 = 10 \text{ mV},$ $C_1 = 20 \text{ pF}$	r = B ₁ , See Figure 3	−55°C		52°		
			300 r igure 3	125°C		44°							

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operating characteristics, V_{DD} = 5 V, T_A = 25°C

	PARAMETER		TEST CONDITIONS			TLC272Y		
	PARAWETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$R_L = 10 \text{ k}\Omega$,	C _L = 20 pF,	V _{IPP} = 1 V		3.6		V/us
SK .	Siew rate at unity gain	See Figure 1		V _{IPP} = 2.5 V		2.9		ν/μδ
Vn	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$,	See Figure 2		25		nV/√ Hz
ВОМ	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	$C_L = 20 pF,$	$R_L = 10 \text{ k}\Omega$,		320		kHz
B ₁	Unity-gain bandwidth	$V_{I} = 10 \text{ mV},$	$C_L = 20 pF$,	See Figure 3		1.7		MHz
φm	Phase margin	V _I = 10 mV, See Figure 3	$f = B_1$,	C _L = 20 pF,		46°	·	

operating characteristics, V_{DD} = 10 V, T_A = 25°C

	PARAMETER	_	TEST CONDITIONS			TLC272Y		
	FARAIVIETER	'	EST CONDITION	NO	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$R_L = 10 \text{ k}\Omega$,	$C_L = 20 pF$,	V _{IPP} = 1 V		5.3		V/μs
Jok	Siew rate at unity gain	See Figure 1		V _{IPP} = 5.5 V		4.6		ν/μδ
Vn	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$,	See Figure 2		25		nV/√ Hz
ВОМ	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	$C_L = 20 pF$,	$R_L = 10 \text{ k}\Omega$,		200		kHz
B ₁	Unity-gain bandwidth	V _I = 10 mV,	C _L = 20 pF,	See Figure 3		2.2		MHz
φm	Phase margin	V _I = 10 mV, See Figure 3	f = B ₁ ,	C _L = 20 pF,		49°		

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

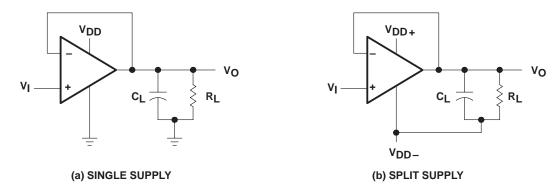


Figure 1. Unity-Gain Amplifier

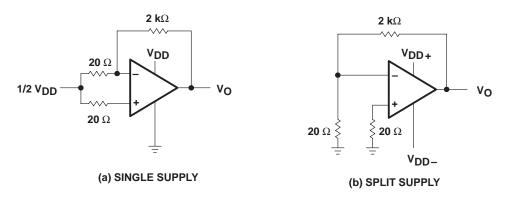


Figure 2. Noise-Test Circuit

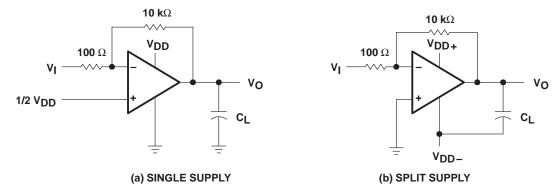


Figure 3. Gain-of-100 Inverting Amplifier



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PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC272 and TLC277 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- 1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

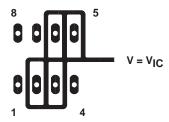


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

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PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
VIO	Input offset voltage	Distribution	6, 7
ανιο	Temperature coefficient of input offset voltage	Distribution	8, 9
Vон	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
VOL	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
AVD	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I _{IB}	Input bias current	vs Free-air temperature	22
IIO	Input offset current	vs Free-air temperature	22
VIC	Common-mode input voltage	vs Supply voltage	23
IDD	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
V _{O(PP)}	Maximum peak-to-peak output voltage	vs Frequency	29
B ₁	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
φm	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
٧ _n	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS

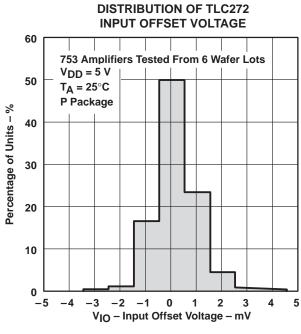


Figure 6

DISTRIBUTION OF TLC272 AND TLC277 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

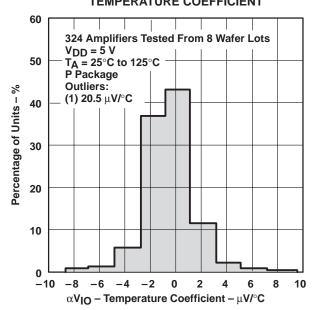


Figure 8

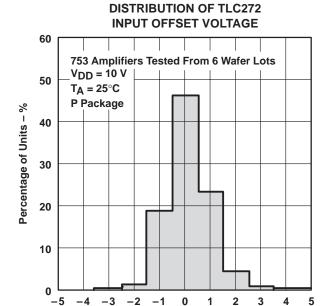


Figure 7

V_{IO} - Input Offset Voltage - mV

DISTRIBUTION OF TLC272 AND TLC277 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

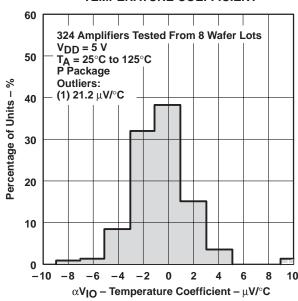
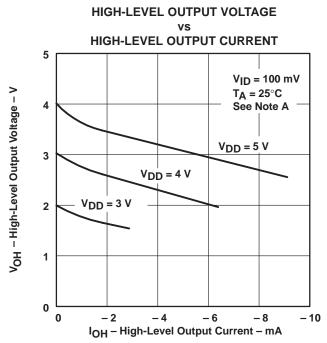


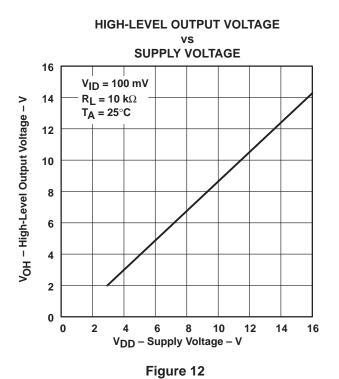
Figure 9

TYPICAL CHARACTERISTICS†



NOTE A: The 3-V curve only applies to the C version.

Figure 10



HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

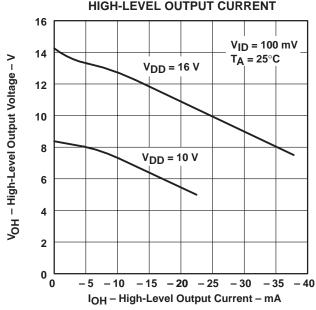


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE

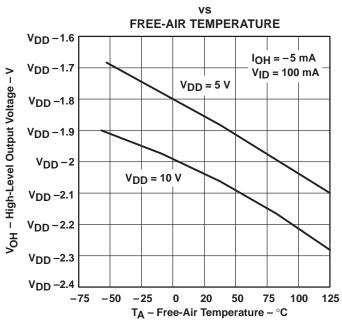
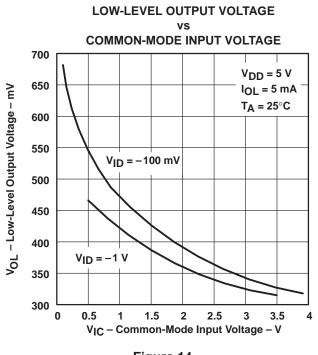


Figure 13



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS[†]





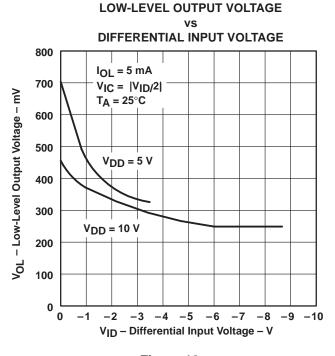


Figure 16

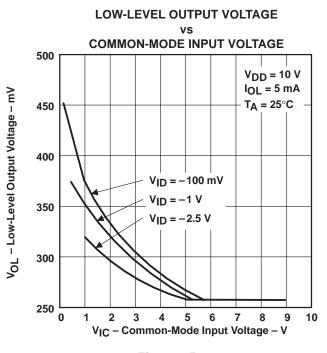


Figure 15

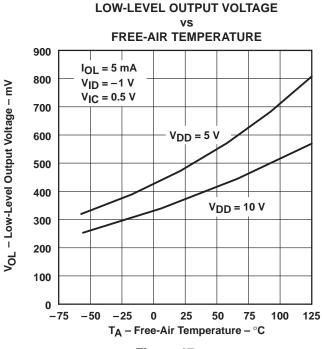


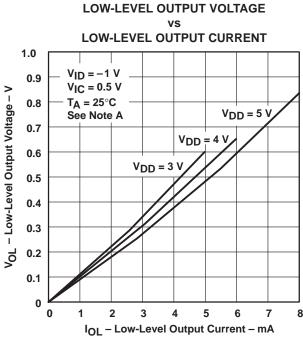
Figure 17

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



LOW-LEVEL OUTPUT VOLTAGE

TYPICAL CHARACTERISTICS[†]



NOTE A: The 3-V curve only applies to the C version. **Figure 18**

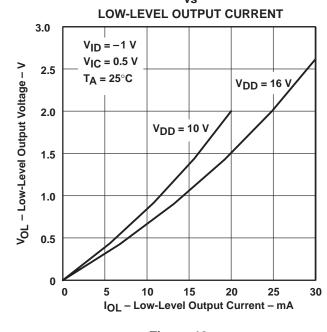
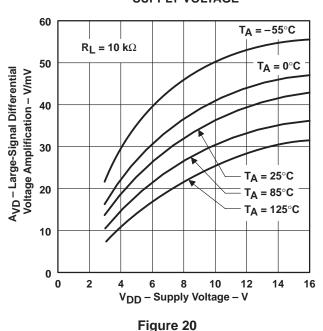
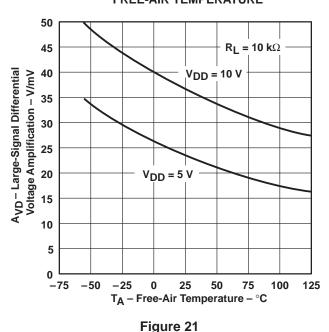


Figure 19





LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

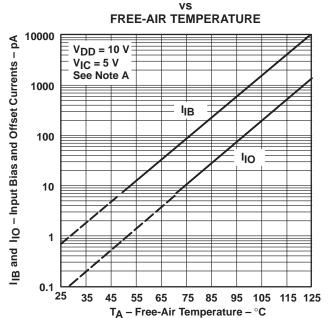


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS[†]

INPUT BIAS CURRENT AND INPUT OFFSET CURREN



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

SUPPLY VOLTAGE 16 T_A = 25°C 14 12

COMMON-MODE

INPUT VOLTAGE POSITIVE LIMIT

vs

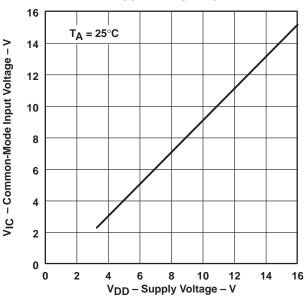
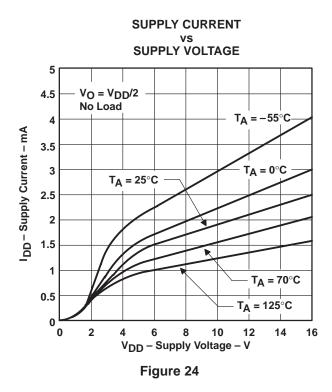


Figure 22

Figure 23



SUPPLY CURRENT vs FREE-AIR TEMPERATURE

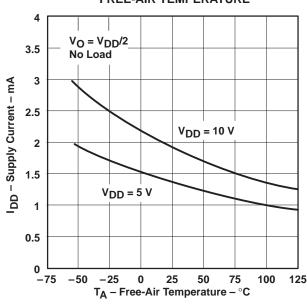


Figure 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



SLEW RATE

TYPICAL CHARACTERISTICS†

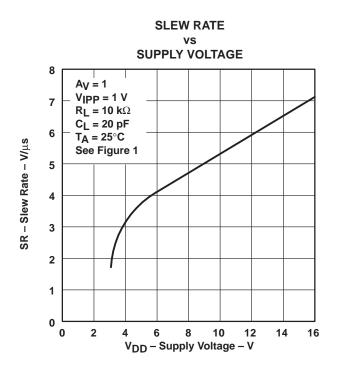


Figure 26

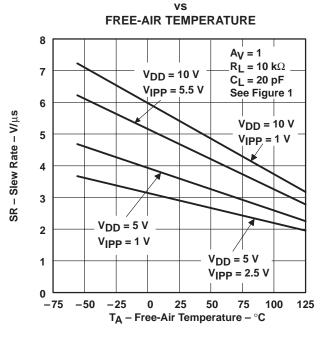
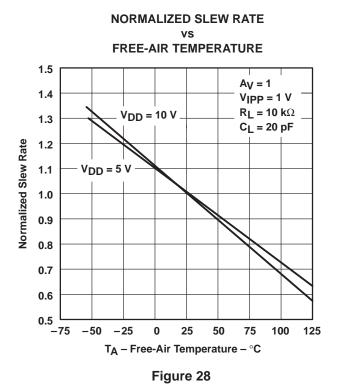
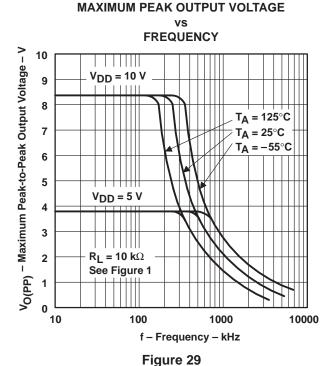


Figure 27

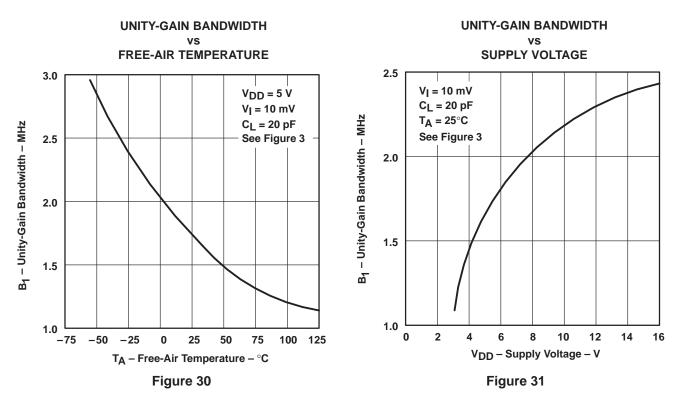




† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS[†]



LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT

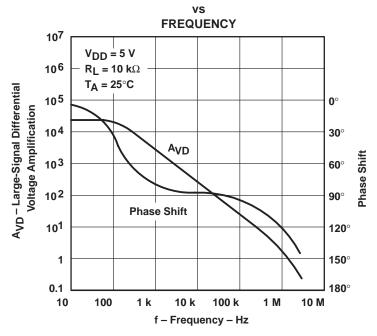


Figure 32

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS[†]

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT

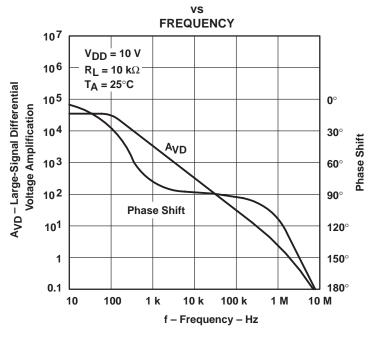
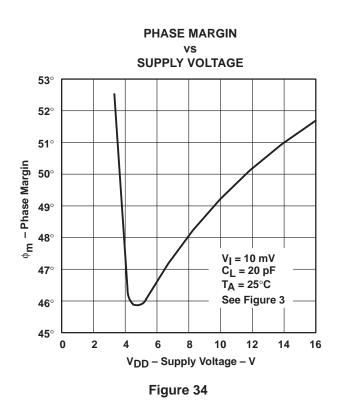


Figure 33



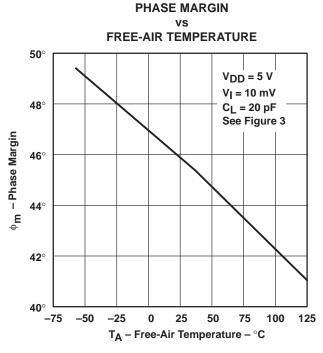
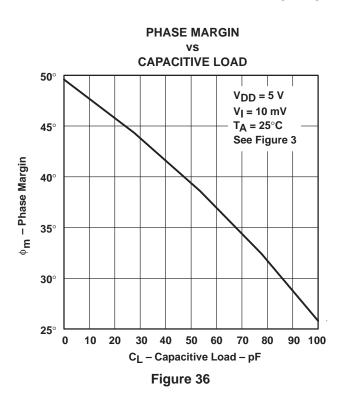
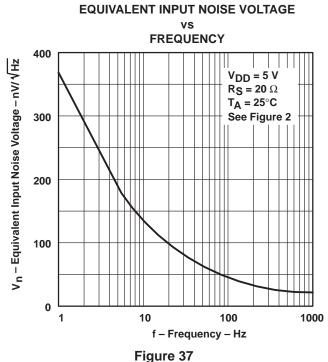


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS





single-supply operation

While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- 1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- 2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.

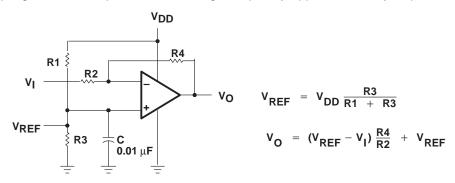
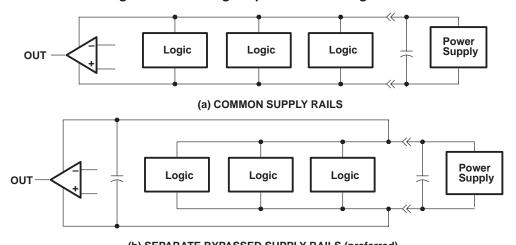


Figure 38. Inverting Amplifier With Voltage Reference



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common vs Separate Supply Rails

input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD}-1$ V at $T_A=25^{\circ}$ C and at $V_{DD}-1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

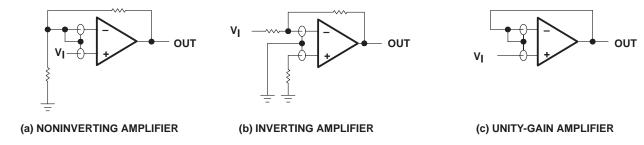


Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC272 and TLC277 are measured using a 20-pF load. The devices can drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



output characteristics (continued)

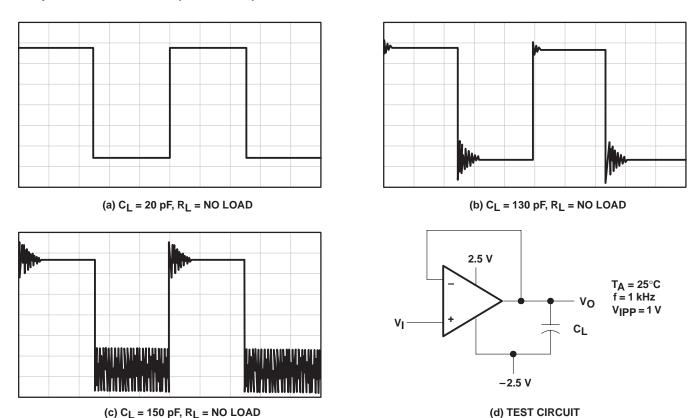
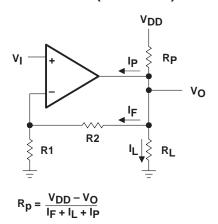


Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Second, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

output characteristics (continued)



 I_p = Pullup current required by the operational amplifier (typically 500 μ A)

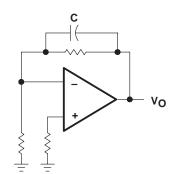


Figure 42. Resistive Pullup to Increase VOH

Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

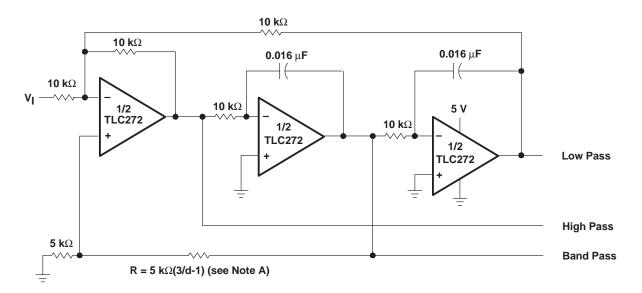
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand -100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.





NOTE A: d = damping factor, 1/Q

Figure 44. State-Variable Filter

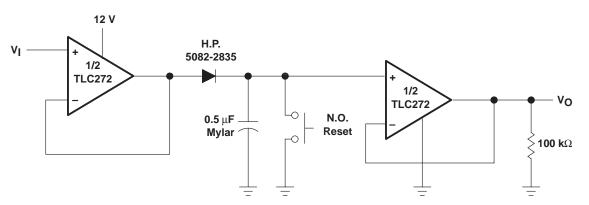
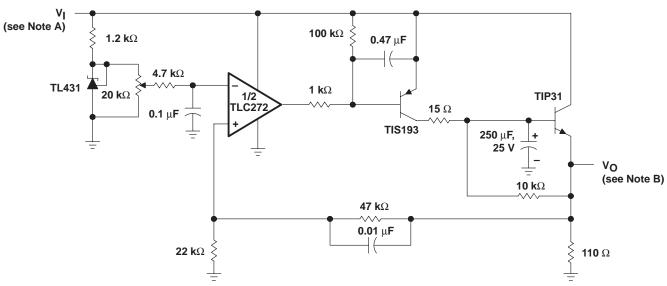
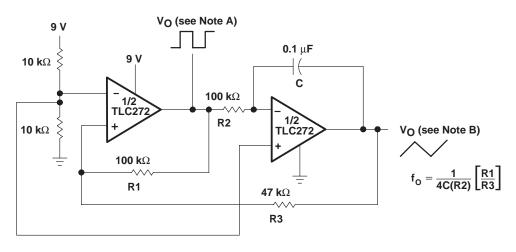


Figure 45. Positive-Peak Detector



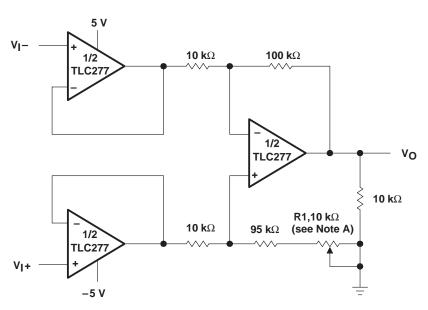
NOTES: A. $V_I = 3.5$ to 15 V B. $V_O = 2$ V, 0 to 1 A

Figure 46. Logic-Array Power Supply



NOTES: A. $V_{O(PP)} = 8 \text{ V}$ B. $V_{O(PP)} = 4 \text{ V}$

Figure 47. Single-Supply Function Generator



NOTE B: CMRR adjustment must be noninductive.

Figure 48. Low-Power Instrumentation Amplifier

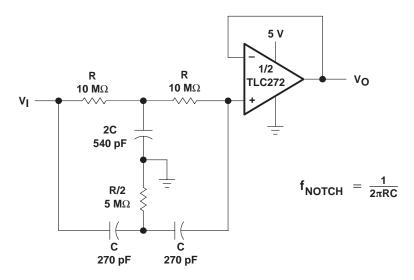


Figure 49. Single-Supply Twin-T Notch Filter

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BLOCK DIAGRAMS

PRODUCT SUPPORT: <u>DEVELOPMENT TOOLS</u> | <u>APPLICATIONS</u>

TLC272, Dual Single Supply Operational Amplifier

DEVICE STATUS: ACTIVE

PARAMETER NAME	TLC272
Vs (max) (V)	16
Vs (min) (V)	3
IQ per channel (max) (mA)	1.6
IQ per channel (typ) (mA)	0.7
GBW (typ) (MHz)	1.7
Slew Rate (typ) (V/us)	3.6
VIO (Full Range) (max) (mV)	12
VIO (25 deg C) (max) (mV)	10
IIB (max) (pA)	600
CMRR (min) (dB)	65
Vn at 1kHz (typ) (nV/rtHz)	25
Number of Channels	2
Spec'd at Vs (V)	5
Open Loop Gain (min) (dB)	74
Offset Drift (typ) (uV/C)	1.8

FEATURES <u>Back to Top</u>

- Trimmed Offset Voltage:
- TLC277...500 uV Max at 25°C,
- $\bullet V_{DD} = 5 V$
- Input Offset Voltage Drift...Typically
 0.1 uV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:
- 0°C to 70°C...3 V to 16 V

- -40°C to 85°C...4 V to 16 V
- -55°C to 125°C...4 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise...Typically 25 nV/ √ Hz\ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input impedance...10¹² Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-in Latch-Up Immunity

The TLC272 and TLC277 precision dual

operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas instruments silicon-gate LinCMOSTM

LinCMOS is a trademark of Texas Instruments Incorporated. technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the

low-cost TLC272 (10 mV) to the high-precision TLC277 (500 uV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

In general, many features associated with bipolar technology are available on LinCMOSTM operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand -100-mA surge currents without

sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.

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- Analog Applications Journal, September 1999 edition (SLYT005 Updated: 07/15/1999)
- Analysis Of The Sallen-Key Architecture (SLOA024A Updated: 07/27/1999)

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- Universal Operational Amplifier Evaluation Module Selection Guide (SLOU060A, 16 KB Updated: 09/28/2000)
- Universal Operational Amplifier Single, Dual, Quad (MSOP/TSSOP) (SLOU055, 1196 KB Updated: 10/22/1999)
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TLC272ID	<u>D</u>	8		ACTIVE		Request Samples
TLC272IP	<u>P</u>	8		ACTIVE		Request Samples

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	PACKAGE	PINS		STATUS	<u>BUDGETARY</u>			PRICING/AVAILABILITY
<u>ORDERABLE</u>			<u>TEMP</u>		<u>PRICE</u>	<u>PACK</u>	<u>DSCC</u>	

<u>DEVICE</u>			<u>(°C)</u>		<u>US\$/UNIT</u> <u>QTY=1000+</u>	<u>QTY</u>	NUMBER	
TLC272CD	<u>D</u>	8	0 TO 70	ACTIVE	0.49	75		Check stock or order
TLC272CDR	<u>D</u>	8	0 TO 70	ACTIVE	0.49	2500		Check stock or order
TLC272CP	<u>P</u>	8	0 TO 70	ACTIVE	0.49	50		Check stock or order
TLC272CPS	<u>PS</u>	8	0 TO 70	ACTIVE	0.49	80		Check stock or order
TLC272CPSR	<u>PS</u>	8	0 TO 70	ACTIVE	0.49	2000		Check stock or order
TLC272CPW	<u>PW</u>	8	0 TO 70	ACTIVE	0.49	150		Check stock or order
TLC272CPWLE	<u>PW</u>	8	0 TO 70	OBSOLETE				Replaced by TLC272CPWR
TLC272CPWR	<u>PW</u>	8	0 TO 70	ACTIVE	0.49	2000		Check stock or order
TLC272ID	<u>D</u>	8		ACTIVE	0.52	75		Check stock or order
TLC272IDR	<u>D</u>	8		ACTIVE	0.52	2500		Check stock or order
TLC272IP	<u>P</u>	8		ACTIVE	0.52	50		Check stock or order
TLC272IPW	<u>PW</u>	8		PREVIEW				Check stock or order
TLC272MFKB	<u>FK</u>	20	-55 TO 125	OBSOLETE				
TLC272MJG	<u>JG</u>	8	-55 TO 125	OBSOLETE				
TLC272MJGB	<u>JG</u>	8	-55 TO 125	OBSOLETE				
TLC272P-M	<u>P</u>	8		PREVIEW				Check stock or order

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UNIV-OPAMP- 4B	Universal EVM for Single/Dual/Quad OpAmps with/without Shutdown in SOIC packages	Evaluation Modules (EVM)
UNIV-OPAMP- 5B	Universal EVM for Single/Dual/Quad OpAmps with/without Shutdown in PDIP packages	Evaluation Modules (EVM)

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TLC272A, LinCMOS(TM) Precision Dual Operational Amplifier

DEVICE STATUS: ACTIVE

PARAMETER NAME	TLC272A
Vs (max) (V)	16
Vs (min) (V)	3
IQ per channel (max) (mA)	1.6
IQ per channel (typ) (mA)	0.7
GBW (typ) (MHz)	1.7
Slew Rate (typ) (V/us)	3.6
VIO (Full Range) (max) (mV)	6.5
VIO (25 deg C) (max) (mV)	5
IIB (max) (pA)	600
CMRR (min) (dB)	65
Vn at 1kHz (typ) (nV/rtHz)	25
Number of Channels	2
Spec'd at Vs (V)	5
Open Loop Gain (min) (dB)	74
Offset Drift (typ) (uV/C)	1.8

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- Trimmed Offset Voltage:
- TLC277...500 uV Max at 25°C,
- $V_{DD} = 5 V$
- Input Offset Voltage Drift...Typically
 0.1 uV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:
- 0°C to 70°C...3 V to 16 V
- -40°C to 85°C...4 V to 16 V

- -55°C to 125°C...4 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise...Typically 25 nV/ √ Hz\ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input impedance...10¹² Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-in Latch-Up Immunity

The TLC272 and TLC277 precision dual

operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas instruments silicon-gate LinCMOSTM

LinCMOS is a trademark of Texas Instruments Incorporated. technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the

low-cost TLC272 (10 mV) to the high-precision TLC277 (500 uV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

In general, many features associated with bipolar technology are available on LinCMOSTM operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.

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- Analysis Of The Sallen-Key Architecture (SLOA024A Updated: 07/27/1999)

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- <u>Universal Operational Amplifier Evaluation Module Selection Guide</u> (SLOU060A, 16 KB Updated: 09/28/2000)
- Universal Operational Amplifier Single, Dual, Quad (MSOP/TSSOP) (SLOU055, 1196 KB Updated: 10/22/1999)
- <u>Universal Operational Amplifier Single, Dual, Quad (PDIP)</u> (SLOU062, 1211 KB Updated: 10/22/1999)

PRICING/AVAILABILITY

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ORDERABLE DEVICE	PACKAGE	<u>PINS</u>	TEMP (°C)	<u>STATUS</u>	BUDGETARY PRICE US\$/UNIT QTY=1000+	PACK QTY	PRICING/AVAILABILITY
TLC272ACD	<u>D</u>	8		ACTIVE	0.52	75	Check stock or order
TLC272ACDR	<u>D</u>	8		ACTIVE	0.52	2500	Check stock or order
TLC272ACP	<u>P</u>	8		ACTIVE	0.52	50	Check stock or order
TLC272ACPS	<u>PS</u>	8		ACTIVE	0.52	80	Check stock or order
TLC272ACPSR	<u>PS</u>	8		ACTIVE	0.52	2000	Check stock or order
TLC272AID	<u>D</u>	8		ACTIVE	0.55	75	Check stock or order
TLC272AIDR	<u>D</u>	8		ACTIVE	0.55	2500	Check stock or order

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TLC272AIP	<u>P</u>	8	ACTIVE	0.55	50	Check stock or order
TLC272AIP10	<u>P</u>	8	PREVIEW			Check stock or order

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Tool Part Number	Tool Title	Tool Type
UNIV-OPAMP- 1B	Universal EVM for Single/Dual OpAmps without Shutdown in MSOP/SOIC/SOT-23 packages	Evaluation Modules (EVM)
UNIV-OPAMP- 2B	Universal EVM for Single/Dual OpAmps with Shutdown in MSOP/SOIC/SOT-23 packages	Evaluation Modules (EVM)
UNIV-OPAMP- 3B	Universal EVM for Single/Dual/Quad OpAmps with/without Shutdown in MSOP/TSSOP packages	Evaluation Modules (EVM)
UNIV-OPAMP- 4B	Universal EVM for Single/Dual/Quad OpAmps with/without Shutdown in SOIC packages	Evaluation Modules (EVM)
UNIV-OPAMP- 5B	Universal EVM for Single/Dual/Quad OpAmps with/without Shutdown in PDIP packages	Evaluation Modules (EVM)

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PRODUCT SUPPORT: <u>DEVELOPMENT TOOLS</u> | <u>APPLICATIONS</u>

TLC272B, LinCMOS Precision Dual Operational Amplifier

DEVICE STATUS: ACTIVE

PARAMETER NAME	TLC272B
Vs (max) (V)	16
Vs (min) (V)	3
IQ per channel (max) (mA)	1.6
IQ per channel (typ) (mA)	0.7
GBW (typ) (MHz)	1.7
Slew Rate (typ) (V/us)	3.6
VIO (Full Range) (max) (mV)	3
VIO (25 deg C) (max) (mV)	2
IIB (max) (pA)	600
CMRR (min) (dB)	65
Vn at 1kHz (typ) (nV/rtHz)	25
Number of Channels	2
Spec'd at Vs (V)	5
Open Loop Gain (min) (dB)	74
Offset Drift (typ) (uV/C)	1.8

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- Trimmed Offset Voltage:
- TLC277...500 uV Max at 25°C,
- $\bullet V_{DD} = 5 V$
- Input Offset Voltage Drift...Typically
 0.1 uV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:
- 0°C to 70°C...3 V to 16 V
- -40°C to 85°C...4 V to 16 V

- -55°C to 125°C...4 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise...Typically 25 nV/ √ Hz\ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input impedance...10¹² Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-in Latch-Up Immunity

The TLC272 and TLC277 precision dual

operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas instruments silicon-gate LinCMOSTM

LinCMOS is a trademark of Texas Instruments Incorporated. technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the

low-cost TLC272 (10 mV) to the high-precision TLC277 (500 uV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

In general, many features associated with bipolar technology are available on LinCMOSTM operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.

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- Analog Applications Journal, September 1999 edition (SLYT005 Updated: 07/15/1999)
- Analysis Of The Sallen-Key Architecture (SLOA024A Updated: 07/27/1999)

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- Universal Operational Amplifier Evaluation Module Selection Guide (SLOU060A, 16 KB -Updated: 09/28/2000)
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- Universal Operational Amplifier Single, Dual, Quad (PDIP) (SLOU062, 1211 KB Updated: 10/22/1999)

PRICING/AVAILABILITY

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ORDERABLE DEVICE	PACKAGE	<u>PINS</u>	TEMP (°C)	<u>STATUS</u>	BUDGETARY PRICE US\$/UNIT QTY=1000+	PACK QTY	PRICING/AVAILABILITY
TLC272BCD	<u>D</u>	8		ACTIVE	0.55	75	Check stock or order
TLC272BCDR	<u>D</u>	8		ACTIVE	0.55	2500	Check stock or order
TLC272BCP	<u>P</u>	8		ACTIVE	0.55	50	Check stock or order
TLC272BCPS	<u>PS</u>	8		ACTIVE	0.55	80	Check stock or order
TLC272BCPSR	<u>PS</u>	8		ACTIVE	0.55	2000	Check stock or order
TLC272BID	<u>D</u>	8		ACTIVE	0.56	75	Check stock or order
TLC272BIDR	<u>D</u>	8		ACTIVE	0.56	2500	Check stock or order

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TLC272BIP	<u>P</u>	8	ACTIVE	0.56	50	Check stock or order

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Tool Part Number	Tool Title	Tool Type
UNIV-OPAMP- 1B	Universal EVM for Single/Dual OpAmps without Shutdown in MSOP/SOIC/SOT-23 packages	Evaluation Modules (EVM)
UNIV-OPAMP- 2B	Universal EVM for Single/Dual OpAmps with Shutdown in MSOP/SOIC/SOT-23 packages	Evaluation Modules (EVM)
UNIV-OPAMP- 3B	Universal EVM for Single/Dual/Quad OpAmps with/without Shutdown in MSOP/TSSOP packages	Evaluation Modules (EVM)
UNIV-OPAMP- 4B	Universal EVM for Single/Dual/Quad OpAmps with/without Shutdown in SOIC packages	Evaluation Modules (EVM)
UNIV-OPAMP- 5B	Universal EVM for Single/Dual/Quad OpAmps with/without Shutdown in PDIP packages	Evaluation Modules (EVM)

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APPLICATION NOTES | USER MANUALS

PRODUCT SUPPORT: <u>DEVELOPMENT TOOLS</u> | <u>APPLICATIONS</u>

TLC277, Dual Precision Single Supply Operational Amplifier

DEVICE STATUS: ACTIVE

PARAMETER NAME	TLC277
Vs (max) (V)	16
Vs (min) (V)	3
IQ per channel (max) (mA)	1.6
IQ per channel (typ) (mA)	0.7
GBW (typ) (MHz)	1.7
Slew Rate (typ) (V/us)	3.6
VIO (Full Range) (max) (mV)	1.5
VIO (25 deg C) (max) (mV)	0.5
IIB (max) (pA)	600
CMRR (min) (dB)	65
Vn at 1kHz (typ) (nV/rtHz)	25
Number of Channels	2
Spec'd at Vs (V)	5
Open Loop Gain (min) (dB)	74
Offset Drift (typ) (uV/C)	1.8

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- Trimmed Offset Voltage:
- TLC277...500 uV Max at 25°C,
- $V_{DD} = 5 V$
- Input Offset Voltage Drift...Typically
 0.1 uV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:
- 0°C to 70°C...3 V to 16 V
- -40°C to 85°C...4 V to 16 V

- -55°C to 125°C...4 V to 16 V
- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise...Typically 25 nV/ √ Hz\ at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input impedance...10¹² Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-in Latch-Up Immunity

The TLC272 and TLC277 precision dual

operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas instruments silicon-gate LinCMOSTM

LinCMOS is a trademark of Texas Instruments Incorporated. technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the

low-cost TLC272 (10 mV) to the high-precision TLC277 (500 uV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

In general, many features associated with bipolar technology are available on LinCMOSTM operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.

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TLC277ID	<u>D</u>	8		ACTIVE		Request Samples
TLC277IP	<u>P</u>	8		ACTIVE		Request Samples

PRICING/AVAILABILITY

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ORDERABLE DEVICE	PACKAGE	<u>PINS</u>	<u>TEMP</u> (°C)	<u>STATUS</u>	BUDGETARY PRICE US\$/UNIT QTY=1000+	PACK QTY	<u>DSCC</u> NUMBER	PRICING/AVAILABILITY
5962- 89494022A	<u>FK</u>	20	-55 TO 125	OBSOLETE				
TLC277CD	<u>D</u>	8		ACTIVE	0.84	75		Check stock or order

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TLC277CDR	<u>D</u>	8		ACTIVE	0.84	2500	Check stock or order
TLC277CP	<u>P</u>	8		ACTIVE	0.84	50	Check stock or order
TLC277CPS	<u>PS</u>	8		ACTIVE	0.84	80	Check stock or order
TLC277CPSR	<u>PS</u>	8		ACTIVE	0.84	2000	Check stock or order
TLC277ID	<u>D</u>	8		ACTIVE	0.88	75	Check stock or order
TLC277IDR	<u>D</u>	8		ACTIVE	0.88	2500	Check stock or order
TLC277IP	<u>P</u>	8		ACTIVE	0.88	50	Check stock or order
TLC277MFKB	<u>FK</u>	20	-55 TO 125	OBSOLETE			
TLC277MJG	<u>JG</u>	8	-55 TO 125	OBSOLETE			
TLC277MJGB	<u>JG</u>	8	-55 TO 125	OBSOLETE			

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