USB97C242

USB 2.0 Flash Drive Controller

Datasheet

Product Features

- 2.5 Volt, Low Power Core Operation
- 3.3 Volt I/O with 5V input tolerance
- Complete USB Specification 2.0 Compatibility
  - Includes USB 2.0 Transceiver
  - A Bi-directional Control and a Bi-directional Bulk Endpoint are provided.
- Complete System Solution for interfacing SmartMedia (SM), and NAND flash devices to USB 2.0 bus
  - Supports USB Bulk Only Mass Storage Compliant Bootable BIOS
  - Support for the following devices:
    - SM: 2M –15MB/sec
    - NAND Flash: 2M – 15MB/sec
  - Built-in hardware 1-bit ECC support.
- 8051 8 bit microprocessor
  - Provides low speed control functions
  - 30 Mhz execution speed at 4 cycles per instruction average
  - 12K Bytes of internal SRAM for general purpose scratchpad
  - 768 Bytes of internal SRAM for general purpose scratchpad or program execution with external flash
- Double Buffered Bulk Endpoint
  - Bi-directional 512 Byte Buffer for Bulk Endpoint
  - 64 Byte RX Control Endpoint Buffer
  - 64 Byte TX Control Endpoint Buffer
- Internal or External Program Memory Interface
  - 48K Byte Internal Code Space or optional 64K Byte External Code Space using Flash, SRAM, or EPROM memory.
- On Board 12Mhz Crystal Driver Circuit
- Internal PLL for 480Mhz USB2.0 Sampling, 30Mhz MCU clock
- Supports firmware upgrade via USB bus if sector-erasable Flash program memory is used
- 7 GPIOs for special function use: LED indicators, button inputs, power control to memory devices, etc.
  - Inputs capable of generating interrupts with either edge sensitivity
- 100 Pin TQFP (12x12x1.4 body) Lead-Free RoHS Compliant Package also available

ORDERING INFORMATION

Order Number(s):

USB97C242-MN-xx for 100 pin TQFP package

USB97C242-MV-04 for 100 pin TQFP Lead-Free RoHS Compliant Package

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

USB97C242 Revision History

PAGE(S)	SECTION/FIGURE/ENTRY	CORRECTION	DATE REVISED
1	Cover	Added lead-free ordering information	Rev. 1.4 02-16-06
5	Chapter 1 – General Description	First bullet modified under the following section: Internal program code provides the following features: ▪ Support for 1 to 8, 128Mb through 2Gb, 512byte and 2048 byte page size, 8bit parallel NAND flash memories, including multiple memory aggregates in multi-chip-modules (MCM) up to 8, 2Gb devices (ie 16Gb), as long as individual memory device Chip Enables are pinned out in the MCM.	Rev. 1.3 07-08-04
16	Table 7.1 - DC Electrical Characteristics	Updated High Input Leakage units.	Rev. 1.2 11-05-03
5	Chapter 1 - General Description	Revised list of object code software and licenses; internal program code features	Rev. 1.1 04-03-03
8	Chapter 3 - Pin TablesTable 3.1 – USB97C242 100 Pin Package	Updated tables	Rev. 1.1 04-03-03
10	Figure 4.1 – 100 Pin TQFP	Diagram updated, new pin names	Rev. 1.1 04-03-03
12	Table 6.1 – USB97C242 Pin Descriptions	Updated misc pin section	Rev. 1.1 04-03-03
22	Table 11.1 - GPIO Usage	Updated table	Rev. 1.1 04-03-03
23	Chapter 12 - Typical Application	Typical application diagram deleted	Rev. 1.1 04-03-03

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1 General Description

The USB97C242 is a USB2.0 Bulk Only Mass Storage Class Peripheral Controller intended for supporting SmartMedia (SM), and NAND flash memory devices. It provides a single chip USB reader solution for the SM and NAND flash devices in the market*.

The device consists of a USB 2.0 PHY and SIE, buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, 48KB program ROM and SM controller.

Provisions for optional external Flash Memory up to 64K bytes for program storage is provided.

12K bytes of scratchpad SRAM and 768Bytes of scratchpad SRAM are also provided.

Seven GPIO pins are for the 100-pin device. Provisions are made to allow dynamic attach and re-attach to the USB bus to allow hot swap of flash media to be implemented.

SMSC provides the following object code software and licenses free of charge with purchase of the USB97C242**:

- Windows 98 Mass Storage Class driver.
- Windows application for programming VID/PID/OEM strings, and unique serial number into serial EEPROM (SM reader) or NAND Flash via USB.
- Production test and format utilities
- Password protection API and example applet.
- Firmware with field upgrade capability via USB (requires external specific model 128KB Flash for firmware storage).

The Internal program code provides the following features:

- Support for 1 to 8, 128Mb through 2Gb, 512byte and 2048 byte page size, 8bit parallel NAND flash memories, including multiple memory aggregates in multi-chip-modules (MCM) up to 8, 2Gb devices (ie 16Gb), as long as individual memory device Chip Enables are pinned out in the MCM.
- Autodetection of NAND Flash memory type and capacity
- Supports write protect switch
- Wear leveling
- Internal VID/PID/Serial Number/OEM String storage in NAND flash itself, eliminating need for external serial EEPROM
- High performance transfers (interleaving, copy block caching, etc.)
- Drive password protection

SMSC may make complete internal specifications available for those customers requiring programming information, subject to SMSC's applicable Proprietary Information Agreement (nondisclosure agreement). Contact your SMSC sales representative for more information.**

Note:

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Chapter 2 Acronyms & Definition

2.1 Acronyms

SM: SmartMedia

SMC: SmartMedia Controller

FM: Flash Media

FMC: Flash Media Controller

ECC: Error Checking and Correcting

CRC: Cyclic Redundancy Checking

Chapter 3 Pin Tables

Table 3.1 – USB97C242 100 Pin Package

NAND FLASH/SMARTMEDIA INTERFACE (17 PINS)			
D0	D1	D2	D3
D4	D5	D6	D7
ALE	CLE	nRE	nWE
nWP	nB/R	nCE	nCD
nWPS			
USB INTERFACE (7 PINS)			
USB+	USB-	LOOPFLTR	RBIAS
RTERM	FS+	FS-	
MEMORY/IO INTERFACE (29 PINS)			
MA0	MA1	MA2	MA3
MA4	MA5	MA6	MA7
MA8	MA9	MA10	MA11
MA12	MA13	MA14	MA15
MD0	MD1	MD2	MD3
MD4	MD5	MD6	MD7
nMRD	nMWR	nMCE	
nIOW	nIOR		
MISC (21 PINS)			
ROMEN	GPIO1	GPIO20	GPIO3
GPIO4	GPIO5	GPIO6	GPIO7
XTAL1/CLKIN	XTAL2	nRESET	
nCS4	nCS5	nCS6	nCS7
nCS0	nCS1	nCS2	nCS3
nTEST0	nTEST1		
POWER, GROUNDS, AND NC (26 PINS)			
TOTAL 100			

3.1 100 Pin List

Table 3.2 – 100 Pin TQFP

PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
1	MA0	8	26	MD5	8	51	nWE	12	76	RBIAS	
2	MA1	8	27	MD6	8	52	nWP	12	77	*VDDA*	
3	MA2	8	28	MD7	8	53	nCE	8	78	FS+	
4	MA3	8	29	nMRD	8	54	nWPS		79	USB+	
5	MA4	8	30	nMWR	8	55	nB/R		80	USB-	
6	MA5	8	31	*VSSIO*	8	56	nCD		81	FS-	
7	MA6	8	32	nMCE	8	57	nCS0		82	RTERM	
8	MA7	8	33	nIOW	8	58	*VDDCORE*		83	*VSSA*	

PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
9	MA8	8	34	nIOR	8	59	nCS1		84	XTAL1/CLKIN	
10	MA9	8	35	ROMEN		60	*VSSCORE*		85	XTAL2	
11	MA10	8	36	D0	12	61	nCS2		86	*VSSP*	
12	*VDDCORE*		37	D1	12	62	*VDDIO*		87	LOOPFLTR	
13	MA11	8	38	D2	12	63	nCS3		88	*VDDP*	
14	*VSSCORE*		39	*VDDCORE*		64	nCS4		89	GPIO1	8
15	*VSSIO*		40	D3	12	65	*VSSIO*		90	GPIO2	8
16	MA12	8	41	*VSSCORE*		66	nCS5		91	GPIO3	8
17	MA13	8	42	D4	12	67	nCS6		92	GPIO4	8
18	MA14	8	43	*VDDIO*		68	nCS7		93	GPIO5	8
19	MA15	8	44	D5	12	69	NC		94	GPIO6	8
20	*VDDIO*		45	D6	12	70	NC		95	GPIO7	8
21	MD0	8	46	D7	12	71	NC		96	nRESET	
22	MD1	8	47	ALE	12	72	NC		97	*VSSIO*	
23	MD2	8	48	*VSSIO*		73	NC		98	nTEST0	
24	MD3	8	49	nRE	24	74	NC		99	*VDDIO*	
25	MD4	8	50	CLE	12	75	NC		100	nTEST1	

Chapter 4 Pin Configuration

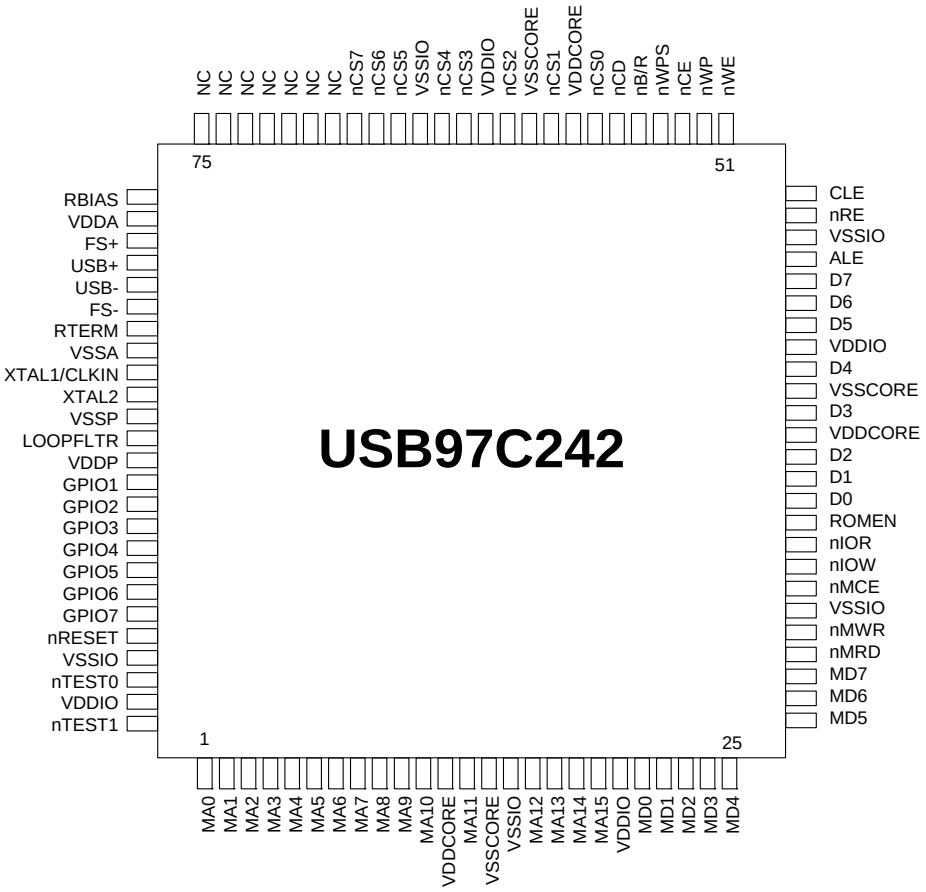
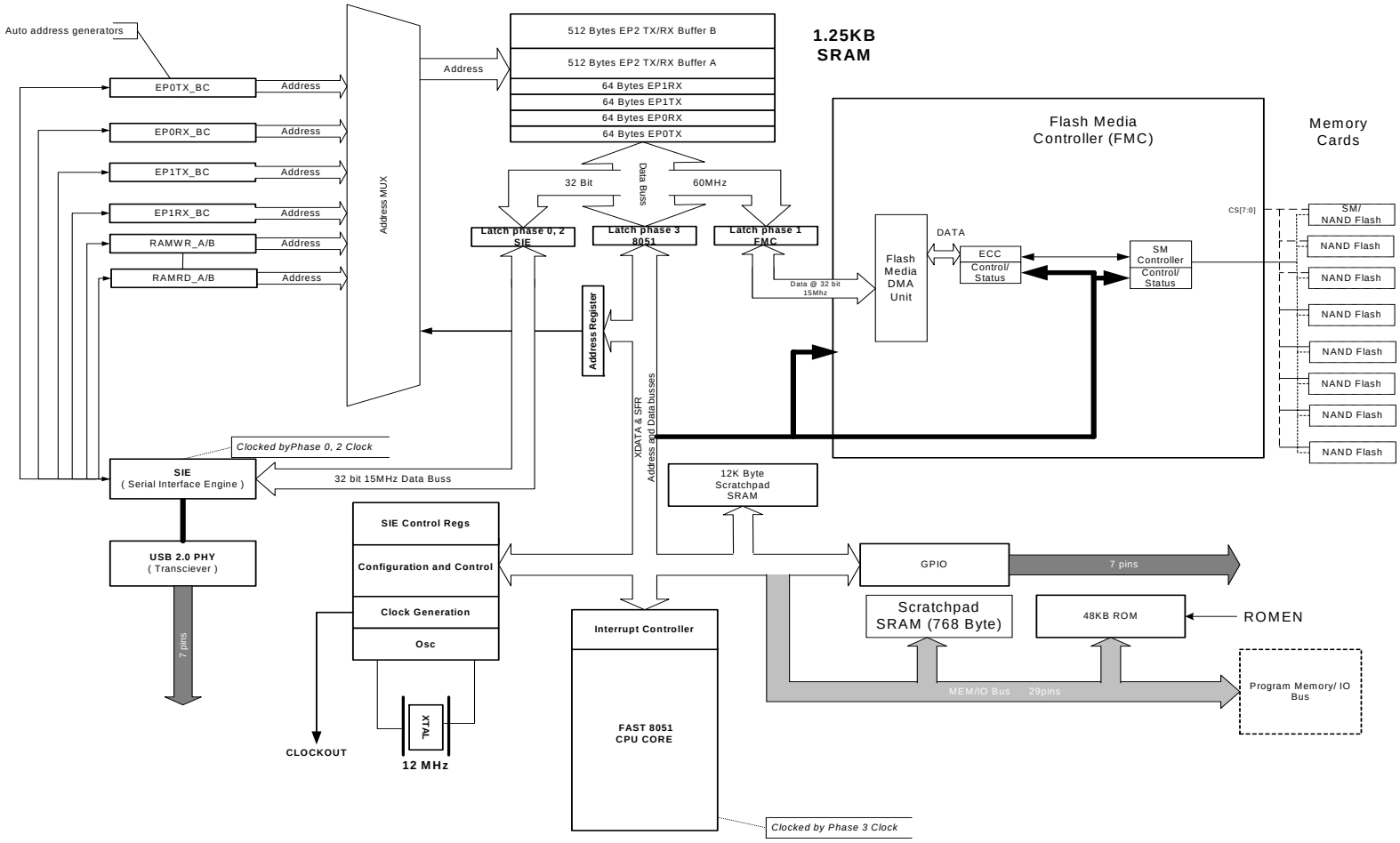


Figure 4.1 – 100 Pin TQFP

Chapter 5 Block Diagram



Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

Table 6.1 – USB97C242 Pin Descriptions

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
NAND FLASH/SMARTMEDIA INTERFACE			
SM Write Protect	nWP	O12	This pin is an active low write protect signal for the SM or NAND flash device.
SM Address Strobe	ALE	O12	This pin is an active high Address Latch Enable signal for the SM or NAND flash device.
SM Command Strobe	CLE	O12	This pin is an active high Command Latch Enable signal for the SM or NAND flash device.
SM Data7-0	D[7:0]	I/OPU12	These pins are the bi-directional data signal D7-D0. The bi-directional input signal should have an internal weak pull-up resister on the input.
SM Read Enable	nRE	O24	This pin is an active low read strobe signal for SM or NAND flash device.
SM Write Enable	nWE	O12	This pin is an active low write strobe signal for SM or NAND flash device.
SM Write Protect Switch	nWPS	IPU	A write-protect seal is detected, when this pin is low. This pin has an internal weak pull-up resistor.
SM Busy or Data Ready	nB/R	IPU	This pin is connected to the BSY/RDY pin of the SM or NAND flash device. This pin has an internal weak pull-up resistor.
SM Chip Enable	nCE	OPU8	This pin is the active low chip enable signal to the SM or NAND flash device. This pin should be used to support a single SM or NAND flash device only.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
SM Card Detection	nCD	IPU	This is the card detection signal from SM device to indicate if the device is inserted. This pin has internal weak pull-up resistor.
USB INTERFACE			
USB Bus Data	USB- USB+	I/O-U	These pins connect to the USB bus data signals.
USB Transceiver Filter	LOOPFLTR		This pin provides the ability to supplement the internal filtering of the transceiver with an external network, if required.
USB Transceiver Bias	RBIAS		A precision 9.09K resistor is attached from ground to this pin to set the transceiver's internal bias currents.
Termination Resistor	RTERM		A precision 1.5K resistor is attached to this pin from a 3.3V supply.
Full Speed USB Data	FS- FS+	I/O-U	These pins connect to the USB- and USB+ pins through 31.6 ohm series resistors.
MEMORY/IO INTERFACE			
Memory Data Bus	MD[7:0]	I/OPU8	When ROMEN = 0, these signals are used to transfer data between the internal CPU and the external program memory. When ROMEN = 1, internal weak pull up are activated to prevent these pins from floating.
Memory Address Bus	MA[15:0]	O8	These signals address memory locations within the external memory.
Memory Read Strobe	nMWR	O8	Program Memory Write; active low
Memory Read Strobe	nMRD	O8	Program Memory Read; active low
Memory Chip Enable	nMCE	O8	Program Memory Chip Enable; active low. This signal shall be de-asserted, when all of the following conditions are met: IDLE bit (PCON.0) is 1. INT2 is negated SLEEP bit of CLOCK_SEL is 1. This signal shall be asserted whenever any of the three conditions are no longer met.
I/O Read Strobe	nIOR	O8	This is a active low I/O Read strobe signal of Xdata bus.
I/O Write Strobe	nIOW.	O8	This is a active low I/O Write strobe signal of Xdata bus.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
MISC			
Crystal Input/External Clock Input	XTAL1/ CLKIN	ICLKx	12Mhz Crystal or external clock input. This pin can be connected to one terminal of the crystal or can be connected to an external 12Mhz clock when a crystal is not used.
Crystal Output	XTAL2	OCLKx	12Mhz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.
Internal ROMEN	ROMEN	IPU	When tied low, an external program memory should be connected to the memory/data bus. The USB97C242 uses this external bus for program execution. When this pin is left unconnected or tied high, the USB97C242 uses the internal ROM for program execution. The state of this pin is latched internally on the rising edge of nRESET to determine if internal or external program memory is used. The state latched is stored in ROMEN bit of GPIO_IN1 register.
General Purpose I/O	GPIO1	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output. See Chapter 11 for usage by program in internal ROM.
General Purpose I/O	GPIO2	I/OPU8	This pin may be used either as input, edge sensitive interrupt input, or output. See Chapter 11 for usage by program in internal ROM.
General Purpose I/O	GPIO3	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output. See Chapter 11 for usage by program in internal ROM.
General Purpose I/O	GPIO[7:4]	I/O8	These pins may be used either as input, edge sensitive interrupt input, or output. See Chapter 11 for usage by program in internal ROM.
NAND flash Chip Select Signal	nCS[7:0]	OPU8	These pins can be used to chip enable the NAND flash devices, when multiple NAND flash devices are used.
RESET input	nRESET	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 100ns wide.
TEST Input	nTEST[0:1]	I	These signals are used for testing the chip. User should normally leave them unconnected.
POWER, GROUNDS, AND NO CONNECTS			
	VDD		+2.5V Core power
	VDDIO		+3.3V I/O power
	VDDP		+2.5 Analog power
	VSSP		Analog Ground Reference
	VDDA		+3.3V Analog power
	VSSA		Analog Ground Reference
	GND		Ground Reference

Note: nMCE is normally asserted except when the 8051 is in standby mode.

6.1 Buffer Type Descriptions

Table 6.2 - USB97C242 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IPU	Input with internal weak pull-up resistor.
IPD	Input with internal weak pull-down resistor.
IS	Input with Schmitt trigger
I/O4	Input/Output with 4mA drive
I/OD4	Input/Open drain output … 4mA sink
I/O8	Input/Output with 8mA drive
I/OD8	Input/Open drain output … 8mA sink
I/OPD8	Input/Output with 8mA drive and controlled weak pull down.
I/OPU8	Input/Output with 8mA drive and controlled weak pull up.
O4	Output with 4mA drive
O8	Output with 8mA drive
OPD8	Output with 8mA drive and controlled weak pull down.
OPU8	Output with 8mA drive and controlled weak pull up.
I/O12	Output with 12mA drive
I/OPU12	Input/Output with 12mA drive and controlled weak pull up on input.
OPU12	Output with 12mA drive and controlled weak pull up.
OPD12	Output with 12mA drive and controlled weak pull down.
O12	Output with 12mA drive
OD12	Open drain….12mA sink
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Defined in USB specification

Chapter 7 DC Parameters

7.1 Maximum Guaranteed Ratings

Operating Temperature Range ..... 0^oC to $+70^oC$
Storage Temperature Range ..... -55^o to $+150^oC$
Lead Temperature Range (soldering, 10 seconds) ..... $+325^oC$
Positive Voltage on any pin, with respect to Ground 5.5V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum V_{DD}, V_{DDP} ..... +3.0V
Maximum V_{DDIO}, V_{DDA} ..... +4.0V

*Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

Table 7.1 - DC Electrical Characteristics

(T_A = 0°C - 70°C, V_{DDIO}, V_{DDA}= +3.3 V ± 10%, V_{DD}, V_{DDP} = *+2.5 V* ± 10%,)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	uA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	uA	V_{IN} = V_{DDIO}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	uA	V_{IN} = 0 to V_{DDIO} (Note 7.1)
I/O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -4 mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DDIO} (Note 7.1)
I/O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ V_{DDIOE} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DDIO} (Note 7.1,Note 7.3)
I/O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DDIO} (Note 7.1,Note 7.3)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO-U Note 7.2						
Supply Current Unconfigured	I_{CCINIT}		85 60		mA mA	@ V_{DD}, V_{DDP} = 2.5V @ V_{DDIO}, V_{DDA} = 3.3V
Supply Current Active	I_{CC}		85 60	110 70	mA mA	@ V_{DD}, V_{DDP} = 2.5V @ V_{DDIO}, V_{DDA} = 3.3V
Supply Current Standby	I_{CSBY}			150 150	µA	@ V_{DD}, V_{DDP} = 2.5V @ V_{DDIO}, V_{DDA} = 3.3V

Note 7.1 Output leakage is measured with the current pins in high impedance.

Note 7.2 See Appendix A for USB DC electrical characteristics.

Note 7.3 Output leakage is valid only on pins without internal weak pull ups or pull downs.

7.1.1 Capacitance TA = 25°C; FC = 1MHz; VDD, VDDP = 2.5V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Chapter 8 AC Specifications

Refer to the appropriate specification document in the chapter of “Reference” for each flash media device or USB interface.

Chapter 9 Package Outline

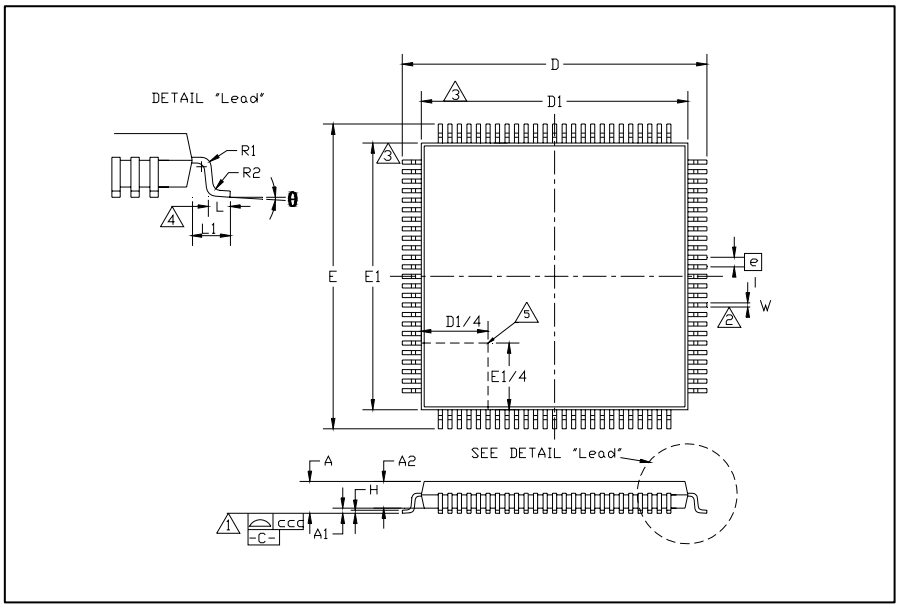


Figure 9.1 – 100 Pin TQFP Package Outline, 12x12x1.4 Body (Rev A)

Table 9.1 – 100 Pin TQFP Package Parameters (Rev A)

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	13.80	~	14.20	X Span
D1	11.80	~	12.20	X body Size
E	13.80	~	14.20	Y Span
E1	11.80	~	12.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e		0.40 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.13	0.16	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:
[1] Controlling Unit: millimeter.
[2] Tolerance on the position of the leads is ± 0.035 mm maximum.
[3] Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm.
[4] Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
[5] Details of pin 1 identifier are optional but must be located within the zone indicated.

Chapter 10 Reference

1. SmartMedia™ Electrical Specification Version 1.30
2. SmartMedia™ Physical Format Specifications Version 1.30
3. SmartMedia™ Logical Format Specifications Version 1.20
4. SMIL (SmartMedia Interface Library) Software Edition Version 1.00, Toshiba Corporation, 01, July, 2000
5. SMIL (SmartMedia Interface Library) Hardware Edition Version 1.00, Toshiba Corporation, 01, July, 2000
6. K9K2G08U0M, 256Mx8 Bit NAND Flash Memory Data Sheet, Samsung.
7. Universal Serial Bus Specification Rev 2.0

Chapter 11 GPIO Usage Table

Table 11.1 - GPIO Usage

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	Flash Media Activity LED	Indicates media activity. Media or USB cable must not be removed with LED lit. Active High.
GPIO2	H	Ready/Busy# 1/4	Ready/Busy# line from NAND Flash chips 0, or 0 & 4
GPIO3	H	V_BUS	USB V bus dectect
GPIO4	H	Ready/Busy# for Chips 1/5	Ready/Busy# line from NAND Flash chips 1, or 1 & 5
GPIO5	H	HS_IND/Ready/Busy# 2/6	In Rom -03; HS_LED output indicator; in later ROM patterns, the Ready/Busy# line from NAND Flash chips 2, or 2 & 6
GPIO6	H	A16	A16 address line when external Rom is used; unused output otherwise.
GPIO7	H	Ready/Busy# 3/7	Ready/Busy# line from NAND Flash chips 3, or 3 & 7

Chapter 12 Typical Application

Contact SMSC Sales for the latest reference designs and information and details about software licenses and the latest capabilities/features included in current production versions of the internal ROM.