REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add vendor CAGE 01295. Add case outlines L and 3. Change drawing CAGE code to 67268. Technical changes in 1.4, table I, and figure 3. Editorial changes throughout.	89-08-14	M. A. Frye
B	Make corrections to figure 4. Update boilerplate. Editorial changes throughout –jak.	00-10-25	Thomas M. Hess

FIRST PAGE OF THIS DRAWING HAS BEEN CHANGED.

CURRENT CAGE CODE 67268

REV																			
SHEET																			
REV	B																		
SHEET	15																		

REV STATUS OF SHEETS																
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Marcia B. Kelleher

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

CHECKED BY
Monica L. Poelking

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

APPROVED BY
Michael A. Frye

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL TRANSPARENT LATCH WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

DRAWING APPROVAL DATE
87-04-27

AMSC N/A

REVISION LEVEL
B

SIZE	CAGE CODE	
A	**14933**	**5962-87556**

SHEET
1 OF 15

DSCC FORM 2233
APR 97

5962-E249-00

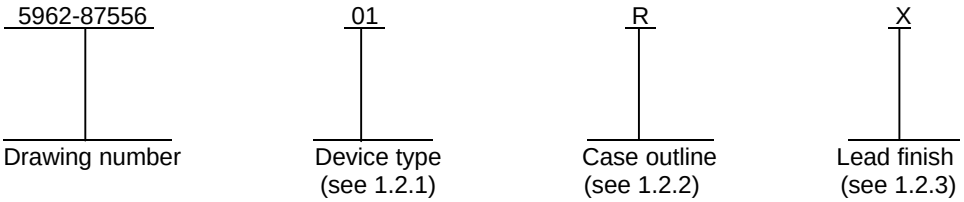
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

For device classes M and Q:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT373	Octal transparent latch with three-state outputs and TTL compatible inputs
02	54ACT11373	Octal transparent latch with three-state outputs and TTL compatible inputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Input clamp diode current (I_{IK})	±20 mA
Output clamp diode current (I_{OK})	±20 mA
DC output current (per pin)	±50 mA
DC V_{CC} or GND current	±100 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D) 2/	500 mW 3/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J) 3/	+175°C 4/

1.4 Recommended operating conditions. 2/, 5/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall times (V_{CC} = 4.5 V to 5.5 V)	0 to 8 ns/V
Minimum setup time, Dn to LE (t_s):	
T_C = +25°C, V_{CC} = 4.5 V	7.0 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	8.5 ns
Minimum hold time, Dn to LE (t_h):	
Device type 01, T_C = +25°C, V_{CC} = 4.5 V	0.0 ns
Device type 01, T_C = -55°C to +125°C, V_{CC} = 4.5 V	1.0 ns
Device type 02, T_C = +25°C, V_{CC} = 4.5 V	3.5 ns
Device type 02, T_C = -55°C to +125°C, V_{CC} = 4.5 V	3.5 ns
Minimum pulse width, LE (t_w):	
T_C = +25°C, V_{CC} = 4.5 V	7.0 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V	8.5 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability..
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ For T_C = 100°C to +125°C, derate linearly at 12 mW/°C.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ Unless otherwise specified, the values listed apply over the full V_{CC} recommended operating range.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Table I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	V_{CC}	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH} 1/	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -50\ \mu A$	All	4.5 V	1, 2, 3	4.4		V
			All	5.5 V		5.4		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -24$ mA	All	4.5 V		3.7		
			All	5.5 V		4.7		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OH} = -50$ mA	All	5.5 V		3.85		
Low level output voltage	V_{OL} 1/	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = 50\ \mu A$	All	4.5 V	1, 2, 3		0.10	V
				5.5 V			0.10	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = 24$ mA	All	4.5 V			0.50	
				5.5 V			0.50	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $I_{OL} = 50$ mA	All	5.5 V			1.65	
High level input voltage	V_{IH} 2/		All	4.5 V	1, 2, 3	2.0		V
				5.5 V	1, 2, 3	2.0		
Low level input voltage	V_{IL} 2/		All	4.5 V	1, 2, 3		0.8	V
				5.5 V	1, 2, 3		0.8	
Input leakage current low	I_{IL}	$V_{IN} = 0.0$ V	All	5.5 V	1, 2, 3		-1.0	µA
Input leakage current high	I_{IH}	$V_{IN} = 5.5$ V	All	5.5 V	1, 2, 3		1.0	
Quiescent supply current	I_{CCH}	$V_{IN} = V_{CC}$ or GND	All	5.5 V	1, 2, 3		160	µA
	I_{CCL}		All	5.5 V			160	
	I_{CCZ}		All	5.5 V			160	

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits		Unit
						Min	Max	
Maximum I_{CC}/input current, TTL inputs high	ΔI_{CC}	V_{IN} = 3.4 V All other inputs = V_{CC} or GND	All	5.5 V	1, 2, 3		1.6	mA
Three state output leakage current high	I_{OZH}	$V_{IN} = V_{IH}$ min or V_{IL} max, $V_{OUT} = V_{CC}$ or GND	All	5.5 V	1, 2, 3		+10.0	µA
Three state output leakage current low	I_{OZL}		All	5.5 V	1, 2, 3		-10.0	µA
Input capacitance	C_{IN}	See 4.3.1c T_C = +25°C	01		4		8.0	pF
			02				10.0	
Power dissipation capacitance	C_{PD} 3/	See 4.3.1c	01		4		75	pF
		Outputs enabled, See 4.3.1c	02				82	
		Outputs disabled, See 4.3.1c					68	
Functional tests		Tested at V_{CC} = 4.5 V and Repeated at V_{CC} = 5.5 V See 4.3.1d	All	4.5 V	7, 8	L	H	
				5.5 V				
Propagation delay time, Dn to Qn	t_{PHL1}, t_{PLH1} 4/	C_L = 50 pF minimum R_L = 500Ω See figure 4	01	4.5 V	9	1.0	10.5	ns
					10, 11	1.0	12.5	
			02		9	1.0	10.5	
					10, 11	1.0	12.7	
Propagation delay time, LE to Qn	t_{PHL2} 4/	C_L = 50 pF minimum R_L = 500Ω See figure 4	01	4.5 V	9	1.0	10.0	ns
					10, 11	1.0	11.5	
			02		9	1.0	10.9	
					10, 11	1.0	13.0	
	t_{PLH2} 4/		01	4.5 V	9	1.0	10.5	ns
					10, 11	1.0	12.5	
			02		9	1.0	11.3	
					10, 11	1.0	14.1	

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits		Unit
						Min	Max	
Propagation delay Output disable time, $\overline{OE}$ to Qn	t_{PHZ} 4/	C_L = 50 pF minimum R_L = 500Ω See figure 4	01	4.5 V	9	1.0	11.0	ns
					10, 11	1.0	14.0	
			02		9	1.0	12.1	
					10, 11	1.0	14.0	
	t_{PLZ} 4/		01	4.5 V	9	1.0	9.0	ns
					10, 11	1.0	11.0	
			02		9	1.0	9.5	
					10, 11	1.0	11.0	
Propagation delay time, output enable $\overline{OE}$ to Qn	t_{PZH} 4/	C_L = 50 pF minimum R_L = 500Ω See figure 4	01	4.5 V	9	1.0	9.5	ns
					10, 11	1.0	11.5	
			02		9	1.0	10.7	
					10, 11	1.0	13.6	
	t_{PZL} 4/		01	4.5 V	9	1.0	9.0	ns
					10, 11	1.0	11.0	
			02		9	1.0	10.9	
					10, 11	1.0	12.9	

1/ V_{OH} and V_{OL} tests will be tested at V_{CC} = 4.5 V. V_{CC} = 5.5 V tests are guaranteed, if not tested. Limits shown apply to operation at V_{CC} = 5.0 V ± 0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

2/ The V_{IH} and V_{IL} tests are not required and shall be applied as forcing functions for the V_{OH} and V_{OL} tests.

3/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and dynamic current consumption (I_S). Where:

$P_D = (C_{PD} + C_L)\ (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L)\ V_{CC}f + I_{CC}$

f is the frequency of the input signal and C_L is the external output load capacitance.

4/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum AC limits are guaranteed for V_{CC} = 5.5 V by guardbanding V_{CC} = 4.5 V limits to 1.5 ns (minimum).

Device type	01	02	
Case outlines	R, S, and 2	L	3
Terminal number	Terminal symbol		
1	$\overline{OE}$	Q0	NC
2	Q0	Q1	V_{CC}
3	D0	Q2	D3
4	D1	Q3	D2
5	Q1	GND	D1
6	Q2	GND	D0
7	D2	GND	$\overline{OE}$
8	D3	GND	NC
9	Q3	Q4	Q0
10	GND	Q5	Q1
11	LE	Q6	Q2
12	Q4	Q7	Q3
13	D4	LE	GND
14	D5	D7	GND
15	Q5	D6	NC
16	Q6	D5	GND
17	D6	D4	GND
18	D7	V_{CC}	Q4
19	Q7	V_{CC}	Q5
20	V_{CC}	D3	Q6
21	---	D2	Q7
22	---	D1	NC
23	---	D0	LE
24	---	$\overline{OE}$	D7
25	---	---	D6
26	---	---	D5
27	---	---	D4
28	---	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Device types 01 and 02

Inputs			Outputs
LE	$\overline{OE}$	Dn	Qn
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	Q_0

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance
Q_0 = Output prior to last High to Low transition of LE

FIGURE 2. Truth table.

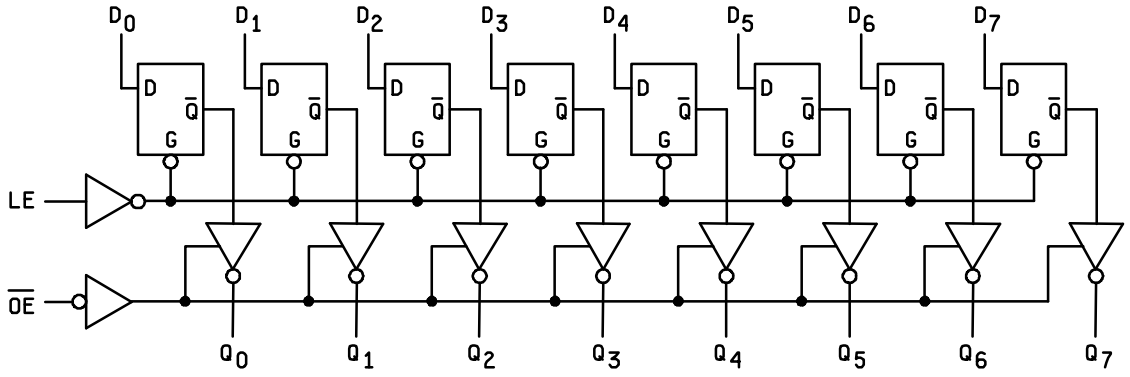


FIGURE 3. Logic diagram.

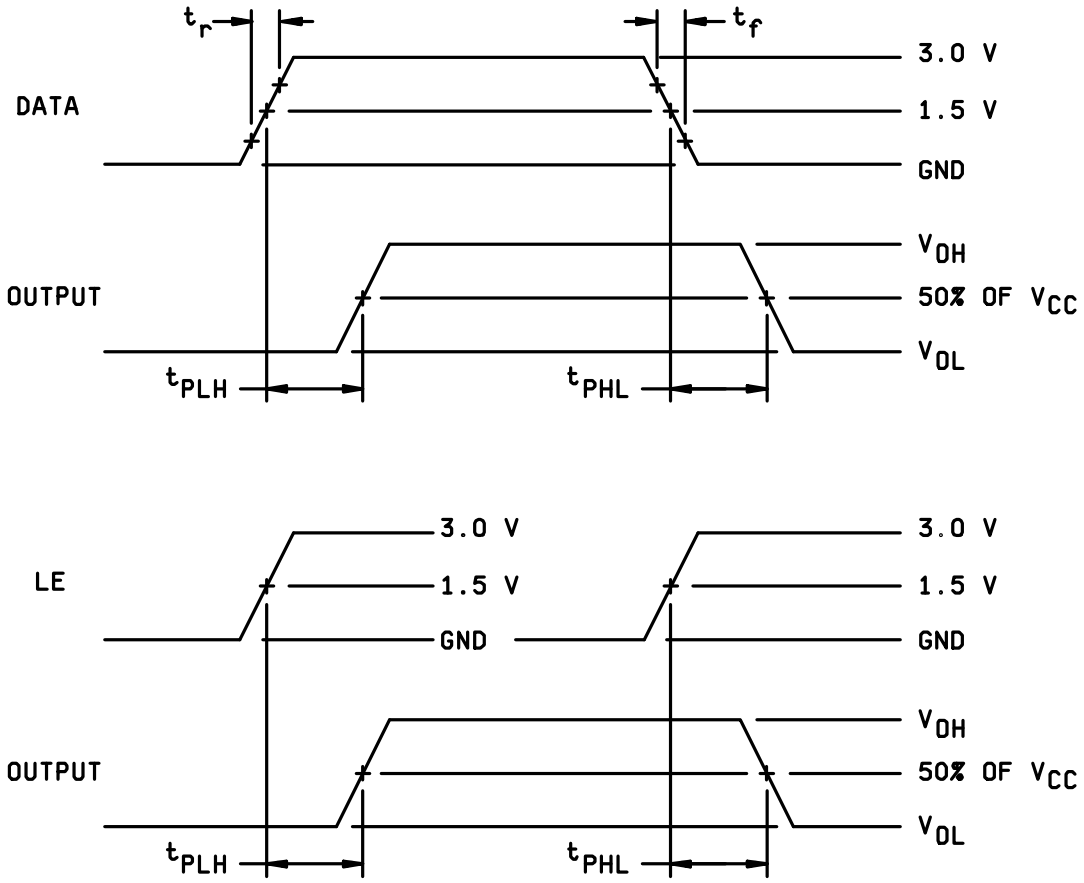


FIGURE 4. Switching waveforms and test circuit.

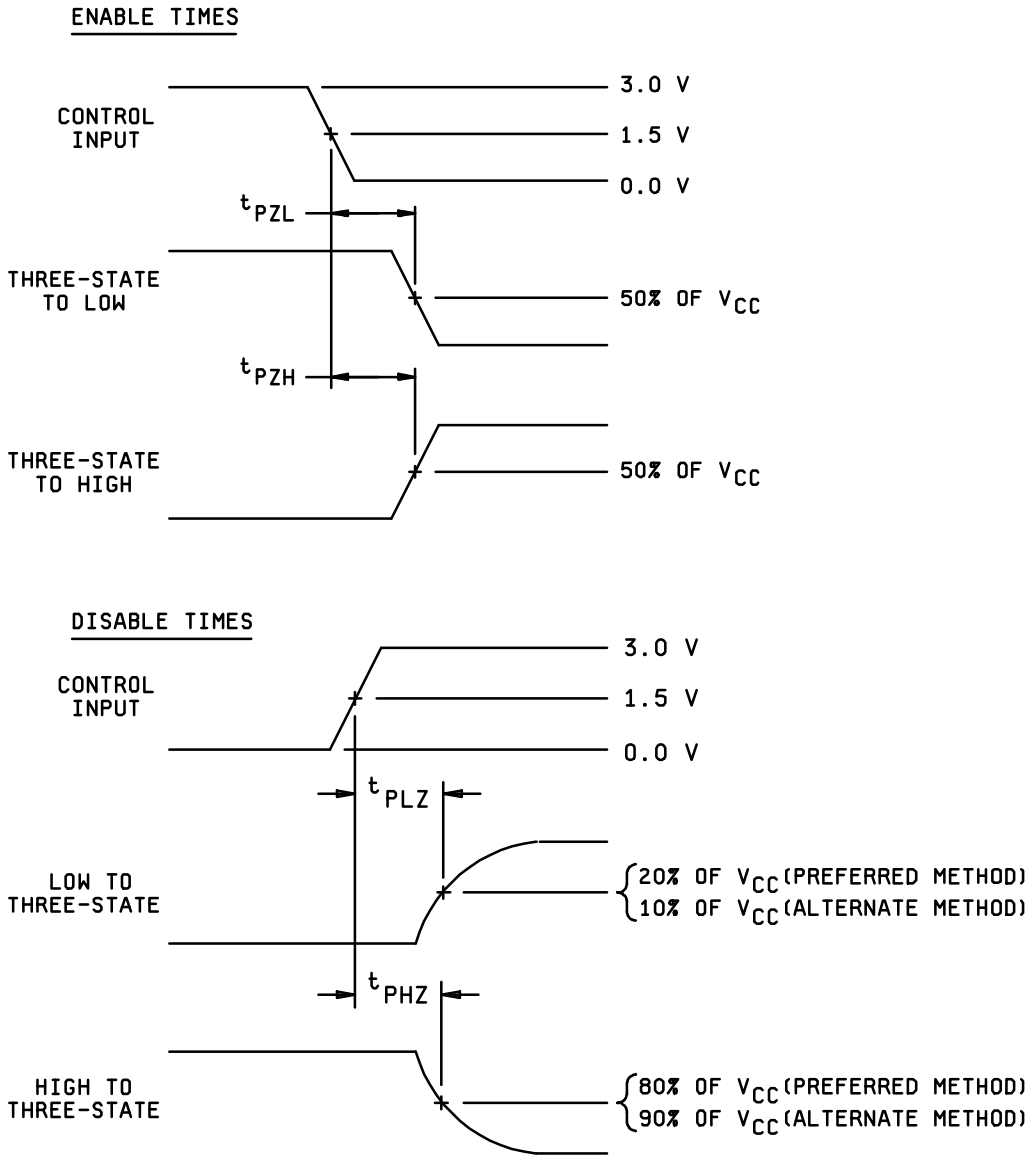
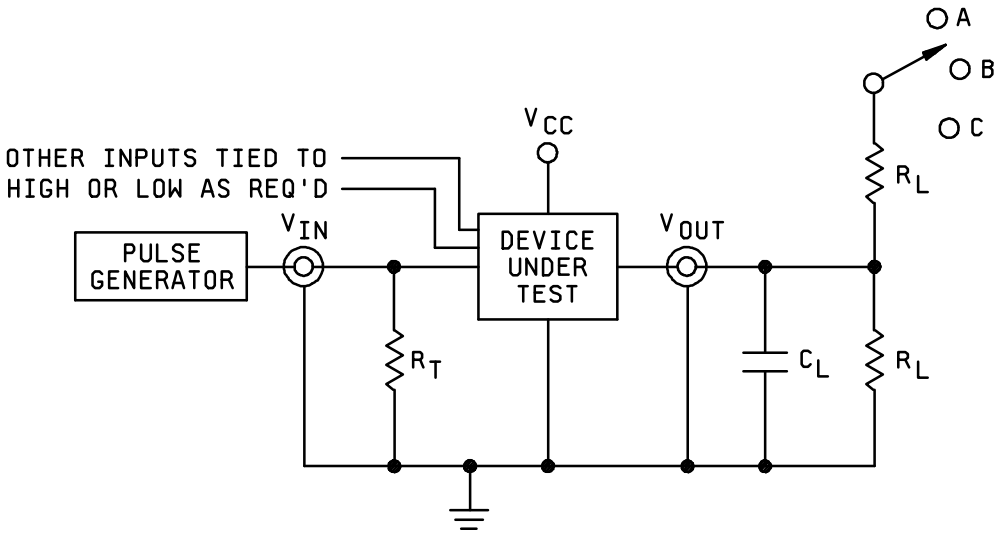


FIGURE 4. Switching waveforms and test circuit – Continued.



NOTES:
1. Preferred method
   When measuring t_{PHZ} and t_{PZH}: A = GND
   When measuring t_{PLZ} and t_{PZL}: B = $2XV_{CC}$
   When measuring t_{PLH} and t_{PHL}: C = OPEN
2. Alternate method
   When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: A = OPEN
   When measuring t_{PLZ} and t_{PZL}: B = $2XV_{CC}$
   C = N/A
3. C_L = 50 pF or equivalent, (includes probe and jig capacitance).
4. $R_T = 50\Omega$, $R_L = 500\Omega$ or equivalent.
5. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; $Z_O = 50\Omega$; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns; t_r. duty cycle = 50 percent.
6. Timing parameters shall be tested at a minimum input frequency of 1MHz.

FIGURE 4. Switching waveforms and test circuit – Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, and D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1, 2, 3, 7, 8, 9 1/
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11 2/
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ PDA applies to subgroup 1.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0674.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 00-10-25

Approved sources of supply for SMD 5962-87556 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8755601RA	27014 01295	54ACT373DMQB SNJ54ACT373J
5962-8755601SA	27014 01295	54ACT373FMQB SNJ54ACT373W
5962-87556012A	27014 01295	54ACT373LMQB SNJ54ACT373FK
5962-8755602LA	3/	SNJ54ACT11373JT
5962-87556023A	3/	SNJ54ACT11373FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090 Point of contact: 5 Foden Road South Portland, ME 04106
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: 6412 Highway 75 South Sherman, TX 75090-0084

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