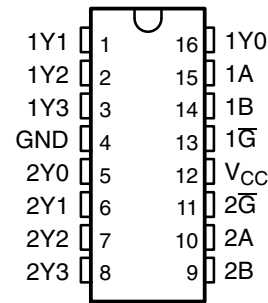


# 74AC11139 DUAL 2-LINE DECODER/DEMULTIPLEXER

SCAS070B – JULY 1989 – REVISED APRIL 1996

- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates Two Enable Inputs to Simplify Cascading and/or Data Reception
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (D) and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic 300-mil DIPs (N)

D, N, OR PW PACKAGE  
(TOP VIEW)



## description

The 74AC11139 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The 74AC11139 is composed of two individual 2-line to 4-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. This decoder/demultiplexer features fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The 74AC11139 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

| ENABLE INPUT<br>$\bar{G}$ | SELECT INPUTS |   | OUTPUTS |    |    |    |
|---------------------------|---------------|---|---------|----|----|----|
|                           | A             | B | Y0      | Y1 | Y2 | Y3 |
| H                         | X             | X | H       | H  | H  | H  |
| L                         | L             | L | L       | H  | H  | H  |
| L                         | H             | L | H       | L  | H  | H  |
| L                         | L             | H | H       | H  | L  | H  |
| L                         | H             | H | H       | H  | H  | L  |



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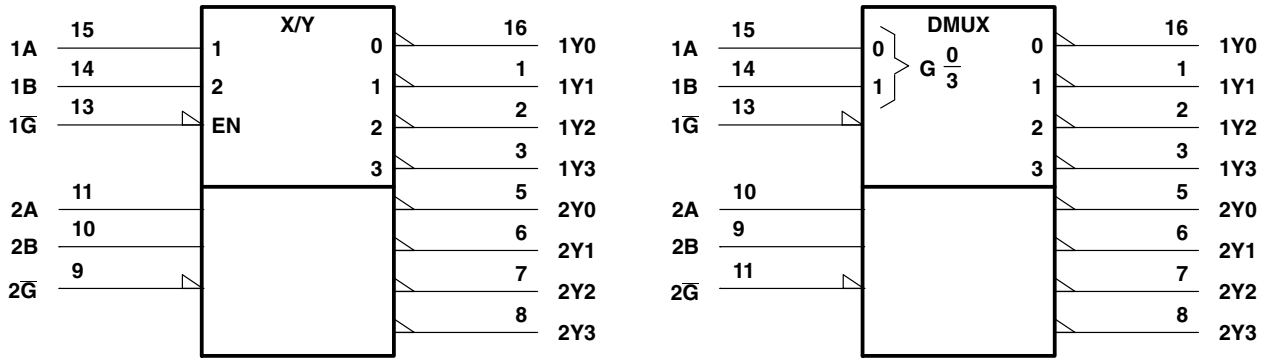
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# 74AC11139 DUAL 2-LINE DECODER/DEMULTIPLEXER

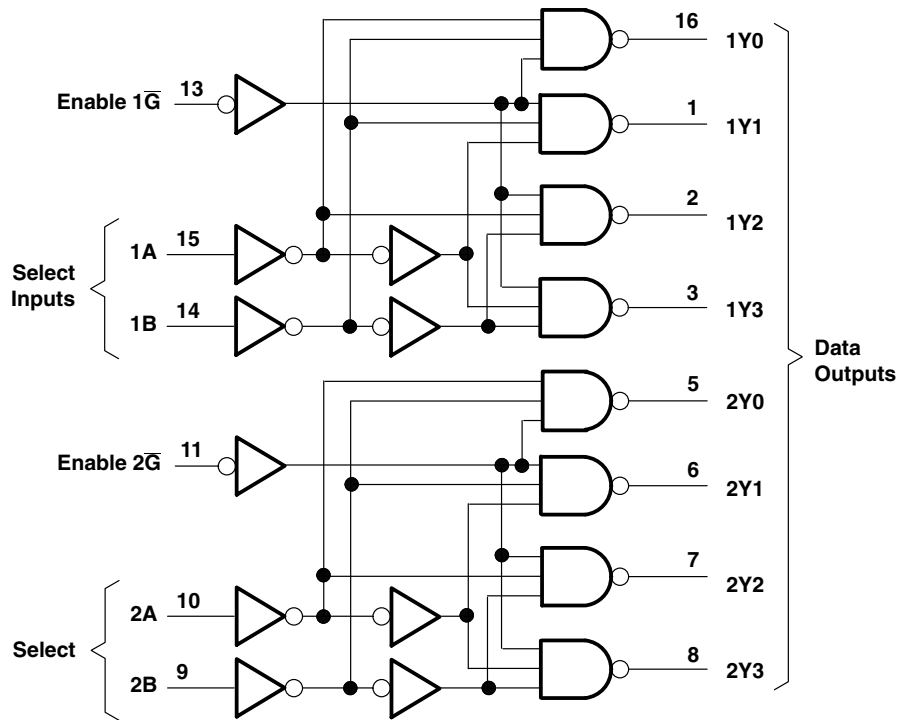
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## logic symbols (alternatives)†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# 74AC11139 DUAL 2-LINE DECODER/DEMULTIPLEXER

SCAS070B – JULY 1989 – REVISED APRIL 1996

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                            |
|--|----------------------------|
| Supply voltage range, $V_{CC}$ .....   | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1) .....                                      | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, $V_O$ (see Note 1) .....                                     | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....                | ±20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....               | ±50 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....                   | ±50 mA                     |
| Continuous current through $V_{CC}$ or GND .....                                   | ±200 mA                    |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): |                            |
| D package .....  | 1.3 W                      |
| N package .....  | 1.1 W                      |
| PW package .....   | 0.5 W                      |
| Storage temperature range, $T_{stg}$ .....   | –65°C to 150°C             |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## recommended operating conditions

|                     |                                    | MIN              | NOM  | MAX      | UNIT |
|---------------------|------------------------------------|------------------|------|----------|------|
| $V_{CC}$            | Supply voltage                     | 3                | 5    | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 3$ V   | 2.1  |          | V    |
|                     |                                    | $V_{CC} = 4.5$ V | 3.15 |          |      |
|                     |                                    | $V_{CC} = 5.5$ V | 3.85 |          |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 3$ V   |      | 0.9      | V    |
|                     |                                    | $V_{CC} = 4.5$ V |      | 1.35     |      |
|                     |                                    | $V_{CC} = 5.5$ V |      | 1.65     |      |
| $V_I$               | Input voltage                      | 0                |      | $V_{CC}$ | V    |
| $V_O$               | Output voltage                     | 0                |      | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 3$ V   |      | –4       | mA   |
|                     |                                    | $V_{CC} = 4.5$ V |      | –24      |      |
|                     |                                    | $V_{CC} = 5.5$ V |      | –24      |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 3$ V   |      | 12       | mA   |
|                     |                                    | $V_{CC} = 4.5$ V |      | 24       |      |
|                     |                                    | $V_{CC} = 5.5$ V |      | 24       |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0                |      | 10       | ns/V |
| $T_A$               | Operating free-air temperature     | –40              |      | 85       | °C   |



# 74AC11139 DUAL 2-LINE DECODER/DEMULTIPLEXER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS   | V <sub>CC</sub> | T <sub>A</sub> = 25°C                 |     |     | MIN  | MAX | UNIT |
|-----------------|---|-----------------|---------------------------------------|-----|-----|------|-----|------|
|                 |   |                 | MIN                                   | TYP | MAX |      |     |      |
| V <sub>OH</sub> | I <sub>OH</sub> = -50 μA                                    | 3 V             | 2.9                                   |     |     | 2.9  |     | V    |
|                 |   | 4.5 V           | 4.4                                   |     |     | 4.4  |     |      |
|                 |   | 5.5 V           | 5.4                                   |     |     | 5.4  |     |      |
|                 | I <sub>OH</sub> = -4 mA                                     | 3 V             | 2.58                                  |     |     | 2.48 |     |      |
|                 |   | 4.5 V           | 3.94                                  |     |     | 3.8  |     |      |
|                 |   | 5.5 V           | 4.94                                  |     |     | 4.8  |     |      |
|                 |   | 5.5 V           | I <sub>OH</sub> = -75 mA <sup>†</sup> |     |     | 3.85 |     |      |
| V <sub>OL</sub> | I <sub>OL</sub> = 50 μA                                     | 3 V             | 0.1                                   |     |     | 0.1  |     | V    |
|                 |   | 4.5 V           | 0.1                                   |     |     | 0.1  |     |      |
|                 |   | 5.5 V           | 0.1                                   |     |     | 0.1  |     |      |
|                 | I <sub>OL</sub> = 12 mA                                     | 3 V             | 0.36                                  |     |     | 0.44 |     |      |
|                 |   | 4.5 V           | 0.36                                  |     |     | 0.44 |     |      |
|                 | I <sub>OL</sub> = 24 mA                                     | 4.5 V           | 0.36                                  |     |     | 0.44 |     |      |
|                 |   | 5.5 V           | 0.36                                  |     |     | 0.44 |     |      |
| I <sub>I</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5.5 V           | ±0.1                                  |     |     | ±1   |     | μA   |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           | 8                                     |     |     | 80   |     | μA   |
| C <sub>i</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             | 3.5                                   |     |     |      |     | pF   |

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | T <sub>A</sub> = 25°C |     |     | MIN | MAX | UNIT |
|------------------|--------------|-------------|-----------------------|-----|-----|-----|-----|------|
|                  |              |             | MIN                   | TYP | MAX |     |     |      |
| t <sub>PLH</sub> | A or B       | Y           | 1.5                   | 5.3 | 8.1 | 1.5 | 9   | ns   |
| t <sub>PHL</sub> |              |             | 1.5                   | 6   | 8.4 | 1.5 | 9.4 |      |
| t <sub>PLH</sub> | G            | Y           | 1.5                   | 5.3 | 6.9 | 1.5 | 7.6 | ns   |
| t <sub>PHL</sub> |              |             | 1.5                   | 5.6 | 7.4 | 1.5 | 8.1 |      |

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

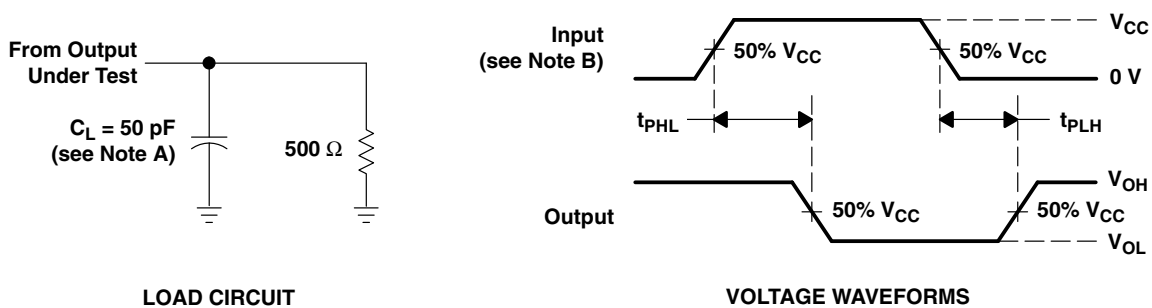
| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | T <sub>A</sub> = 25°C |     |     | MIN | MAX | UNIT |
|------------------|--------------|-------------|-----------------------|-----|-----|-----|-----|------|
|                  |              |             | MIN                   | TYP | MAX |     |     |      |
| t <sub>PLH</sub> | A or B       | Y           | 1.5                   | 3.5 | 6   | 1.5 | 6.6 | ns   |
| t <sub>PHL</sub> |              |             | 1.5                   | 4.1 | 6.3 | 1.5 | 6.9 |      |
| t <sub>PLH</sub> | G            | Y           | 1.5                   | 3.8 | 5.2 | 1.5 | 5.7 | ns   |
| t <sub>PHL</sub> |              |             | 1.5                   | 4   | 5.6 | 1.5 | 6.2 |      |

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

| PARAMETER  | TEST CONDITIONS                   | TYP | UNIT |
|--|-----------------------------------|-----|------|
| C <sub>pd</sub> Power dissipation capacitance per gate | C <sub>L</sub> = 50 pF, f = 1 MHz | 47  | pF   |



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> = 3 ns, t<sub>f</sub> = 3 ns.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| 74AC11139D       | OBSOLETE              | SOIC         | D               | 16   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| 74AC11139DR      | OBSOLETE              | SOIC         | D               | 16   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| 74AC11139N       | OBSOLETE              | PDIP         | N               | 16   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| 74AC11139PWLE    | OBSOLETE              | TSSOP        | PW              | 16   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |
| 74AC11139PWR     | OBSOLETE              | TSSOP        | PW              | 16   |             | TBD                     | Call TI              | Call TI                      | Samples Not Available       |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

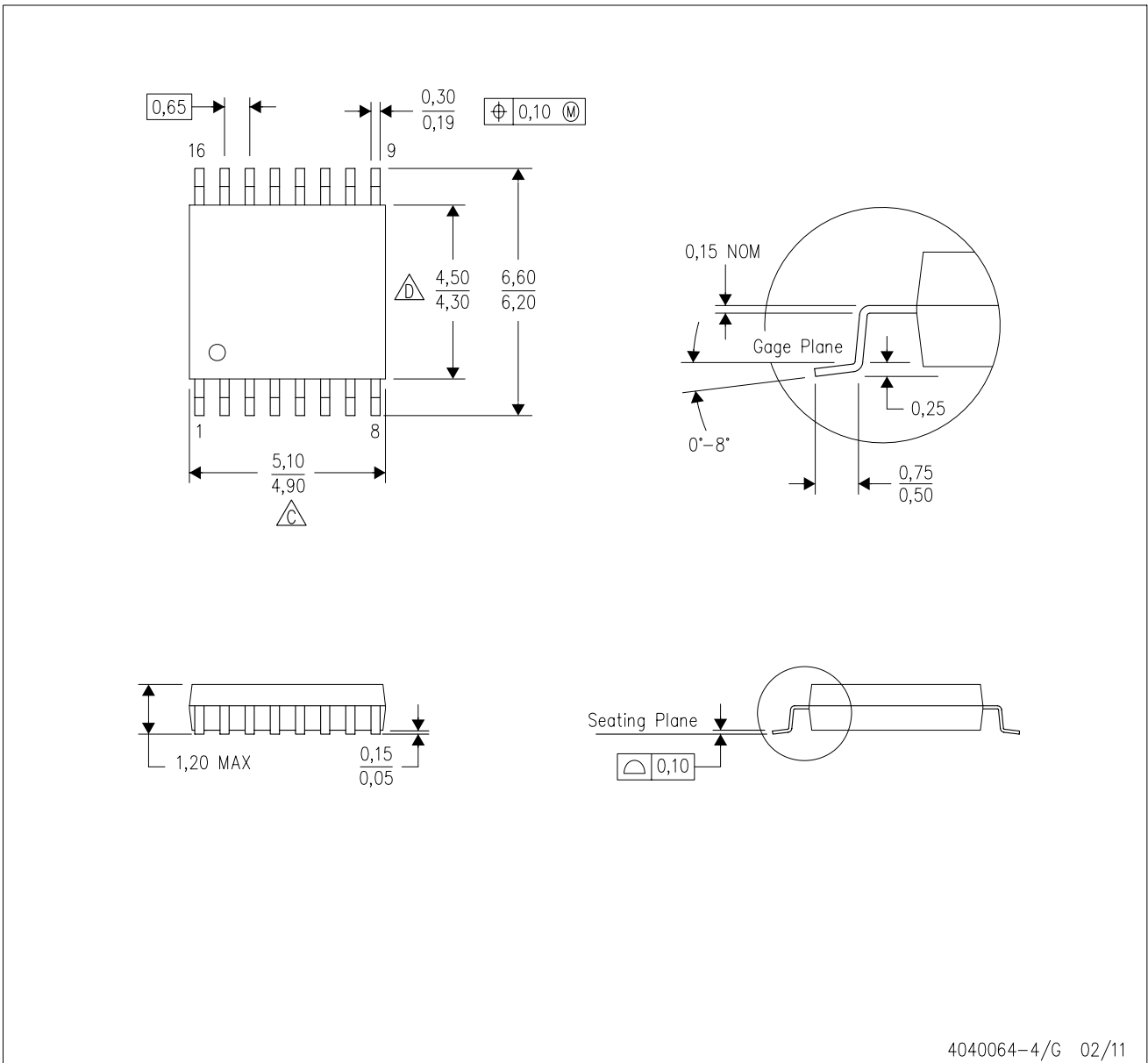


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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