B9948

3.3V, 160-MHz, 1:12 Clock Distribution Buffer

Features

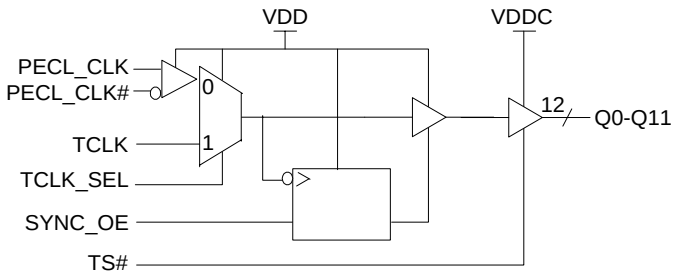
- **160-MHz clock support**
- **LVPECL or LVCMOS/LVTTL clock input**
- **LVCMOS/LVTTL compatible inputs**
- **12 clock outputs: drive up to 24 clock lines**
- **Synchronous Output Enable**
- **Output three-state control**
- **350-ps maximum output-to-output skew**
- **Pin compatible with MPC948**
- **Industrial temp. range: –40°C to +85°C**
- **32-pin TQFP package**

Description

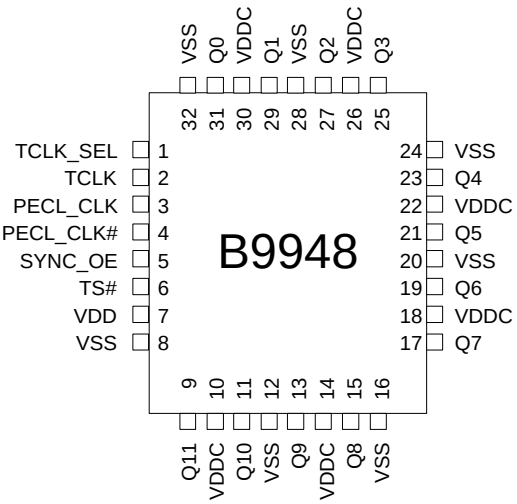
The B9948 is a low-voltage clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The twelve outputs are 3.3V LVCMOS or LVTTL compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9948 has an effective fan-out of 1:24. The outputs can also be three-stated via the three-state input TS#. Low output-to-output skews make the B9948 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The B9948 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

Block Diagram



Pin Configuration



Pin Description[[1]]

Pin	Name	PWR	I/O	Description
3	PECL_CLK		I, PU	PECL Input Clock
4	PECL_CLK#		I, PD	PECL Input Clock
2	TCLK		I, PU	External Reference/Test Clock Input
9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	Q(11:0)	VDDC	O	Clock Outputs
1	TCLK_SEL		I, PU	**Clock Select Input**. When LOW, PECL clock is selected and when HIGH TCLK is selected.
5	SYNC_OE		I, PU	**Output Enable Input**. When asserted HIGH, the outputs are enabled and when set LOW the outputs are disabled in a LOW state.
6	TS#		I, PU	**Three-state Control Input**. When asserted LOW, the output buffers are three-stated. When set HIGH, the output buffers are enabled.
10, 14, 18, 22, 26, 30	VDDC			3.3V Power Supply for Output Clock Buffers
7	VDD			3.3V Power Supply
8, 12, 16, 20, 24, 28, 32	VSS			Common Ground

Note:
1. PD = internal pull-down, PU = internal pull-up.

Output Enable/ Disable

The B9948 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC_OE is asserted LOW, the outputs are disabled in a LOW state. When SYNC_OE is set HIGH, the outputs are enabled as shown in *Figure 1*.

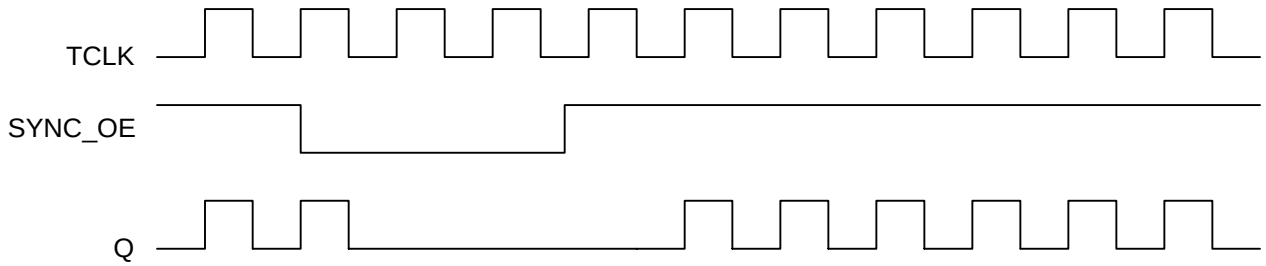


Figure 1. SYNC_OE Timing Diagram

Maximum Ratings[2]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: .....–65°C to + 150°C

Operating Temperature: .....-40°C to +85°C

Maximum ESD Protection..... 2 KV

Maximum Power Supply: 5.5V

Maximum Input Current:.....±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: V_{DDC} = 3.3V ±10%, V_{DD} = 3.3V ±10%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	PECL_CLK, Single Ended	1.49		1.825	V
		All other inputs	V_{SS}		0.8	
V_{IH}	Input High Voltage	PECL_CLK, Single Ended	2.135		2.42	V
		All other inputs	2.0		V_{DD}	
I_{IL}	Input Low Current (@V_{IL} = V_{SS})	Note [3]			–100	µA
I_{IH}	Input High Current (@V_{IL} =V_{DD})				100	µA
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK	Note [4]	300		1000	mV
V_{CMR}	Common Mode Range PECL_CLK		V_{DD} – 2.0		V_{DD} – 0.6	V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA, Note [5]			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –20 mA, V_{DDC} = 3.3V, Note [5]	2.5			V
I_{DD}	Quiescent Supply Current	All V_{DDC} and V_{DD}		1	2	mA
C_{in}	Input Capacitance				4	pF

Notes:

2. **Multiple Supplies**: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required
3. Inputs have pull-up resistors that effect input current, PECL_CLK# has a pull-down resistor.
4. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the V_{CMR} range and the input lies within the V_{PP} specification.
5. Driving series or parallel terminated 50Ω (or 50Ω to V_{DD}/2) transmission lines.

AC Parameters[[6]]**:** V_{DDC} = 3.3V ±10%, V_{DD} = 3.3V ±10%, T_A = –40°C to +85°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Maximum Input Frequency[[7]]		160			MHz
Tpd	PECL_CLK to Q Delay[[7]]		4.0		8.0	ns
	TCLK to Q Delay[[7]]		4.4		8.9	
FoutDC	Output Duty Cycle[[7],[8]]	Measured at V_{DDC}/2	TCYCLE/2 – 800		TCYCLE/2 + 800	ps
tpZL, tpZH	Output enable time (all outputs)		2		10	ns
tpLZ, tpHZ	Output disable time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew[[7],[9]]				350	ps
Tskew (pp)	Part-to-Part Skew[[10]]	PECL_CLK to Q			1.5	ns
		TCLK to Q			2.0	
Ts	Set-up Time[[7],[11]]	SYNC_OE to PECL_CLK	1.0			ns
		SYNC_OE to TCLK	0.0			
Th	Hold Time[[7],[11]]	PECL_CLK to SYNC_OE	0.0			ns
		TCLK to SYNC_OE	1.0			
Tr/Tf	Output Clocks Rise/Fall Time[[9]]	0.8V to 2.0V	0.2		1.0	ns

Notes:

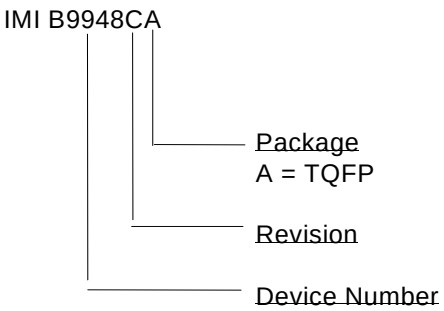
6. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
7. Outputs driving 50Ω transmission lines.
8. 50% input duty cycle.
9. Outputs loaded with 30 pF each.
10. Part-to-Part Skew at a given temperature and voltage.
11. Set-up and Hold times are relative to the falling edge of the input clock.

Ordering Information

Part Number	Package Type	Production Flow
IMIB9948CA	32-pin TQFP	Industrial, –40°C to +85°C
IMIB9948CAT	32-pin TQFP - Tape and Reel	Industrial, –40°C to +85°C

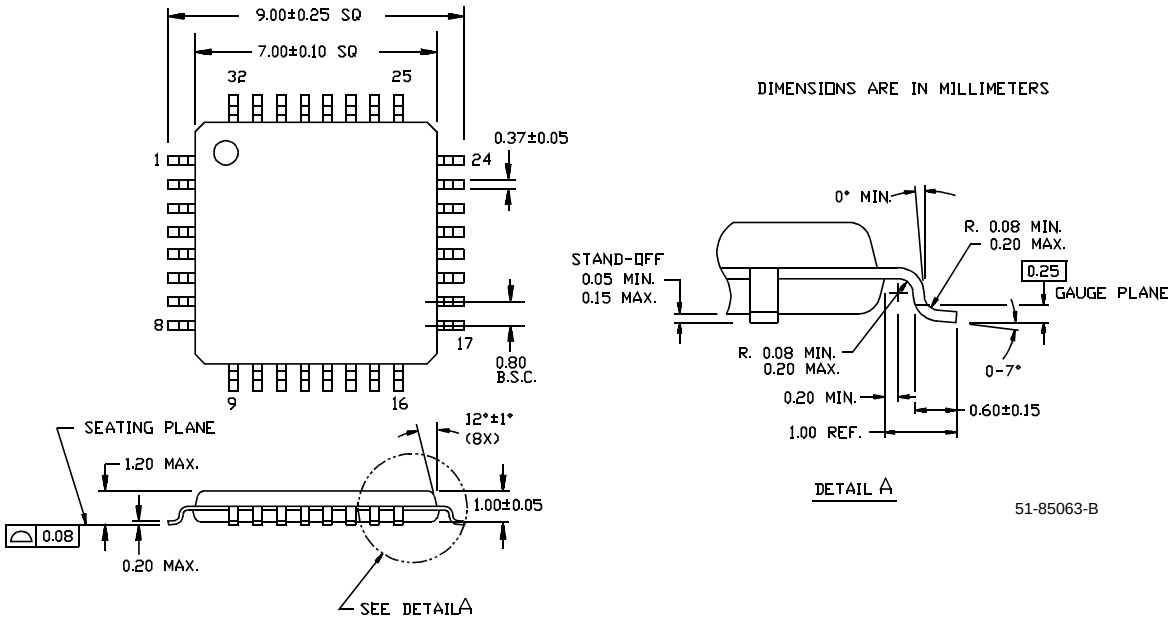
Note:The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
B9948CA
Date Code, Lot #



Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.0mm A32



Document History Page

Document Title: B9948 3.3V, 160 MHz, 1:12 Clock Distribution Buffer Document Number: 38-07079				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107115	06/06/01	IKA	Convert from IMI to Cypress
*A	108060	07/03/01	NDP	Changed Commercial to Industrial (See page 6)
*B	109805	01/31/02	DSG	Convert from Word to Frame (Cypress format)
*C	118058	09/16/02	RGL	Add a tape and reel option in the ordering information table. Change the package drawing and dimension to Cypress standard.
*D	122764	12/14/02	RBI	Add power up requirements to maximum ratings information