SN54ALS845, SN54AS845, SN54ALS846, SN54AS846
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

D2825, DECEMBER 1983—REVISED APRIL 1986

- 3-State Buffer-Type Outputs Drive Bus-Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Buffered Control Inputs to Reduce DC Loading
- Power-Up High-Impedance State
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The 'ALS845 and 'AS845 have noninverting data (D) inputs. The 'ALS846 and 'AS846 have inverting $\overline{D}$ inputs. Since $\overline{CLR}$ and $\overline{PRE}$ are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

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SN54ALS845, SN54AS845 . . . JT PACKAGE
SN74ALS845, SN74AS845 . . . DW OR NT PACKAGE
(TOP VIEW)

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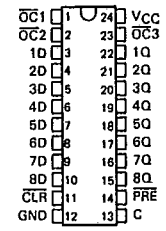
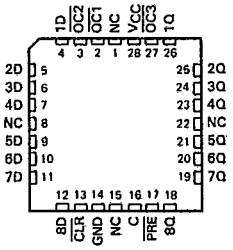
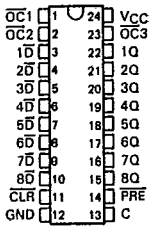


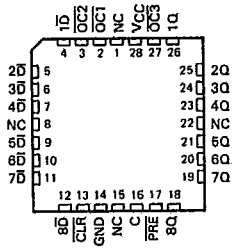
SN54ALS845, SN54AS845 . . . FK PACKAGE
SN74ALS845, SN74AS845 . . . FN PACKAGE
(TOP VIEW)



SN54ALS846, SN54AS846 . . . JT PACKAGE
SN74ALS846, SN74AS846 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS846, SN54AS846 . . . FK PACKAGE
SN74ALS846, SN74AS846 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

2

ALS and AS Circuits

SN54ALS845, SN54AS845, SN54ALS846, SN54AS846
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

The -1 versions of the SN74ALS845 and SN74ALS846 parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS845 and SN54ALS846.

The SN54ALS845, SN54AS845, SN54ALS846, and SN54AS846 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS845, SN74AS845, SN74ALS846, and SN74AS846 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'ALS845, 'AS845

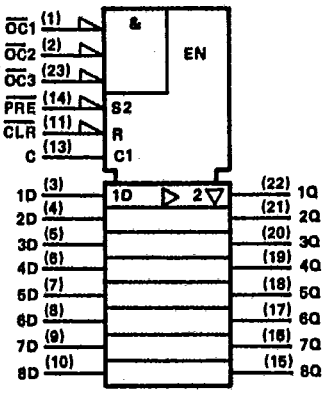
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

'ALS846, 'AS846

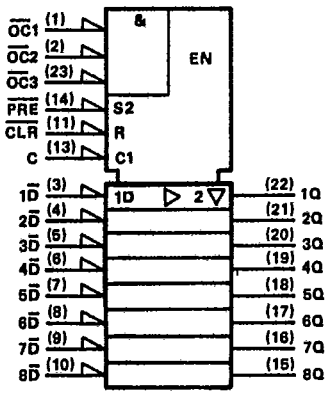
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	$\overline{D}$	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

logic symbols†

'ALS845, 'AS845



'ALS846, 'AS846



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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SN54ALS845, SN54AS845, SN54ALS846, SN54AS846
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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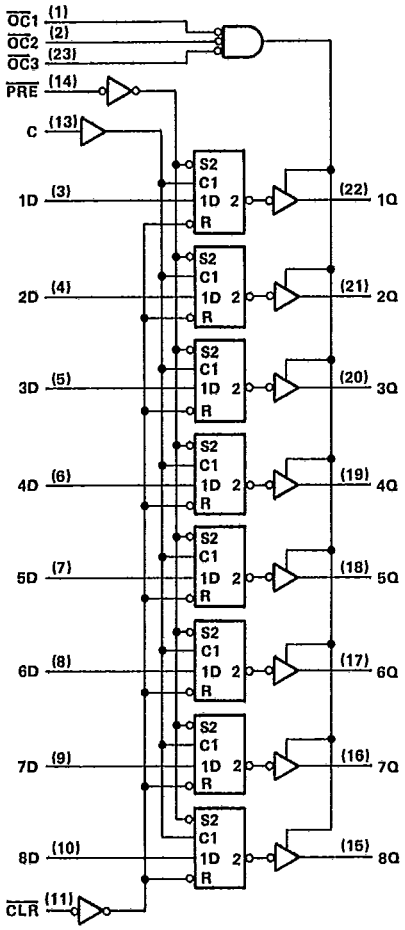
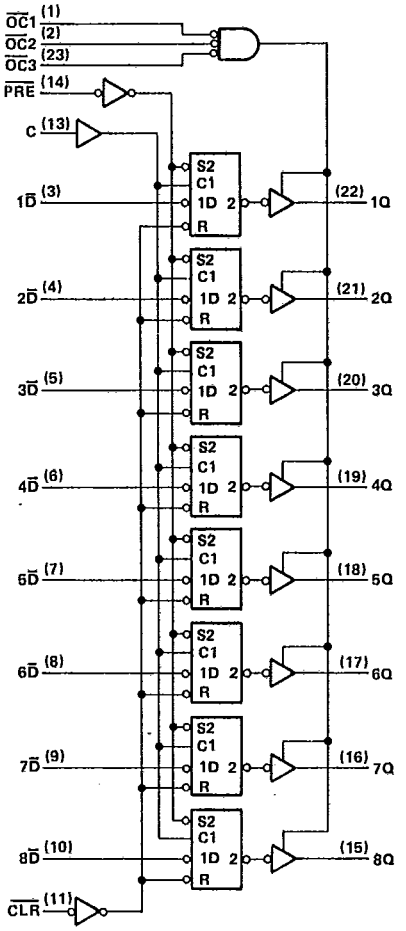
logic diagrams (positive logic)

'ALS845, 'AS845



'ALS846, 'AS846



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range:
SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 . . . . . −55°C to 125°C
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 . . . . . −0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

SN54ALS845, SN74ALS845
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

			SN54ALS845			SN74ALS845			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	40			35			ns
		C high	25			20			
t_{su}	Setup time, data before enable C↓		16			10			ns
t_h	Hold time, data after enable C↓		7			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS845-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS845			SN74ALS845			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		21	36		21	36	mA
		Outputs low		41	67		41	67	
		Outputs disabled		25	42		25	42	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS845			SN54ALS845		SN74ALS845		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		7	11	2	15	2	13	ns
t_{PHL}				11	15	4	20	4	18	
t_{PLH}	C	Q		12	18	5	25	5	21	ns
t_{PHL}				16	23	8	30	8	26	
t_{PLH}	$\overline{PRE}$	Q		13	19	5	25	6	22	ns
t_{PHL}				19	26	4	35	6	30	ns
t_{PLH}	$\overline{CLR}$	Q		19	26	4	35	6	30	ns
t_{PHL}				16	22	6	28	6	24	ns
t_{PZH}	$\overline{OC}$	Q		9	14	2	18	3	16	ns
t_{PZL}				12	17	4	20	5	18	
t_{PHZ}	$\overline{OC}$	Q		4	9	1	12	1	11	ns
t_{PLZ}				6	11	2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS846, SN74ALS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

recommended operating conditions

			SN54ALS846			SN74ALS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	40			35			ns
		C high	25			20			
t_{su}	Setup time, data before enable C↓		16			10			ns
t_h	Hold time, data after enable C↓		7			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

† The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V. The 48 mA limit applies for SN74ALS846-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS846			SN74ALS846			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
	V_{CC} = 4.5 V, (I_{OL} = 48 mA for -1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		22	36		22	36	mA
		Outputs low		43	72		43	72	
		Outputs disabled		28	48		28	48	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'ALS846			SN54ALS846		SN74ALS846		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q		11	16	4	22	4	20	ns
t_{PHL}				9	13	3	17	3	15	
t_{PLH}	C	Q		17	23	8	31	8	27	ns
t_{PHL}				14	19	6	26	6	22	
t_{PLH}	$\overline{PRE}$	Q		13	17	5	24	5	20	ns
t_{PHL}				18	24	9	36	9	26	
t_{PLH}	$\overline{CLR}$	Q		14	19	6	23	6	21	ns
t_{PHL}				16	21	9	25	9	23	
t_{PZH}	$\overline{OC}$	Q		10	13	3	17	3	15	ns
t_{PZL}				13	17	5	20	5	18	
t_{PHZ}	$\overline{OC}$	Q		7	10	1	12	1	11	ns
t_{PLZ}				7	11	2	14	2	12	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54AS845, SN54AS846
SN74AS845, SN74AS846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

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recommended operating conditions

			SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5			4			ns
		C high	5			4			
t_{su}	Setup time, data before enable C↓		3.5			2.5			ns
t_h	Hold time, data after enable C↓		3.5			2.5			ns
t_r	Recovery time	$\overline{PRE}$	17			15			ns
		$\overline{CLR}$	16			14			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS845	V_{CC} = 5.5 V	Outputs high		35	58		35	58	mA
			Outputs low		52	85		52	85	
			Outputs disabled		52	85		52	85	
	'AS846		Outputs high		36	59		36	59	
			Outputs low		53	87		53	87	
			Outputs disabled		53	87		53	87	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS845 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS845		SN74AS845		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14	2	13	ns
t_{PHL}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS846 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS846		SN74AS846		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	Q	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14.5	2	13.5	ns
t_{PHL}	$\overline{OC}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.