ANALOG DEVICES

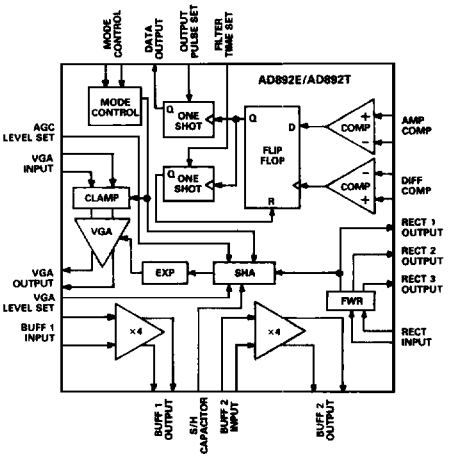
30 Mb/s Peak Detectors

AD892E/AD892T

FEATURES

- **30 Mb/s Data Transfer Rate Capability (AD892E)**
- **25 Mb/s Data Transfer Rate Capability (AD892T)**
- **1 ns (max) Additional Pulse Pairing**
- **Two Versions**
  - **Differential ECL Data Output (AD892E)**
  - **TTL Data Output (AD892T)**
- **Variable Gain Amplifier with 30 dB max Gain and 40 dB Control Range**
- **Two Gain of 4 RF Buffers with 200 Ω Differential-Load Drive Capability**
- **0.2 dB/ms Typical Gain Drift in Hold Mode**
- **1 µs AGC Attack/Decay Times Using a 1000 pF External Capacitor**
- **Dynamic Input Clamp Ensures Fast Recovery after Write to Read Transients**
- **Two Matched Offset Trimmed Comparators**
- **One-Shot Pulse Width Set Using External Resistor**
- **Operates from +5 V and +12 V Supplies**

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD892E/AD892T is a complete subsystem for recovering binary information from differentiating channels with transfer rates up to 30 megabits per second. It is connected to the output of the head amplifier and performs the signal conditioning and the data qualification task with a minimum of external components.

The AD892E/AD892T has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Fast acquisition and low droop while in the hold mode allows for the AGC operation to be performed within the sector header without compromising channel behavior when reading data. Two user-defined filter/equalizer stages may be employed, thus allowing maximum design flexibility. This greatly simplifies the design of the overall channel characteristics.

Three low offset, 50 MHz full-wave rectifiers are provided. One rectifier drives the internal sample-and-hold circuitry; this signal is available to the user to set the attack and decay characteristics of the sample and hold. The other two rectifier outputs are provided to generate the qualification level and to feed the single-ended passive differentiator. The threshold setting and differentiation is performed by an external RLC network.

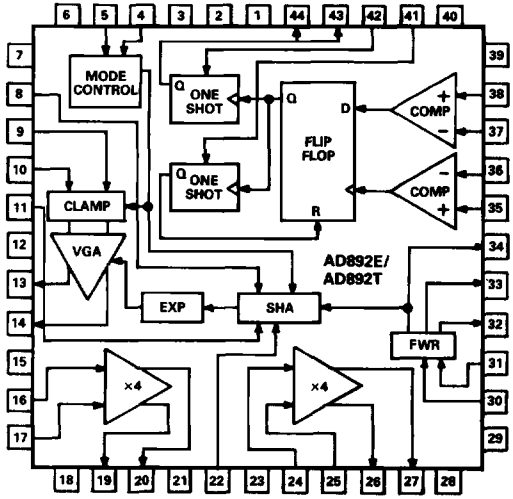
The AD892E/AD892T provides both level and time-domain qualification. Level qualification is performed on half cycles of the rectified data waveform using a user-defined threshold level which is applied to the level qualification comparator. The output of this comparator drives the data input of a master-slave flip-flop. A second, matched comparator detects zero-crossings and clocks the flip-flop. Each valid zero-crossing causes a time-domain filter one-shot to generate a pulse with a user-defined period. During the one-shot period the flip-flop is disabled, preventing the detection of additional zero-crossing events. This technique prevents single-bit errors from being propagated into two-bit errors. The zero-crossing event also triggers an output one-shot, again with a user defined pulse width. For maximum flexibility, the data output is a Schottky open-collector transistor with a separate digital ground to minimize digital feedthrough (AD892T) or differential ECL (AD892E).

The AD892E/AD892T is available in a 44-pin plastic leaded chip carrier (PLCC) and is specified to operate over the commercial (0 to +70°C) temperature range.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

PIN ASSIGNENTS

Pin	Description
1	+5 V Supply
2	No Connection (Can Be Left Floating)
3	No Connection (Can Be Left Floating)
4	Mode Control Bit B (TTL Compatible)
5	Mode Control Bit A (TTL Compatible)
6	Digital Ground
7	No Connection (Can Be Left Floating)
8	"AGC Level Set" Input Voltage
9	Variable Gain Amplifier Input (+)
10	Variable Gain Amplifier Input (−)
11	"VGA Level Set" Input Voltage
12	No Connection (Can Be Left Floating)
13	Variable Gain Amplifier Output (−)
14	Variable Gain Amplifier Output (+)
15	No Connection (Can Be Left Floating)
16	#1 12.75 dB Buffer Input (−)
17	#1 12.75 dB Buffer Input (+)
18	+12 V Supply (Analog)
19	#1 12.75 dB Buffer Output (+)
20	#1 12.75 dB Buffer Output (−)
21	No Connection (Can Be Left Floating)
22	Sample-and-Hold Capacitor
23	No Connection (Can Be Left Floating)
24	#2 12.75 dB Buffer Input (−)
25	#2 12.75 dB Buffer Input (+)
26	#2 12.75 dB Buffer Output (+)
27	#2 12.75 dB Buffer Output (−)
28	Analog Ground
29	No Connection (Can Be Left Floating)
30	Full Wave Rectifier Input (+)
31	Full Wave Rectifier Input (−)
32	Rectified Signal to Derive Threshold
33	Rectified Signal for Differentiator
34	Rectified Signal to S/H; AGC Attack and Decay Is Programmed at This Point
35	Zero Crossing Comparator Input (+)
36	Zero Crossing Comparator Input (−)
37	Minimum Threshold Level Input
38	Signal Amplitude Comparator Input
39	Internal Voltage Reference
40	+12 V Supply (Digital)
41	Apply Resistor to Program Time Domain Filter Pulse Width
42	Apply Resistor to Program Output Pulse Width
43	Data Output (Open Collector AD892T) Data Output (+ ECL AD892E)
44	Data Output Ground (Emitter of Output Device AD892T) Data Output (− ECL AD892E)



ORDERING GUIDE

Model No.	Package Description	Package Option*
AD892EJP	44-Pin PLCC	P-44A
AD892TJP	44-Pin PLCC	P-44A

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.