

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Octal Transparent Latch with 3-State Outputs; **Octal D-Type Flip-Flop** with 3-State Output

The SN74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

The SN74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all ON Semiconductor TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Тур	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current – High	, O		-2.6	mA
l _{OL}	Output Current – Low		O.V	24	mA



ON Semiconductor

http://onsemi.com

LOW **POWER** SCHOTTKY

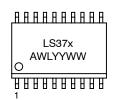
MARKING DIAGRAMS



SN74LS37xN **AWLYYWW**

PDIP-20 N SUFFIX **CASE 738**





SOIC-20 **DW SUFFIX CASE 751D**



74LS37x **AWLYWW**

= 3 or 4

CASE 967

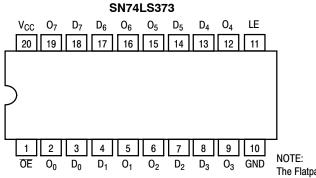
= Assembly Location

WL = Wafer Lot YY = Year WW = Work Week

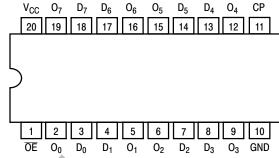
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

CONNECTION DIAGRAM DIP (TOP VIEW)



SN74LS374



The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
65 U.L.	15 U.L.

PIN NAMES

 $D_0 - D_7$ Data Inputs Latch Enable (Active HIGH) Input LE Clock (Active HIGH Going Edge) Input CP ŌΕ Output Enable (Active LOW) Input $O_0 - O_7$ Outputs

NOTES:

a) 1 TTL Unit Load (U.L.) = $40 \mu A HIGH/1.6 mA LOW$.

LS373

D _n	LE	OE	On
Н	Н	٦	Н
L	Н	Ŧ	
Х	_	Ţ	Q_0
X	X	Н	Z*

H = HIGH Voltage Level

L = LOW Voltage Level

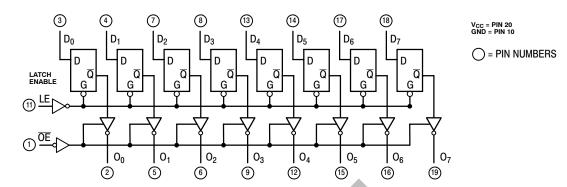
X = Immaterial

the Dual In-Line Package.					
	LOADIN	G (No	te a)		
	HIGH	ı	_OW		P
ta Inputs	0.5 U.L.	0.2	25 U.L.	~	O'
ch Enable (Active HIGH) Input	0.5 U.L.	0.2	25 U.L.	\cdot \cdot \cdot \cdot	
ck (Active HIGH Going Edge) Input	0.5 U.L.	0.2	25 U.L.		
tput Enable (Active LOW) Input	0.5 U.L.	0.5	25 U.L.		7
tputs	65 U.L.	1	5 U.L.		
ad (U.L.) = 40 μA HIGH/1.6 mA LOW.			2. (
λα (σ.Ε.) – 40 μΑ ΤΙΙΟΠ) 1.0 ΠΙΑ Έσνι.					
TRUTH TABLE	20 1	13.			
IRUIN IABLE	V C	/ . (LS37	4	
On	7	D _n	LE	OE	On
H		H	4	L	Н
10,711	·.O1	L	4	L	L
Q_0		X	Х	Н	Z*
Z*				•	
الم م دالا					
(,, (,, (,, ,, ,, ,, ,, ,, ,, ,, ,, ,, ,					
77 77					
ected by the state of the Output Enable	input (OE).				
0 03					

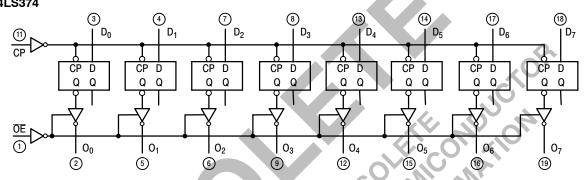
 $Z = \mbox{High Impedance}$ * Note: Contents of flip-flops unaffected by the state of the Output Enable input (\$\overline{OE}\$).

LOGIC DIAGRAMS

SN74LS373



SN74LS374



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

			Limits	~ O	7/3	.00	
Symbol	Parameter	Min	Тур	Max	Unit	Tes	t Conditions
V _{IH}	Input HIGH Voltage	2.0		JA	Y	Guaranteed Input All Inputs	t HIGH Voltage for
V _{IL}	Input LOW Voltage		7	0.8	V	Guaranteed Input All Inputs	t LOW Voltage for
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} =$	–18 mA
V _{OH}	Output HIGH Voltage	2.4	3.1		V	V_{CC} = MIN, I_{OH} = or V_{IL} per Truth T	
.,	0.1.11000000		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN,
V _{OL}	Output LOW Voltage	4,5	0.35	0.5	V	I _{OL} = 24 mA	$V_{IN} = V_{IL}$ or V_{IH} per Truth Table
I _{OZH}	Output Off Current HIGH			20	μΑ	V _{CC} = MAX, V _{OU}	_T = 2.7 V
I _{OZL}	Output Off Current LOW			-20	μΑ	V _{CC} = MAX, V _{OU}	T = 0.4 V
Luc	Input HIGH Current			20	μΑ	$V_{CC} = MAX, V_{IN}$	= 2.7 V
I _{IH}	input i liai i cuitett			0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN}	= 0.4 V
Ios	Short Circuit Current (Note 1)	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			40	mA	$V_{CC} = MAX$	

^{1.} Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$)

			Limits						
			LS373		LS374				
Symbol	Parameter	Min	Тур	Max	Min	Тур	Max	Unit	Test Conditions
f _{MAX}	Maximum Clock Frequency				35	50		MHz	
t _{PLH} t _{PHL}	Propagation Delay, Data to Output		12 12	18 18				ns	C 45 pF
t _{PLH} t _{PHL}	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	C_L = 45 pF, R_L = 667 Ω
t _{PZH} t _{PZL}	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t _{PHZ}	Output Disable Time		12 15	20 25		12 15	20 25	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS ($T_A = 25$ °C, $V_{CC} = 5.0 \text{ V}$)

		Limits		0			
			LS	373	LS	374	
Symbol	Parameter		Min	Max	Min	Max	Unit
t _W	Clock Pulse Width		15		15	,	ns
t _s	Setup Time		5.0	14	20	77	ns
t _h	Hold Time		20		0	7	ns

DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

SN74LS373

AC WAVEFORMS

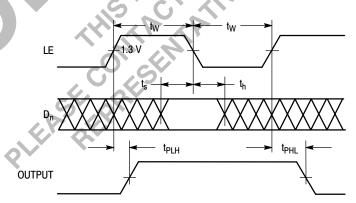


Figure 1.

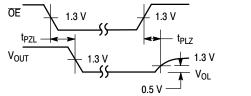


Figure 2.

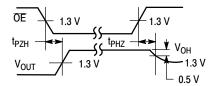
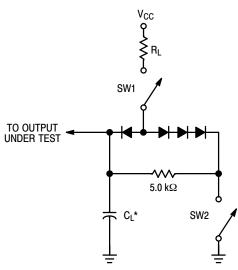


Figure 3.

SN74LS373

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t _{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

Figure 4.

AC WAVEFORMS

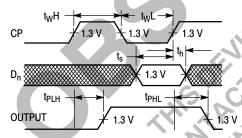


Figure 5.

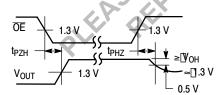


Figure 7.

SN74LS374

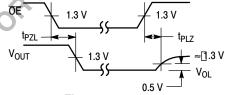
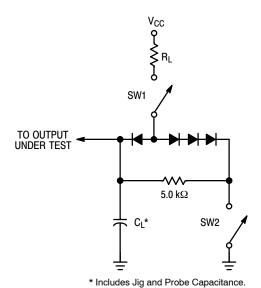


Figure 6.

SN74LS374

AC LOAD CIRCUIT



SWITCH POSITIONS

SYMBOL	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

Figure 8.

DEVICE ORDERING INFORMATION

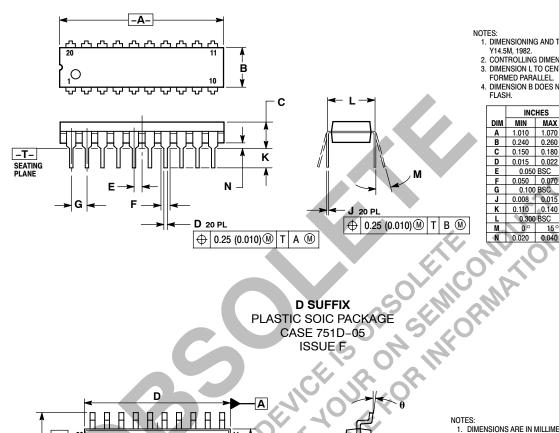
Device Order Number	Package Type	Tape and Reel Size
SN74LS373N	PDIP-20	1440 Units/Box
SN74LS373DW	SOIC-WIDE	38 Units/Rail
SN74LS373DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS373M	SOEIAJ-20	See Note 2
SN74LS373MEL	SOEIAJ-20	See Note 2
SN74LS374N	PDIP-20	1440 Units/Box
SN74LS374DW	SOIC-WIDE	38 Units/Rail
SN74LS374DWR2	SOIC-WIDE	2500/Tape and Reel
SN74LS374M	SOEIAJ-20	See Note 2
SN74LS374MEL	SOEIAJ-20	See Note 2

^{2.} For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

PACKAGE DIMENSIONS

N SUFFIX

PLASTIC PACKAGE CASE 738-03 **ISSUE E**



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- Y14.5M, 1982.

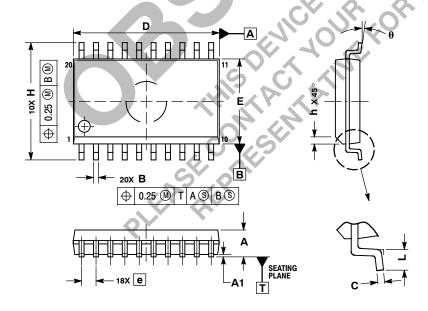
 2. CONTROLLING DIMENSION: INCH.

 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

 4. DIMENSION B DOES NOT INCLUDE MOLD

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	1.010	1.070	25.66	27.17	
В	0.240	0.260	6.10	6.60	
С	0.150	0.180	3.81	4.57	
D	0.015	0.022	0.39	0.55	
Е	0.050	BSC	1.27 BSC		
F	0.050	0.070	1.27	1.77	
G	0.100	BSC	2.54 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.140	2.80	3.55	
L	0.300 BSC		7.62 BSC		
M_	0°	15°	0°	15°	
N	0.020	0.040	0.51	1.01	

D SUFFIX PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



- DIMENSIONS ARE IN MILLIMETERS.
 INTERPRET DIMENSIONS AND TOLERANCES.
- PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD
- PROTRUSION.

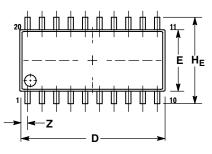
 MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- MAXIMUM MOLD PHO HUSION 0.15 PER SIDE. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

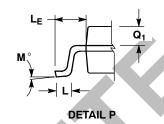
	MILLIMETERS					
DIM	MIN	MAX				
Α	2.35	2.65				
A1	0.10	0.25				
В	0.35	0.49				
С	0.23	0.32				
D	12.65	12.95				
Е	7.40	7.60				
е	1.27	BSC				
Н	10.05	10.55				
h	0.25	0.75				
L	0.50	0.90				
A	0 0	7 0				

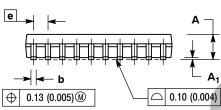
PACKAGE DIMENSIONS

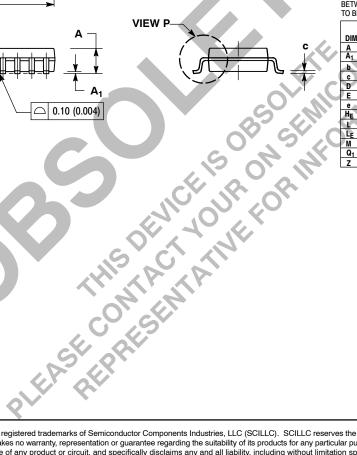
M SUFFIX

SOEIAJ PACKAGE CASE 967-01 **ISSUE O**









NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
 THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH
 DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT, MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α		2.05	j	0.081
A₁_ˈ	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e_	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
7	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10°
Q_1	0.70	0.90	0.028	0.035
Z		0.81		0.032

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