ISL6388

Advanced Linear EAPP Digital 6-Phase Green PWM Controller for Digital Power Management With NVM and AUTO Phase Shedding

FN8571
Rev 0.00
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The ISL6388 is a **smart** and **smallest** 6-Phase **Green** PWM controller, designed to be compliant to Intel VR12.5/VR12 specifications and control the microprocessor core or memory voltage regulator. It includes programmable functions and telemetries for easy use, system flexibility and over-clocking applications using SMBus, PMBus, or I^2C interface, which is designed to be conflict free with CPU's SVID bus and to program NVM banks up to 8 different compensations and system parameters. This **minimizes** external components and significantly reduces design complexity and PCB area, and **simplifies** the manufacturing process.

The ISL6388 utilizes Intersil's proprietary **Advanced Linear EAPP** (Enhanced Active Pulse Positioning) **Digital** control scheme to achieve the extremely fast linear transient response with fewer output capacitors and overcomes many hurdles of traditional digital approach, which uses non-linear, discrete control method for both voltage loop and current balance loop and runs into beat frequency oscillation and non-linear response. The ISL6388 accurately monitors the load current via the IMON pin and reports this information via the I_{OUT} register to the microprocessor, which sends a PSI# signal to the controller at low power mode via SVID bus. The controller enters 1- or 2-phase operation in low power mode (PSI1); in the ultra low power mode (PSI2, PSI3), it operates in single phase with diode emulation option. In low power modes, the magnetic core and switching losses are significantly reduced, yielding high efficiency at light load. After the PSI# signal is de-asserted, the dropped phase(s) are added back to sustain heavy load transient response and efficiency. In addition, the ISL6388 features auto-phase shedding to optimize the efficiency from light to full load for **Greener Environment** without sacrificing the transient performance.

The ISL6388 senses the output current continuously by a dedicated current sense resistor or the DCR of the output inductor. The sensed current flows through a digitally programmable 1% droop resistor for precision load-line control. Current sensing circuits also provide the needed signals for channel-current balancing, average overcurrent protection and individual phase current limiting. The TM pin senses an NTC thermistor's temperature, which is internally digitized for thermal monitoring and for integrated thermal compensation of the current sense elements of the regulator.

The ISL6388 features remote voltage sensing and completely eliminates any potential difference between remote and local grounds. This improves regulation and protection accuracy. The threshold-sensitive enable input is available to accurately coordinate the start-up of the ISL6388 with other voltage rails.

Features

- Intel VR12.5/VR12 compliant for core and memory
  - Programmable IMAX, TMAX, BOOT, DVID rate, address
- SMBus/PMBus/I^2C compatible
  - Up to 1.5MHz bus interface with SVID conflict free
  - NVM to store up to 8 configurations with programmable frequency, droop, auto, faults (OCP, UVP, CFP), etc.
  - No firmware required and hassle free with checksum
- **Advanced Linear EAPP Digital** control scheme (patented)
  - Digitally programmable compensation
  - Auto phase shedding option for greener environment
  - Variable frequency control during load transients to reduce beat frequency oscillation
  - Linear control with evenly distributed PWM pulses for better phase current balance during load transients
  - Voltage feed-forward and ramp adjustable options
  - High frequency and PSI compensation
  - Active phase adding and dropping with diode emulation scheme for enhanced light load efficiency
- Phase doubler and coupled-inductor compatibility
- Differential remote voltage sensing with ±0.5% accuracy
- Programmable 1- or 2-phase operation in PSI1 mode
- Programmable slew rate of fast dynamic VID with dynamic VID compensation (DVC)
- Support 5V PWM or 3.3V PWM DrMOS and driver
- Zero current shutdown with ISL6627
- Precision resistor or DCR differential current sensing
  - Accurate load-line (Droop) programming and control
  - Accurate current monitoring and channel-current balancing with calibration capability
- True input current sensing for catastrophic failure protection
- Average overcurrent protection and channel-current limiting
- High common mode current sense input (VCC-1.5V)
- Open sensing and single point of loop failure protection
- Thermal monitoring and integrated compensation
- 1- to 6-Phase option and up to 2MHz per phase
- Start-up into pre-charged load
- Pb-Free (RoHS Compliant) 40 Ld 5x5 Plastic Package

Applications

- Core and memory for Intel VR12/VR12.5 based processor
- High performance server core or memory rail
- High performance graphic rail
- High-end desktop with over-clocking option

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Ordering Information

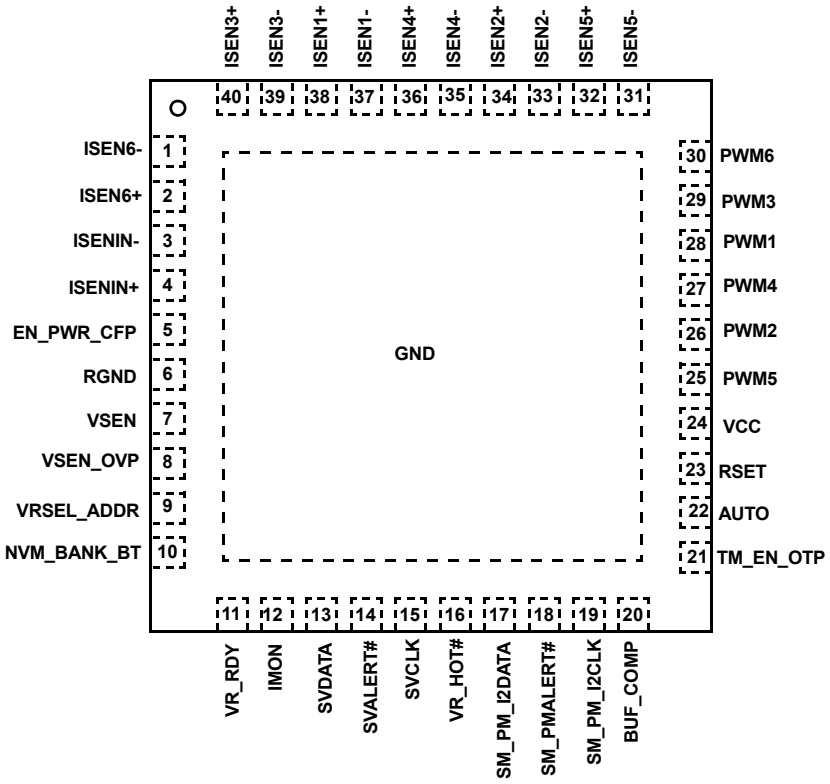
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6388HRTZ	ISL6388 HRTZ	-10 to +100	40 Ld 5x5 TQFN	L40.5x5
ISL6388IRTZ	ISL6388 IRTZ	-40 to +85	40 Ld 5x5 TQFN	L40.5x5
ISL6388EVAL1Z	6-Phase Evaluation Board with Socket R3 for VR12.5 Server			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL6388
(40 LD 5X5 TQFN)
TOP VIEW

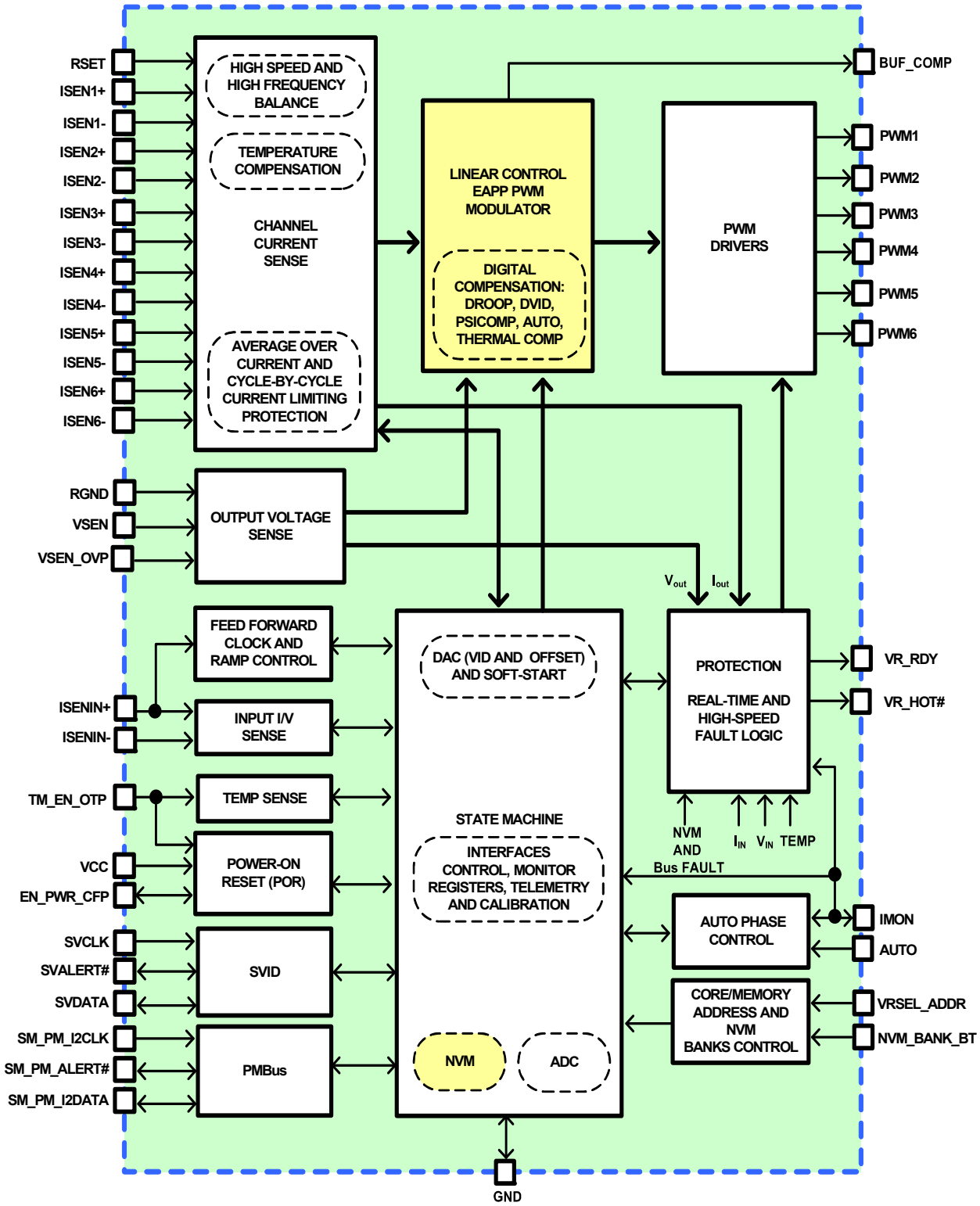


Driver/DrMOS Recommendation

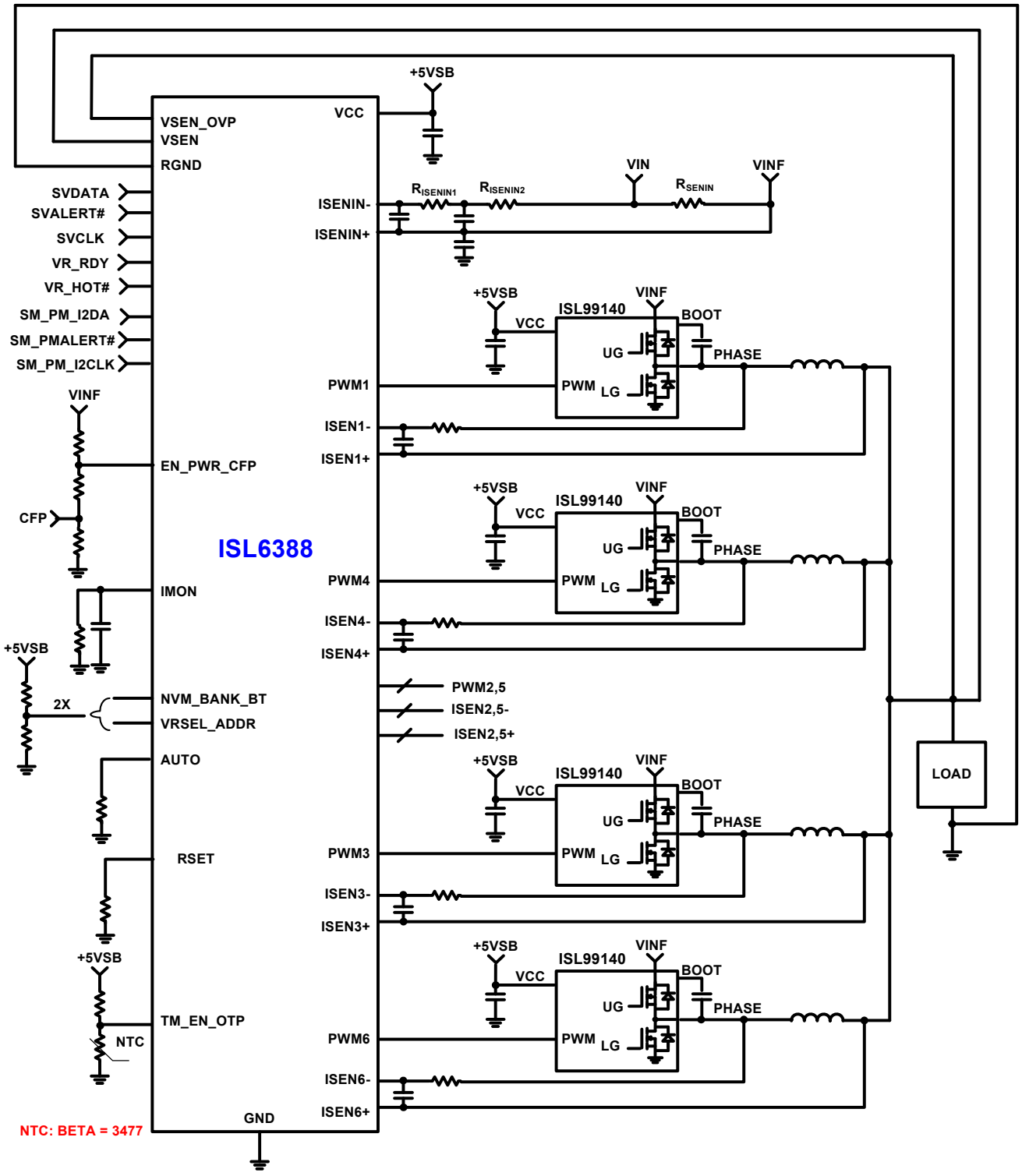
DRIVER/ DrMOS	QUIESCENT CURRENT (mA)	GATE DRIVE (V)	# OF DRIVERS	DIODE EMULATION (DE)	GATE DRIVE DROP (GVOT)	COMMENTS
ISL6627	1.0	5V	Single	Yes	No	For PSI# channel (and its coupled channel in coupled inductor applications) or all channels.
ISL6620 ISL6620A	1.2	5V	Single	Yes	No	For PSI# channel (and its coupled channel in coupled inductor applications) or all channels. Shorter body diode conduction time when entering PSI2 mode at a fixed voltage.
ISL6596	0.19	5V	Single	No	No	For dropped phases or all channels without DE.
ISL6610 ISL6610A	0.24	5V	Dual	No	No	For dropped phases or all channels without DE.
ISL6611A	1.25	5V	Dual	No	No	Phase Doubler with Integrated Drivers, up to 12-Phase. For all channels with DE Disabled.
ISL6617	5.0	N/A	N/A	No	No	PWM Doubler for DrMOS, up to 12- or 24-Phase. For all channels with DE Disabled.
ISL6622	5.5	12V	Single	Yes	Yes	For PSI# channel (and its coupled channel in coupled inductor applications) or all channels. Shorter body diode conduction time when entering PSI2 mode at a fixed voltage.
ISL6622A ISL6622B	5.5	12V	Single	Yes	No Yes	For PSI# channel (and its coupled channel in coupled inductor applications) or all channels. Shorter body diode conduction time when entering PSI2 mode at a fixed voltage.
ISL99140	0.47	5V	Single	Yes	No	DrMOS with 40A current capability. ISL99140's diode emulation is not compatible with ISL6388. Both DrMOS and ISL6388 should disable their diode emulation operation.

NOTE: Intersil 5V and 12V drivers are mostly pin-to-pin compatible and allow for dual footprint layout implementation to optimize MOSFET selection and efficiency. The 5V Drivers are more suitable for high frequency and high power density applications.

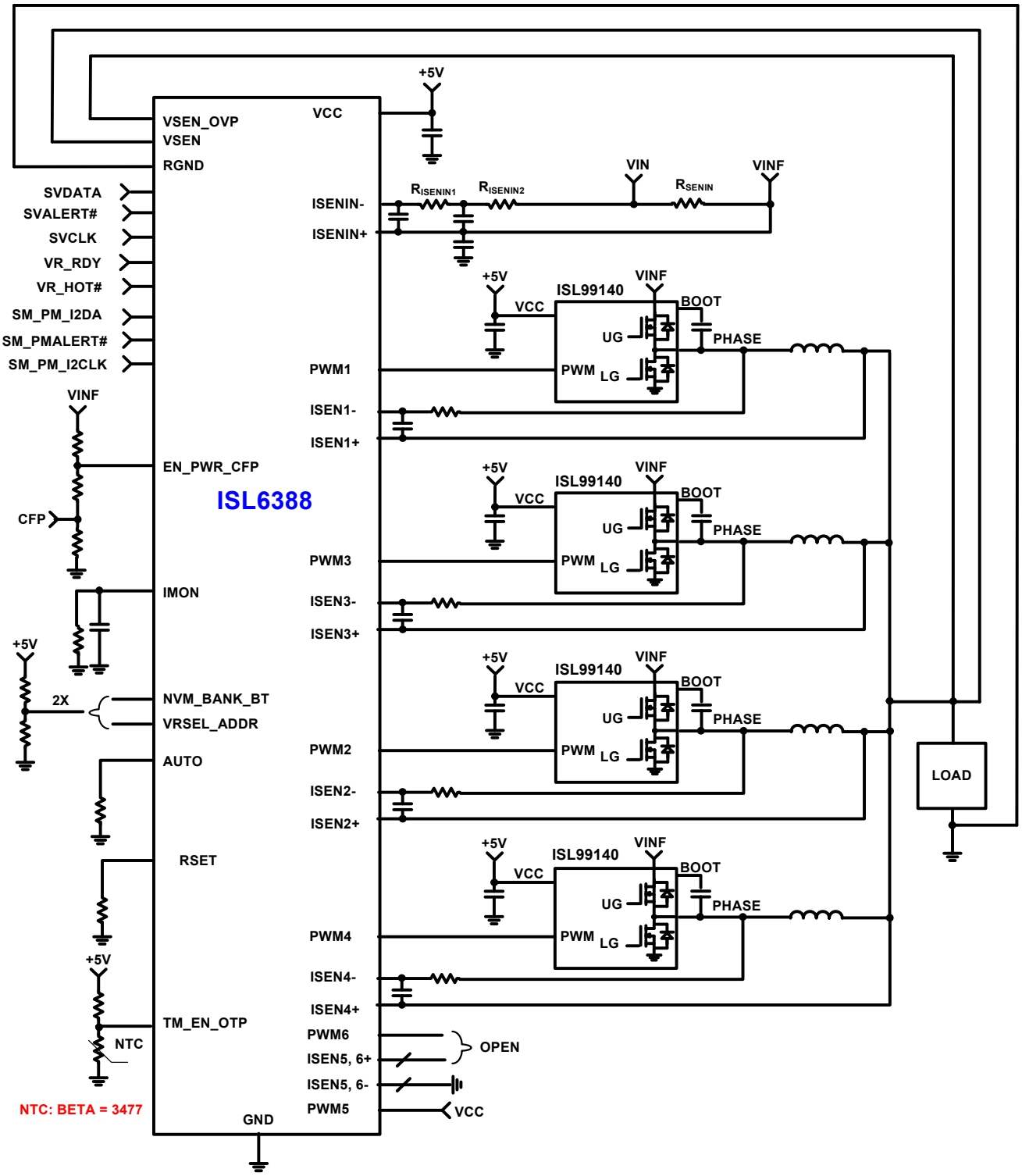
ISL6388 internal Block Diagram



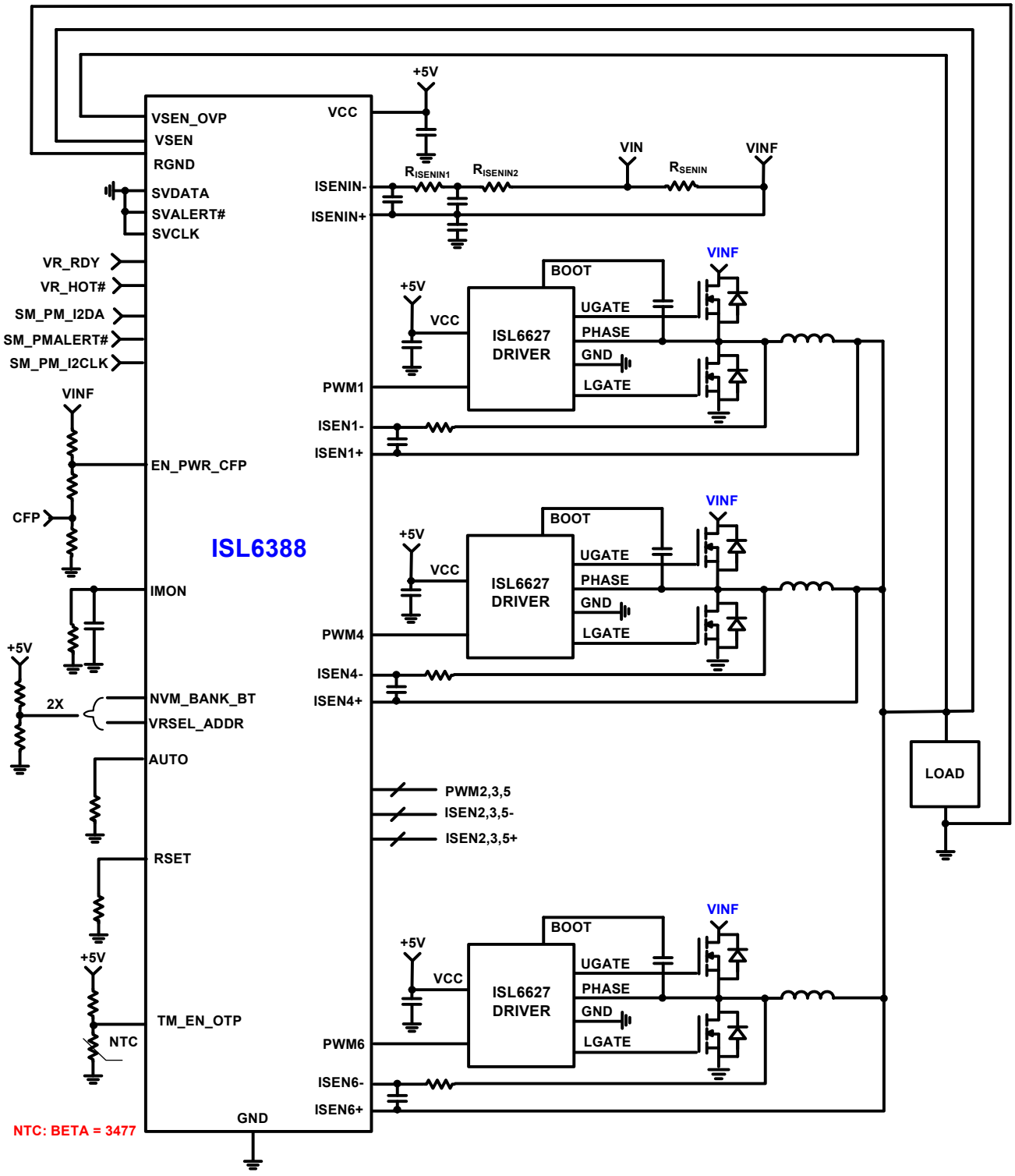
Typical Application: 6-Phase Core VR With PMBus/SMBus/I²C



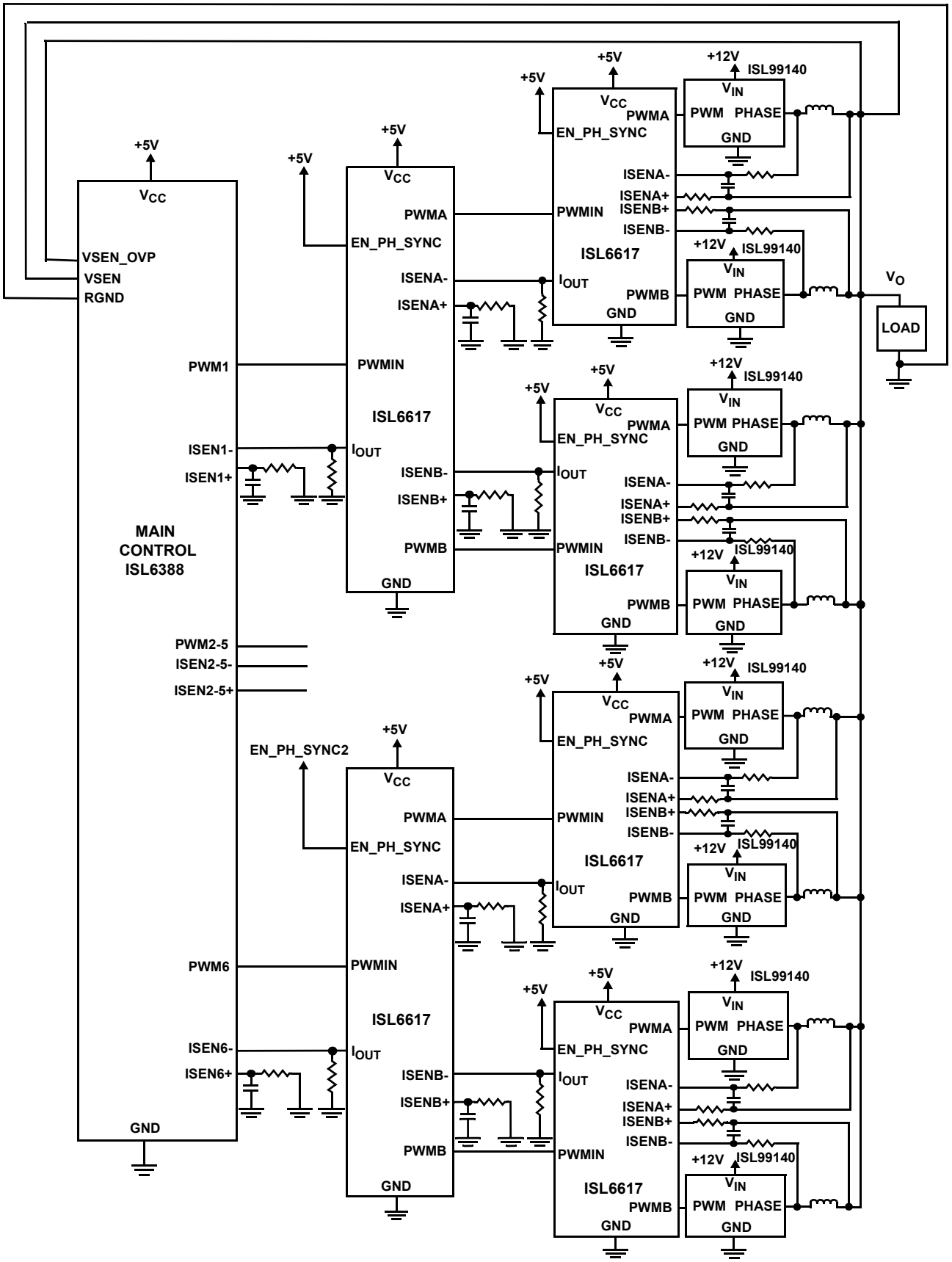
Typical Application: 4-Phase Memory VR With PMBus/SMBus/I²C



Typical Application: 6-Phase General Processor VR



Typical Application: 12-Phase Over-clocking VR



Absolute Maximum Ratings

VCC, VR_RDY . . . . . +6V
ISENIN± . . . . . .GND -0.3V to 27V
All Other Pins . . . . . .GND -0.3V to V_{CC} + 0.3V

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . .+5V ±5%
EEPROM Write and Store Command Temperature . . . . . .-40°C to +85°C
Ambient Temperature
ISL6388HRTZ . . . . . .-10°C to +100°C
ISL6388IRTZ . . . . . .-40°C to +85°C

Thermal Information

Thermal Resistance (Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld 5x5 TQFN Package	29	1

Maximum Junction Temperature . . . . . .+150°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply across the operating temperature range.**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{CC} SUPPLY CURRENT					
Nominal Supply	V_{CC} = 5VDC; EN_PWR_CFP = 5VDC; F_{SW} = 390kHz	-	35	**45**	mA
Shutdown Supply	V_{CC} = 5VDC; EN_PWR_CFP = 0VDC	-	27	**33**	mA
POWER-ON RESET AND ENABLE					
V_{CC} Rising POR Threshold		**4.22**	4.35	**4.55**	V
V_{CC} Falling POR Threshold		**4.00**	4.1	**4.22**	V
EN_PWR_CFP High Level Turn-OFF Threshold	Externally Driven	**3.50**	3.60	**3.70**	V
EN_PWR_CFP High Level Turn-ON Threshold	Externally Driven	**3.33**	3.52	**3.58**	V
EN_PWR_CFP Latch-OFF Level	Internally Driven, 5mA Load	**4.80**	-	**-**	V
EN_PWR_CFP Internal Pull-Up Impedance		**-**	12	**34**	Ω
EN_PWR_CFP Rising Threshold		**0.83**	0.85	**0.87**	V
EN_PWR_CFP Falling Threshold		**0.70**	0.77	**0.84**	V
DAC (VID+OFFSET)					
System Accuracy of Commercial Temperature (T_J = 0°C to +70°C, Note 6, Closed-Loop)	DAC = 1.5V to 3.04 V	**-0.5**	-	**0.5**	%VID
	DAC = 0.8V to 1.49V	**-5**	-	**5**	mV
	DAC = 0.25V to 0.795V	**-8**	-	**8**	mV
System Accuracy of ISL6388HRTZ (T_J = -10°C to +100°C, Note 6, Closed-Loop)	DAC = 1.5V to 3.04 V	**-0.55**	-	**0.55**	%VID
	DAC = 0.8V to 1.49V	**-7**	-	**7**	mV
	DAC = 0.25V to 0.795V	**-9**	-	**9**	mV
System Accuracy of ISL6388IRTZ (T_J = -40°C to +85°C, Note 6, Closed-Loop)	DAC = 1.5V to 3.04 V	**-0.6**	-	**0.6**	%VID
	DAC = 0.8V to 1.49V	**-10**	-	**10**	mV
	DAC = 0.25V to 0.795V	**-10**	-	**10**	mV
OSCILLATORS					
Accuracy of Switching Frequency Setting	390kHz, F3[2:0] = 0h = Original, ISL6388HRTZ	**355**	390	**425**	kHz
	390kHz, F3[2:0] = 0h = Original, ISL6388IRTZ	**348**	390	**425**	kHz
Maximum Switching Frequency		**-**	2.025	**-**	MHz
Minimum Switching Frequency		**-**	0.120	**-**	MHz

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply across the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Soft-Start Ramp Rate	FDVID = 1.25mV/µs	**0.3125**	-	**-**	mV/µs
	FDVID = 10mV/µs	**2.5**	3.0	**3.4**	mV/µs
	FDVID = 20mV/µs	**5.0**	6.0	**7.0**	mV/µs
	FDVID = 53mV/µs	**13.25**	-	**-**	mV/µs
Minimum Fast Dynamic VID Slew Rate	FDVID = 1.25mV/µs	**1.25**	-	**-**	mV/µs
Maximum Fast Dynamic VID Slew Rate	FDVID = 53mV/µs	**53**	-	**-**	mV/µs
Maximum Duty Cycle Per PWM	390kHz	**95**	98	**99**	%
PWM GENERATOR					
Sawtooth Amplitude	V_{RAMP_ADJ} = 0.7V, ISENIN+ = 12V	**-**	0.7	**-**	V
	V_{AMP_ADJ} = 1.0V, ISENIN+ = 12V	**-**	1.0	**-**	V
	V_{RAMP_ADJ} = 1.2V, ISENIN+ = 12V	**-**	1.2	**-**	V
	V_{RAMP_ADJ} = 1.5V, ISENIN+ = 12V	**-**	1.5	**-**	V
BUFFERED COMP AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground	**-**	96	**-**	dB
Open-Loop Bandwidth		**-**	20	**-**	MHz
Maximum Output Voltage	No Load	**3.6**	4.0	**-**	V
Output High Voltage	1mA Load	**3.4**	3.9	**-**	V
Output Low Voltage	1mA Load	**1.88**	-	**1.99**	V
PWM OUTPUT (PWM[6:1])					
PWM[6:1] Sink Impedance	PWM = Low with 1mA Load for Fast Transition	**-**	80	**-**	Ω
	PWM = Low with 1mA Load, ISL6388HRTZ	**170**	285	**425**	Ω
	PWM = Low with 1mA Load, ISL6388IRTZ	**170**	285	**400**	Ω
PWM[6:1] Source Impedance	PWM = High, Forced to 3.7V	**60**	125	**210**	Ω
PWM PSI1/2/3/Decay Mid-Level	0.4mA Load, 5V PWM	**36**	40	**44**	%VCC
PWM PSI1/2/3/Decay Mid-Level	0.4mA Load, 3.3V PWM	**24**	28	**31**	%VCC
CURRENT SENSE AND OVERCURRENT PROTECTION					
Sensed Current Tolerance CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	(T_J = 0°C to +70°C)	**73**	78	**82.5**	µA
	(T_J = -40°C to +100°C, HRTZ, IRTZ)	**72**	78	**83**	µA
Average OC Trip Level at Normal CCM PWM Mode CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	(T_J = 0°C to +70°C)	**96**	103	**111**	µA
	(T_J = -40°C to +100°C, HRTZ, IRTZ)	**95**	103	**112**	µA
Average Overcurrent Trip Level at PSI1/2/3 Mode CS Offset and Mirror Error Included, R_{SET} = 12.8kΩ	(T_J = 0°C to +70°C)	**92**	107	**122**	µA
	(T_J = -40°C to +100°C, HRTZ, IRTZ)	**90**	125	**124**	µA
Peak Current Limit for Individual Channel CS Offset & Mirror Error Included, R_{SET} = 12.8kΩ	(T_J = 0°C to +70°C)	**118**	125	**133**	µA
	(T_J = -40°C to +100°C, HRTZ, IRTZ)	**116**	125	**134**	µA
IMON OCP Trip Level		**2.9**	3.0	**3.1**	V
IMON VOLTAGE IMAX (FF) TRIP POINT	Higher than this will be “FF”	**2.45**	2.5	**2.56**	V
READ_IIN (1F) Maximum Threshold		**-**	10	**-**	µA
Input Peak Current Trip Level		**13.9**	15	**16.5**	µA
THERMAL MONITORING					
VR_HOT# Pull-down Impedance		**-**	9.2	**13**	Ω
TM Voltage at VR_HOT# Trip	TMAX = +100°C (see Table 7), Programmable via TMAX	**-**	39.12	**-**	%VCC
VR_HOT# and Thermal Alert# Hysteresis		**-**	3	**-**	°C
Leakage Current of VR_HOT#	With external pull-up resistor connected to V_{CC}	**-**	-	**1**	µA
Over-Temperature Shutdown Threshold		**0.91**	0.94	**0.97**	V

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply across the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
Over-Temperature Shutdown Reset Threshold		**1.04**	1.07	**1.11**	V
VR READY AND PROTECTION MONITORS					
Leakage Current of VR_RDY	With pull-up resistor externally connected to V_{CC}	**-**	-	**1**	µA
VR READY Low Voltage	4mA Load	**-**	-	**0.3**	V
Undervoltage Protection Threshold (UVP) Can Be Disabled by DFh	Voltage below VID E1[3:0] = 0h)	**65**	105	**146**	mV
	Voltage below VID E1[3:0] = 1h)	**93**	141	**191**	mV
	Voltage below VID E1[3:0] = 2h)	**121**	178	**236**	mV
	Voltage below VID E1[3:0] = 3h)	**149**	214	**281**	mV
	Voltage below VID E1[3:0] = 4h)	**177**	252	**330**	mV
	Voltage below VID E1[3:0] = 5h)	**207**	291	**378**	mV
	Voltage below VID E1[3:0] = 6h)	**233**	328	**426**	mV
	Voltage below VID E1[3:0] = 7h)	**288**	402	**519**	mV
Undervoltage Warning Threshold (UVP Warning) Can Be Disable by DFh	Voltage below VID E1[3:0] = 0h)	**10**	41	**72**	mV
	Voltage below VID E1[3:0] = 1h)	**35**	72	**109**	mV
	Voltage below VID E1[3:0] = 2h)	**61**	103	**146**	mV
	Voltage below VID E1[3:0] = 3h)	**84**	135	**186**	mV
	Voltage below VID E1[3:0] = 4h)	**109**	168	**226**	mV
	Voltage below VID E1[3:0] = 5h)	**133**	202	**268**	mV
	Voltage below VID E1[3:0] = 6h)	**157**	234	**307**	mV
	Voltage below VID E1[3:0] = 7h)	**201**	298	**389**	mV
Undervoltage Protection Reset Hysteresis	Higher than UVP	**-**	19	**-**	mV
Undervoltage Warning Reset Hysteresis	Higher than UVP Warning	**-**	17	**-**	mV
Overvoltage Protection Threshold (OVP) Can Be Disabled by DFh	Prior to the End of Soft-start (D8h[4:3] = 0h)	**1.51**	1.58	**1.70**	V
	Prior to the End of Soft-start (D8h[4:3] = 1h)	**1.75**	1.86	**1.95**	V
	Prior to the End of Soft-start (D8h[4:3] = 2h)	**2.20**	2.29	**2.40**	V
	Prior to the End of Soft-start (D8h[4:3] = 3h)	**3.10**	3.32	**3.50**	V
	End of Soft-start, the voltage above VID D8[2:0] = 0h)	**91**	135	**177**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 1h)	**125**	177	**225**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 2h)	**158**	218	**274**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 3h)	**191**	260	**323**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 4h)	**254**	342	**424**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 5h)	**318**	425	**526**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 6h)	**347**	460	**580**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 7h)	**395**	549	**697**	mV
Overvoltage Protection Reset Hysteresis	Prior to the End of Soft-start, Lower than OVP	**55**	110	**180**	mV
	During Operation, Lower than OVP	**-**	83	**-**	mV
Overvoltage Warning Threshold (OVP) Can Be Disabled by DFh	End of Soft-start, the voltage above VID D8[2:0] = 0h)	**22**	54	**83**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 1h)	**60**	96	**129**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 2h)	**97**	138	**176**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 3h)	**132**	179	**225**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 4h)	**205**	264	**324**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 5h)	**273**	347	**427**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 6h)	**308**	389	**476**	mV
	End of Soft-start, the voltage above VID D8[2:0] = 7h)	**377**	474	**578**	mV
Overvoltage Warning Reset Hysteresis	Lower than OVP Warning	**-**	42	**-**	mV

Electrical Specifications Recommended Operating Conditions, V_{CC} = 5V, Unless Otherwise specified. **Boldface limits apply across the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
SVID BUS					
SVALERT# Pull-down Impedance		-	-	**13**	Ω
SVDATA		-	-	**13**	Ω
SVCLK Maximum Speed at Room Temperature	T_J = +25°C	-	60	-	MHz
SVCLK Maximum Speed		-	43	-	MHz
SVCLK Minimum Speed		-	13	-	MHz
SMBus/PMBus/I^{2}C					
ALERT# Pull-down Impedance		-	28	**50**	Ω
DATA Pull-down Impedance		-	28	**50**	Ω
CLOCK Maximum Speed		**1.5**	-	-	MHz
CLOCK Minimum Speed		-	-	**0.05**	MHz
Time-out		-	35	-	ms
EEPROM					
Number of NVM_BANK		-	8	-	-
NVM_BANK Loading Time	Including POR delay and Resistor Reading Time	-	16	**20**	ms

NOTES:

6. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Functional Pin Descriptions

Refer to Table 20 on page 55 for Design and Layout Considerations.

VCC - Supplies the power necessary to operate the chip. Connect this pin directly to a +5V supply with a high quality ceramic bypass capacitor. The controller start to operate, when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold.

GND - The bottom metal base of ISL6388 is return of VCC supply. It is also the return of SVID and PMBus Buses as well as all PWM output drivers. Connect it to system ground.

ISENIN+, ISENIN- - These pins are current sense inputs to differential amplifier of the input supply. The sensed current is used for input power monitoring and power management of the system. When is not used, connect ISENIN+ to VIN and a resistor divider with a ratio of 1/3 on ISENIN± pin, say 499k Ohm in between ISENIN± pins and then 1.5MΩ from ISENIN- to ground (see Figure 29). Refer to “Input Current Sensing” on page 32 for configuration details. Regardless input current sense is used or not, ISENIN+ should be connected to input voltage (V_{IN}) for feed-forward compensation to maintain a constant loop gain over the input line variation.

EN_PWR_CFP - This pin is a threshold-sensitive enable input and a catastrophic failure protection (CFP) output. Connecting the power train input supply to this through an appropriate resistor divider provides input undervoltage protection and a means to synchronize the power sequencing of the controller and the MOSFET driver ICs. When EN_PWR_CFP is driven above 0.85V but below 3.3V, the controller is actively depending on status of the TM_EN_OTP, the internal POR, and pending fault states. Driving EN_PWR_CFP below 0.75V or above 3.7V will turn off the controller, clear all fault states (except for CFP fault) and prepare the ISL6388 to soft-start when re-enabled. In addition, this pin will be latched high (VCC) by the input overcurrent (monitored by ISENIN±) or VR overvoltage event. The latch resets by cycling VCC and cannot reset by TM_EN_OTP or EN_PWR_CFP since when the catastrophic failure (CFP) is triggered, the input power is removed from VR so is the VTT voltage rail and it is PGOOD signal. To keep CFP active, VCC should be biased with a standby supply. This feature means to provide protection to the case that the VR with shorted high-side MOSFET draws insufficient current to trigger the input supply’s overcurrent trip level, this pin will send an active high signal (CFP) to disconnect the input supply before catching fire or further damage of PCB. Refer to “Catastrophic Fault Protection” on page 31 for more details

VSEN_OVP - This pin monitors the regulator output for Overvoltage protection. Connect this pin to the positive rail remote sensing point of the microprocessor or load. This pin tracks with the VSEN pin. If a resistive divider is placed on the VSEN pin, a resistive divider with the same ratio should be placed on the VSEN_OVP pin to track UVP and OVP.

VSEN - This pin compensates the voltage drop between the load and local output rail for precision regulation. Connect this pin to the positive rail remote sensing point of the microprocessor or load. It also is the APA level sensing input.

RGND - This pin compensates the offset between the remote ground of the load and the local ground of this device for precision regulation. Connect this pin to the negative rail remote sensing point of the microprocessor or load.

VR_RDY - VR_RDY indicates that soft-start has completed and the output remains in normal operation. It is an open-drain logic output. When OCP, UVP, OVP, or CFP occurs, VR_RDY is pulled low.

TM_EN_OTP - Input pin for the temperature measurement. Connect this pin through an NTC thermistor to GND and a resistor to VCC of the controller. The voltage at this pin is inversely proportional to the VR temperature. The device monitors the VR temperature based on the voltage at the TM pin. Combined with “TCOMP” setting, the sensed current is thermally compensated. The VR_HOT# asserts low if the sensed temperature at this pin is higher than the maximum desired temperature, “TMAX”. The NTC should be placed close to the current sensing element, the output inductor or dedicated sense resistor on Phase 1. A decoupling capacitor (0.1µF) is typically needed in close proximity to the controller. In addition, the controller is disabled when this pin’s voltage drops below 0.95 (typically) and is active when it is above 1.05V (typically); it can serve as Enable and Over-Temperature functions, however, when it is used as an Enable toggle input, bit2 of STATUS_BYTE (78h) will flag OT; CLEAR_FAULTS (03h) command must be sent to clear the fault after VR start-up. If not used, connect a 1MΩ/2MΩ resistor divider or tie to V_{CC}.

PWM[6:1] - Pulse width modulation outputs. Connect these pins to the PWM input pins of the Intersil driver IC(s). The number of active channels is determined by the state of PWM[6:2]. Tie PWM(N+1) to VCC to configure for N-phase operation. PWM firing order is sequential from 1 to N with N being the number of active phases. If PWM1 is tied high, the respective address is released for use, i.e, the VR is disabled and does not respond to the SVID commands.

ISEN[6:1]+, ISEN[6:1] - The ISEN+ and ISEN- pins are current sense inputs to individual differential amplifiers of VR. The sensed current is used for channel-current balancing, overcurrent protection, and droop regulation. Inactive channels should have their respective current sense inputs, ISEN[6:#]- grounded, and ISEN[6:#]+ open. For example, ground ISEN[6:5]- and open ISEN[6:5]+ for 4-phase operation. DO NOT ground ISEN[6:1]+. For DCR sensing, connect each ISEN- pin to the node between the RC sense elements. Tie the ISEN+ pin to the other end of the sense capacitor (typically output rail). The voltage across the sense capacitor is proportional to the inductor current. Therefore, the sensed current is proportional to the inductor current and scaled by the DCR of the inductor and R_{SET}.

BUF_COMP - Buffered output of internal COMP.

VR_HOT# - Indicator of VR temperature reaching above TMAX set by PMBus E8[2:0]. It is an open-drain logic output. Normally open if the measured VR temperature is less than TMAX, and pulled low when the measured VR temperature exceeds TMAX.

RSET - A resistor connected from this pin to ground sets the current gain of the current sensing amplifier. The RSET resistor value can be set from 3.84kΩ to 60.4kΩ and is 64x of the equivalent R_{ISEN} resistor value. Therefore, the effective current sense resistor value can be set between 60Ω and 943Ω.

IMON - IMON is the output pin of sensed, thermally compensated (if internal thermal compensation is used) average current of VR. The voltage at the IMON pin is proportional to the load current and the resistor value. When it reaches to 3.0V, it initiates an overcurrent shutdown, while 2.5V IMON voltage corresponds to maximum SVID IOUT (15h) reading (FFh) and PMBus READ_IOUT (8Ch) maximum reading. By choosing the proper value for the resistor at IMON pin, the overcurrent trip level can be set lower than the fixed internal overcurrent threshold. During dynamic VID, the OCP function of this pin is disabled to avoid false triggering. Tie it to GND if not used. Refer to "Current Sense Output" on page 26 for more details.

AUTO - A resistor from the pin to ground sets the current threshold of phase dropping for operation. The AUTO mode can be permanently disabled by pulling this pin to ground or PMBus D4h[2]. See Table 3 on page 17 and Table 9 on page 33 for more details.

SVCLK - Synchronous clock signal input of SerialVID bus from CPU.

SVDATA - I/O pin for transferring data signals between CPU and VR controller.

SVALERT# - Output pin for transferring the active low signal driven asynchronously from the VR controller to CPU.

SM_PM_I2CLK - Synchronous clock signal input of SMBus/PMBus/I^2C.

SM_PM_I2DATA - I/O pin for transferring data signals SMBus/PMBus/I^2C and VR controller.

SM_PMALERT# - Output pin for transferring the active low signal driven asynchronously from the VR controller to SMBus/PMBus.

VRSEL_ADDR - Register pin used to program VR address (SVID and PMBus) and to determine VR12 or VR12.5 mode.

NVM_BANK_BT - Register pin to select NVM memory bank to use (up to 8 configuration banks) and boot voltage, which can be set by this pin or the value stored in NVM bank.

Operation

The ISL6388 is the **smallest** 6-Phase PWM controller. It utilizes Intersil's proprietary Advanced Linear EAPP (Enhanced Active Pulse Positioning) digital control scheme that can process voltage and current information in real time for fast control and high speed protection and realize digital power management capability and flexibility. It achieves the extremely fast linear transient response with fewer output capacitors and overcomes many hurdles of traditional digital approach, which uses non-linear, discrete control method for both voltage loop and current balance loop and runs into beat frequency oscillation and non-linear response. The ISL6388 is designed to be compliant to Intel VR12.5/VR12 specifications with SerialVID features. The system parameters and SVID required registers are programmable and can be stored into selected NVM_BANK via PMBus, no firmware required. It allows up to 8 memory banks, i.e., 8 different applications. This greatly simplifies the system design for various platforms and lowers inventory complexity and cost by using a single device.

In addition, this controller is compatible with phase doublers (ISL6611A and ISL6617), which can double or quadruple the phase count. For instance, the multi-phase PWM can realize up to 24-phase count system. A higher phase count system can improve thermal distribution and power conversion efficiency at heavy load.

The ISL6388 also supports coupled (2-Phase CI) inductor design. Refer to Intersil's application note, AN1268 for detailed coupled inductor discussion.

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multiphase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter (which are both cost-effective and thermally viable), have forced a change to the cost-saving approach of multiphase. The ISL6388 controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The typical application circuits diagrams on pages 6 through 9 provide the top level views of multiphase power conversion using the ISL6388 controller.

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out-of-phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the 3-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase, as illustrated in Figure 1. The three channel-currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel-current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multiphase circuit, examine Equation 1, which represents an individual channel's peak-to-peak inductor current.

$$I_{P-P} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot F_{SW} \cdot V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and F_{SW} is the switching frequency.

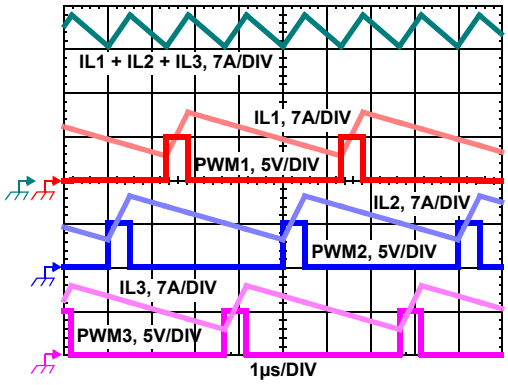


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2, the peak-to-peak overall ripple current $I_{C(P-P)}$ decreases with the increase in the number of channels, as shown in Figure 2.

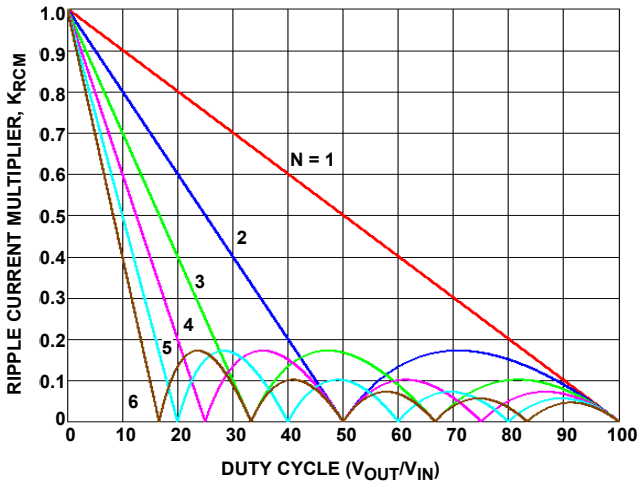


FIGURE 2. RIPPLE CURRENT MULTIPLIER vs DUTY CYCLE

Output voltage ripple is a function of capacitance, capacitor Equivalent Series Resistance (ESR), and the summed inductor ripple current. Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and few or less costly output capacitors for any performance specification.

$$I_{c(p-p)} = \frac{V_{OUT}}{L \cdot F_{SW}} K_{RCM} \quad \text{(EQ. 2)}$$

$$K_{RCM} = \frac{(N \cdot D - m + 1) \cdot (m - (N \cdot D))}{N \cdot D}$$

for $m - 1 \le N \cdot D \le m$

$m = \text{ROUNDUP}(N \cdot D, 0)$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitors. The example in Figure 3 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 3 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has $11.9A_{RMS}$ input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Figures 37, 38 and 39, as described in on “Input Capacitor Selection” on page 54, can be used to determine the input capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 40 shows the single phase input-capacitor RMS current for comparison.

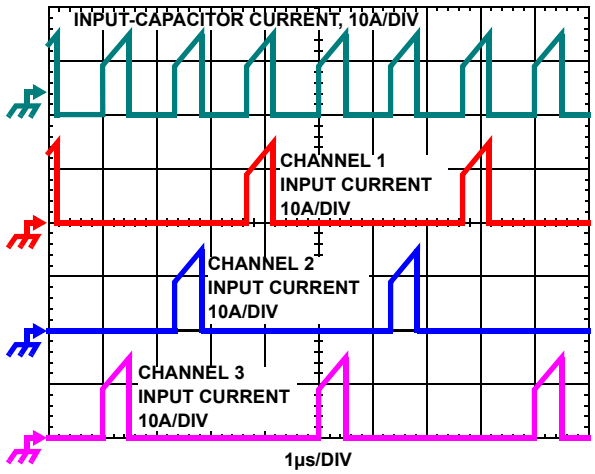


FIGURE 3. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

PWM Modulation Scheme

The ISL6388 adopts Intersil's proprietary Enhanced Active Pulse Positioning (EAPP) modulation scheme to improve transient performance. The EAPP is a unique dual-edge PWM modulation scheme with both PWM leading and trailing edges being independently moved to give the best response to load apply and load release. The EAPP has an inherited function, similar to Intersil's proprietary Adaptive Phase Alignment (APA) technique, to turn on all phases together to further improve the transient response, when there are sufficiently large load step currents. The EAPP is a variable frequency architecture, providing linear control over transient events and evenly distributing the pulses among all phases to achieve very good current balance and eliminate beat frequency oscillation over a wide range of load transient frequencies.

To further improve the line and load transient responses, the multi-phase PWM features feed-forward function to change the up ramp with the input line (voltage on ISENIN+ pin) to maintain a constant overall loop gain over a wide range input voltage. The up ramp of the internal Sawtooth is defined in Equation 3.

$$V_{RAMP} = \frac{V_{IN} \cdot V_{RAMP\_ADJ}}{12V} \quad \text{(EQ. 3)}$$

With EAPP control and feed-forward function, the ISL6388 can achieve excellent transient performance over wide frequency range of load step, resulting in lower demand on the output capacitors.

At DC load conditions, the PWM frequency is constant during normal mode (PSI0) and low power mode (PSI1). However, when PSI2 or PSI3 is asserted in ultra low power conditions, if the VR is configured for diode emulation operation, the EAPP reduces the switching frequency as the load decreases. Thus, the VR can enter burst mode at extreme light load conditions and improve power conversion efficiency significantly. Under steady state conditions, the operation of the ISL6388 PWM modulator is similar to a conventional trailing edge modulator. Conventional analysis and design methods can therefore be used for steady state and small signal analysis.

PWM and PSI# Operation

The timing of each channel is set by the number of active channels. The default channel setting for the ISL6388 is six. The switching cycle is defined as the time between PWM pulse termination signals of each channel. The cycle time of the pulse signal is the inverse of the switching frequency. The PWM signals command the MOSFET driver to turn on/off the channel MOSFETs.

The ISL6388 can work in a 0 to 6-Phase configuration. Tie PWM(N+1) to V_{CC} to configure for N-phase operation. PWM firing order is sequential from 1 to N with N being the number of active phases, as summarized in Table 1. For 6-phase operation, the channel firing sequence is 1-2-3-4-5-6, and they are evenly spaced over 1/6 of a cycle. Connecting PWM6 to V_{CC} configures 5-phase operation, the channel firing order is 1-2-3-4-5 and the phase spacing is 1/5 of a cycle. If PWM2 is connected to V_{CC}, only Channel 1 operation is selected. If PWM1 is connected to V_{CC}, the VR operation is turned off.

TABLE 1. PHASE NUMBER AND PWM FIRING SEQUENCE

N	PHASE SEQUENCE PSI# = PSI0	PWM# TIED TO VCC	ACTIVE PHASE PSI# = PSI1
5	1-2-3-4-5	None	PWM1/3
4	1-2-3-4	PWM5	PWM1/3
3	1-2-3	PWM4	PWM1/2
2	1-2	PWM3	PWM1/2
1	1	PWM2	PWM1
0	OFF	PWM1	OFF

The CPU can enter four distinct power states as shown in Table 2. The ISL6388 supports all states, but it treats PSI2 and PSI3 the same. In addition, the setDecay mode will automatically enter PSI2 state while the output voltage decaying. However, prior to the end of soft-start (i.e: VR_RDY goes high), the lower power modes (PSI1/2/3/Decay) are NOT enabled.

TABLE 2. POWER STATE COMMAND FROM CPU

STATE	DESCRIPTION
PSI0	High Power Mode, All Phases are running
PSI1	Low Power Mode
PSI2	Very Low Power Mode
PSI3	Ultra Low Power Mode, treated as PSI2
Decay	Automatically enter PSI2 and Ramp down the output voltage reference to the target voltage

When the SVID bus sends PSI1/2/3 or Set VID Decay command, it indicates the low power mode operation of the processor. The controller starts phase shedding the next switching cycle. The controller reduces the number of active phases according to the logic on Table 3. “NPSI” register and AUTO pin program the controller in operation of standard (SI), 2-phase coupled, or (N-x)-phase coupled inductors. Different cases yield different PWM output behaviors on both dropped phase(s) and operational phase(s) as PSI# is asserted and de-asserted. When CPU sends PSI0 command, it pulls the controller back to normal CCM PWM operation to sustain an immediate heavy transient load. Note that “N-x” means N-x phase(s) coupled and x phase(s) are uncoupled.

For 2-Phase coupled inductor (CI) operation, both coupled phases should be 180° out-of-phase. In low power states (PSI1/2/3/Decay), the opposite phase of the operational phase turns on its Low-side MOSFET to circulate inductor current to minimize conduction loss when Phase 1 is high.

When PSI1 is asserted, VR0 is in single-phase CCM operation with PWM1, or 2-phase CCM operation with PWM1 and 2, 3 or 4, as shown in Table 1. The number of operational phases is configured by “NPSI” register, shown in Table 3. In PSI2/3/Decay, only PWM1 is in DCM/CCM operation, which is programmed by the “DE” register; the opposite PWM (2, 3, or 4, depending upon configured maximum phase number as in Table 1) pulls low when PWM1 is high (CI applications).

TABLE 3. PHASE DROPPING CONFIGURATION AT PSI1 AND PSI2/3/DECAY

NPSI D2[1:0]	CODE		PSI1 MODE	PSI2/3 AND DECAY
0h	SI1	SI, (N-1)-CI	1-Phase	1-Phase
1h	SI2	SI, (N-2)-CI	2-Phase	1-Phase
2h	CI1	2-Phase CI	1-Phase	1-Phase
3h	CI2	2-Phase CI	2-Phase	1-Phase

NOTE: For 2-Phase CI option, the dropped coupled phase turns on LGATE to circulate current when PWM1 is high. Programmable via PMBus.

While the controller is operational (V_{CC} above POR, TM_EN_OTP and EN_PWR_CFP are both high, valid VID inputs), it can pull the PWM pins to ~40% of V_{CC} (~2V for 5V V_{CC} bias, for 5V PWM) or ~28% of V_{CC} (for 3.3V PWM) during various stages, such as soft-start delay, phase shedding operation, or fault conditions (OC or OV events). The matching driver's internal PWM resistor divider can further raise the PWM potential, but not lower it below the level set by the controller IC. Therefore, the controller's PWM outputs are designed to be compatible with DrMOS and Intersil drivers that require 3.3V and 5V PWM signal amplitudes, programmed by PMBus.

Diode Emulation Operation

To improve light load efficiency, the ISL6388 can enter diode emulation operation in PSI2/3 or Decay mode. Users should select Intersil VR12/VR12.5 compatible drivers: The ISL6627 or ISL6622 for PSI# channel(s). The diode emulation should be disabled via PMBus when non-compatible power stages or drivers are used.

DrMOS and Driver Compatibility

In operational mode, the ISL6388 can actively drive PWM into tri-state level (mid level), which can be programmed to be compatible with 3.3V or 5V PWM input DrMOS or Drivers. The ISL6388’s PWM “LOW” level is 0V and PWM “HIGH” level is V_{CC} (5V). The PWM “HIGH” minimum threshold of the DrMOS should be higher than 33% of V_{CC} for 3.3V PWM logic and 44% of V_{CC} for 5V PWM logic, while the PWM “LOW” maximum threshold of the DrMOS should be lower than 26% of V_{CC} for 3.3V PWM logic and 36% of V_{CC} for 5V PWM logic. Since most of industrial DrMOS

devices are not compatible with Intersil's PWM protocol for diode emulation, therefore, the diode emulation mode should be disabled in both controller and DrMOS. Coupling with the ISL6627, zero current shutdown can be achieved, which minimizes the power stage stress.

Phase Doubler Compatibility

The ISL6388 is compatible with phase doublers (ISL6611A and ISL6617), which can double or quadruple the phase count. For instance, the multi-phase PWM can realize up to 24-phase count system. A higher phase count system can improve thermal distribution and power conversion efficiency at heavy load. Non-Intersil Phase doubler typically does not have current balance and is not compatible with Intersil's multi-phase controllers.

Pre-charged Start-up Capability

Since the ISL6388 uses 5V bias and the high efficiency power train mostly uses 5V driver, this makes the ISL6388 digital power system much more robust and reliable for power-up and down as well as pre-charged start-up, which is typically hardly managed for a system that deals with 3.3V, 5V, and 12V supplies.

Switching Frequency

The VR's switching frequency is programmable from 120kHz to 2.025MHz via PMBus. It is 15kHz/step with a slew rate of step/20µs.

Current Sensing

The ISL6388 senses current continuously for fast response. The ISL6388 supports inductor DCR sensing, or resistive sensing techniques. The associated channel-current sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. The sense current, I_{SEN}, is proportional to the inductor current. The sensed current is used for current balance, load-line regulation, and overcurrent protection.

The internal circuitry, shown in Figures 4 and 5, represents one channel of the VR output, respectively. The ISEN± circuitry is repeated for each channel, but may not be active depending on the status of the PWM[6:2] pins, as described in "PWM and PSI# Operation" on page 17. The input bias current of the current sensing amplifier is typically 25nA; less than 7kΩ input impedance is preferred to minimized the offset error, i.e., a larger C value as needed.

INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance, as measured by the Direct Current Resistance (DCR) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 4. The channel-current I_L, flowing through the inductor, will also pass through the DCR. Equation 4 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 4)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 4.

The voltage on the capacitor V_C, can be shown to be proportional to the channel-current I_L (see Equation 5).

$$V_C(s) = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 5)}$$

If the R-C network components are selected such that the RC time constant matches the inductor time constant (R*C = L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e., proportional to the channel-current.

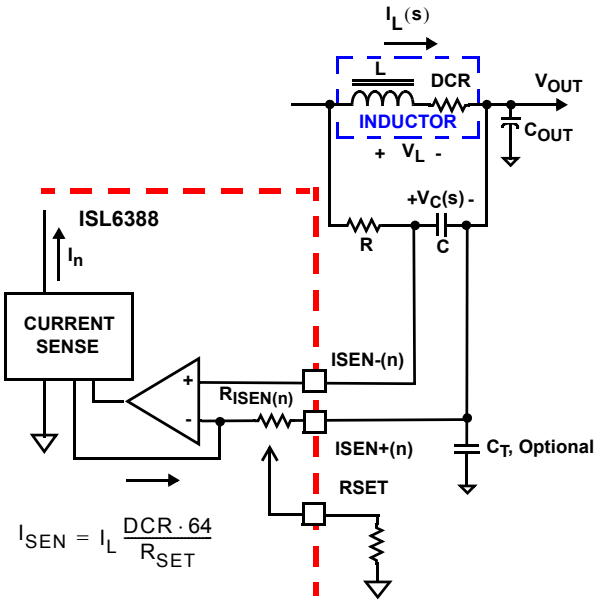


FIGURE 4. DCR SENSING CONFIGURATION

With the internal low-offset current amplifier, the capacitor voltage V_C is replicated across the sense resistor R_{ISEN}. Therefore, the current out of the ISEN+ pin, I_{SEN}, is proportional to the inductor current.

Equation 6 shows that the ratio of the channel-current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} = I_L \frac{DCR \cdot 64}{R_{SET}} \quad \text{(EQ. 6)}$$

RESISTIVE SENSING

For more accurate current sensing, a dedicated current-sense resistor R_{SENSE} in series with each output inductor can serve as the current sense element (see Figure 5). This technique however reduces overall converter efficiency due to the additional power loss on the current sense element R_{SENSE}.

A current sensing resistor has a distributed parasitic inductance, known as ESL (equivalent series inductance, typically less than 1nH) parameter. Consider the ESL as a separate lumped quantity, as shown in Figure 5. The channel-current I_L, flowing through the inductor, will also pass through the ESL. Equation 7 shows the s-domain equivalent voltage across the resistor V_R.

$$V_R(s) = I_L \cdot (s \cdot ESL + R_{SEN}) \quad \text{(EQ. 7)}$$

A simple R-C network across the current sense resistor extracts the R_{SEN} voltage, as shown in Figure 5.

The voltage on the capacitor V_C, can be shown to be proportional to the channel-current I_L (see Equation 8).

$$V_C(s) = \frac{\left(s \cdot \frac{ESL}{R_{SEN}} + 1\right) \cdot (R_{SEN} \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 8)}$$

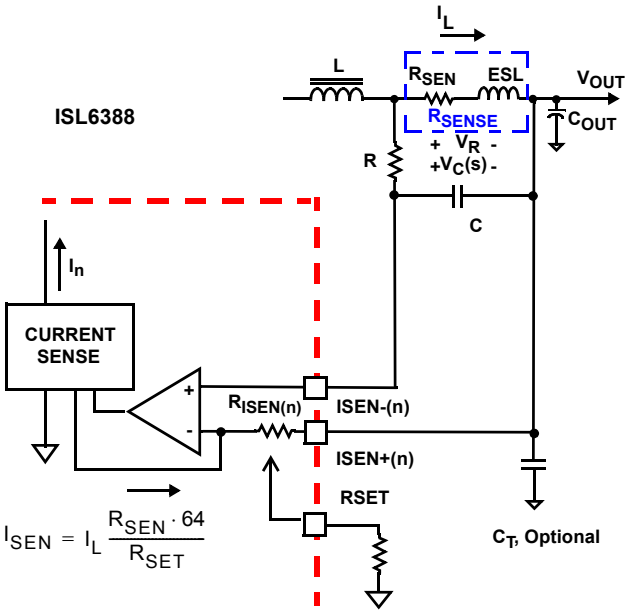


FIGURE 5. SENSE RESISTOR IN SERIES WITH INDUCTORS

If the R-C network components are selected such that the RC time constant matches the ESL-R_{SEN} time constant ($R*C = ESL/R_{SEN}$), the voltage across the capacitor V_C is equal to the voltage drop across the R_{SEN}, i.e., proportional to the channel-current. As an example, a typical 1mΩ sense resistor can use R = 348 and C = 820pF for the matching. Figures 6 and 7 show the sensed waveforms with and without matching RC when using resistive sense.

FIGURE 6. VOLTAGE ACROSS R WITHOUT RC

FIGURE 7. VOLTAGE ACROSS C WITH MATCHING RC

Equation 9 shows that the ratio of the channel-current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the R_{ISEN}.

$$I_{SEN} = I_L \cdot \frac{R_{SEN}}{R_{ISEN}} = I_L \frac{R_{SEN} \cdot 64}{R_{SET}} \quad \text{(EQ. 9)}$$

However, the R_{ISEN} resistor of each channel is integrated, while its value is determined by the R_{SET} resistor. The RSET resistor value can be from 3.84kΩ to 60.4kΩ and is 64x of the required I_{SEN} resistor value. Therefore, the current sense gain resistor (Integrated R_{ISEN}) value can be effectively set at 60Ω to 943Ω.

The inductor DCR value will increase as the temperature increases. Therefore, the sensed current will increase as the temperature of the current sense element increases. In order to compensate the temperature effect on the sensed current signal, a Negative Temperature Coefficient (NTC) resistor can be used for thermal compensation, or the integrated temperature compensation function of ISL6388 should be utilized. The integrated temperature compensation function is described in “Temperature Compensation” on page 30.

Decoupling capacitor (C_T) on ISEN[6:1]- pins are optional and might be required for long sense traces and a poor layout.

L/DCR OR ESL/R_{SEN} MATCHING

Assuming the compensator design is correct, Figure 8 shows the expected load transient response waveforms if L/DCR or ESL/R_{SEN} is matching the R-C time constant. When the load current I_{OUT} has a square change, the output voltage V_{OUT} also has a square response, except for the overshoot at load release. However, there is always some PCB contact impedance of current sensing components between the two current sensing points; it hardly accounts into the L/DCR or ESL/R_{SEN} matching calculation. Fine tuning the matching is necessarily done in the board level to improve overall transient performance and system reliability.

If the R-C timing constant is too large or too small, $V_C(s)$ will not accurately represent real-time $I_{OUT}(s)$ and will worsen the transient response. Figure 9 shows the load transient response when the R-C timing constant is too small. V_{OUT} will sag excessively upon load insertion and may create a system failure or early overcurrent trip. Figure 10 shows the transient response when the R-C timing constant is too large. The V_{OUT} is sluggish in drooping to its final value. There will be excessive overshoot if load insertion occurs during this time, which may potentially hurt the CPU reliability.

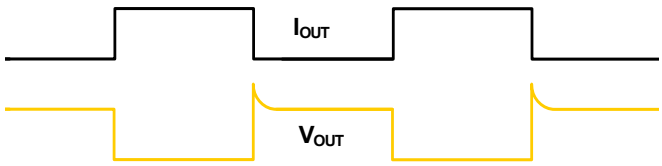


FIGURE 8. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

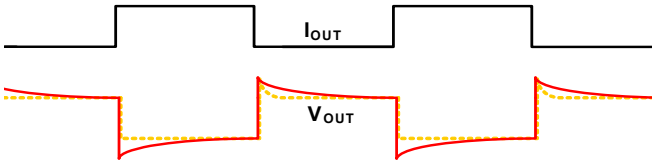


FIGURE 9. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO SMALL

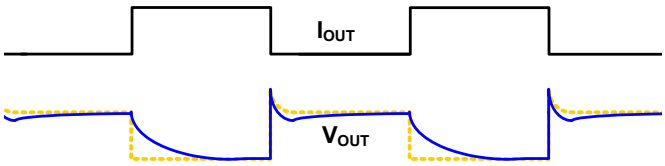


FIGURE 10. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO LARGE

R_{SET} AND L/DCR MATCHING FOR COUPLED INDUCTOR

The current sense circuitry operates in a very similar manner for negative current feedback, where inductor current is flowing from the output of the regulator to the PHASE node, opposite of flow pictured in Figures 4 and 5. However, the range of proper operation with negative current sensing has a limitation. The worst-case peak-to-peak inductor ripple current should be kept less than 80% of the OCP trip point (~80µA). Care should be taken to avoid operation with negative current feedback exceeding this threshold, as this may lead to momentary loss of current balance between phases and disruption of normal circuit operation. Note that the negative current can especially affect coupled inductor designs, where the effective inductance is the leakage between the two channels, much lower than the specified mutual inductance (LM) and self inductance (L). To limit the impact, a higher RSET value (1.5x to 2x) is often used to reduce the effective negative current seen by the controller in coupled inductor designs. Refer to Intersil's application note, AN1268 for detailed coupled inductor discussion and ripple current calculation.

As explained in application note, AN1268, the leakage inductance (not self inductance or mutual inductance) of the coupled inductor should be used as the inductance in the time constant calculation. Therefore, the leakage, self, and mutual inductance should be well controlled for a good coupled inductor design.

Channel-Current Balance

The sensed current I_n from each active channel is summed together and divided by the number of active channels. The resulting average current I_{AVG} provides a measure of the total load current. Channel-current balance is achieved by comparing the sensed current of each channel to the average current to make an appropriate adjustment to the PWM duty cycle of each channel with Intersil's patented current-balance method.

Channel-current balance is essential in achieving the thermal advantage of multiphase operation. With good current balance, the power loss is equally dissipated over multiple devices and a greater area. The ISL6388 can adjust the thermal/current balance of the VR via registers F7 to FC.

Voltage Regulation (VR12 and VR12.5 Mode)

The compensation network shown in Figure 11 assures that the steady-state error in the output voltage is limited only to the error in the reference voltage (DAC and OFFSET) and droop current source, remote sense, and error amplifier.

The sensed average current I_{DROOP} is tied to FB internally and will develop a voltage drop across the resistor between FB and V_{OUT} for droop control. This current can be disconnected from the FB node via PMBus for non-droop applications.

The output of the error amplifier, V_{COMP}, is compared to the internal sawtooth waveforms to generate the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage.

For remote sensing, connect the microprocessor sensing pins to the non-inverting input, VSEN, and inverting input, RGND, of the error amplifier. This configuration effectively removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point.

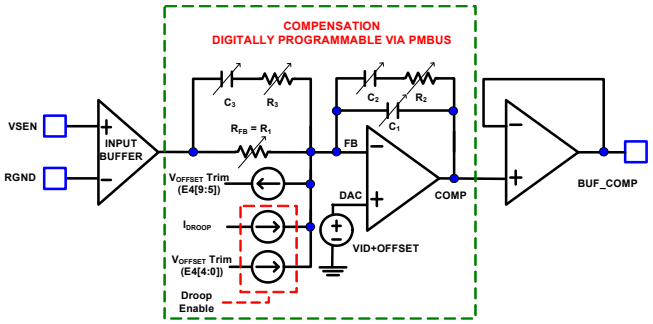


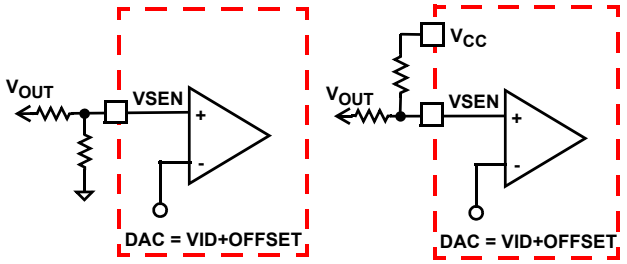
FIGURE 11. OUTPUT VOLTAGE AND LOAD-LINE REGULATION

A digital-to-analog converter (DAC) generates a reference voltage, which is programmable via SVID bus. The DAC decodes the SVID set command into one of the discrete voltages shown in Table 5. In addition, the output voltage can be margined in ±5mV step between -640mV and 635mV for VR12 mode, ±10mV step between -1280mV and 1270mV for VR12.5 mode, as shown in Table 5. For a finer than 5mV or 10mV offset, a large ratio resistor divider can be placed on the VSEN pin between the output and GND for positive offset or V_{CC} for negative offset, as in Figure 12. The VR operational mode is programmed by the "VRSEL_ADDR" pin. Table 4 shows the difference between VR12 and VR12.5 modes. VOUT_MAX and V_{BOOT} registers must be programmed accordingly to support each mode, otherwise, the VR might NOT power-up correctly.

TABLE 4. VR12 vs VR12.5

MODE (VRSEL)	DAC RESOLUTION (mV)	MAXIMUM DAC (V)	VOUT_MAX (24h)	MAXIMUM V_{BOOT} ("BT" pin)	MAXIMUM V_{BOOT} (E6)
VR12	5	2.155	Table 19	1.50	1.52
VR12.5	10	3.011	Table 5 Follow DAC	3.00	3.04

Furthermore, the PMBus register (E4h[9:5]) can program the additional droop current (range from -4µA to 3.75µA) into R1 for DC offset calibration; a negative current will yield a negative offset, while a positive current will yield a positive offset: OFFSET = R1* I(E4[9:5]). In droop applications, E4[4:0] can add current out of IMON pin and droop current through R1 simultaneously (the negative current yields positive offset, and vice versa).



A. V_{OUT} HIGHER THAN DAC B. V_{OUT} LOWER THAN DAC

FIGURE 12. EXTERNAL PROGRAMMABLE REGULATION

TABLE 5. VR12/VR12.5 VID 8-BIT

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
00000000	0	OFF	OFF	0	0
00000001	1	0.250	0.500	5	10
00000010	2	0.255	0.510	10	20
00000011	3	0.260	0.520	15	30
00000100	4	0.265	0.530	20	40
00000101	5	0.270	0.540	25	50
00000110	6	0.275	0.550	30	60
00000111	7	0.280	0.560	35	70
00001000	8	0.285	0.570	40	80
00001001	9	0.290	0.580	45	90
00001010	A	0.295	0.590	50	100
00001011	B	0.300	0.600	55	110
00001100	C	0.305	0.610	60	120
00001101	D	0.310	0.620	65	130
00001110	E	0.315	0.630	70	140
00001111	F	0.320	0.640	75	150
00010000	10	0.325	0.650	80	160
00010001	11	0.330	0.660	85	170

TABLE 5. VR12/VR12.5 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
00010010	12	0.335	0.670	90	180
00010011	13	0.340	0.680	95	190
00010100	14	0.345	0.690	100	200
00010101	15	0.350	0.700	105	210
00010110	16	0.355	0.710	110	220
00010111	17	0.360	0.720	115	230
00011000	18	0.365	0.730	120	240
00011001	19	0.370	0.740	125	250
00011010	1A	0.375	0.750	130	260
00011011	1B	0.380	0.760	135	270
00011100	1C	0.385	0.770	140	280
00011101	1D	0.390	0.780	145	290
00011110	1E	0.395	0.790	150	300
00011111	1F	0.400	0.800	155	310
00100000	20	0.405	0.810	160	320
00100001	21	0.410	0.820	165	330
00100010	22	0.415	0.830	170	340
00100011	23	0.420	0.840	175	350
00100100	24	0.425	0.850	180	360
00100101	25	0.430	0.860	185	370
00100110	26	0.435	0.870	190	380
00100111	27	0.440	0.880	195	390
00101000	28	0.445	0.890	200	400
00101001	29	0.450	0.900	205	410
00101010	2A	0.455	0.910	210	420
00101011	2B	0.460	0.920	215	430
00101100	2C	0.465	0.930	220	440
00101101	2D	0.470	0.940	225	450
00101110	2E	0.475	0.950	230	460
00101111	2F	0.480	0.960	235	470
00110000	30	0.485	0.970	240	480
00110001	31	0.490	0.980	245	490
00110010	32	0.495	0.990	250	500
00110011	33	0.500	1.000	255	510
00110100	34	0.505	1.010	260	520
00110101	35	0.510	1.020	265	530
00110110	36	0.515	1.030	270	540
00110111	37	0.520	1.040	275	550
00111000	38	0.525	1.050	280	560
00111001	39	0.530	1.060	285	570

TABLE 5. VR12/VR12.5 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
00111010	3A	0.535	1.070	290	580
00111011	3B	0.540	1.080	295	590
00111100	3C	0.545	1.090	300	600
00111101	3D	0.550	1.100	305	610
00111110	3E	0.555	1.110	310	620
00111111	3F	0.560	1.120	315	630
01000000	40	0.565	1.130	320	640
01000001	41	0.570	1.140	325	650
01000010	42	0.575	1.150	330	660
01000011	43	0.580	1.160	335	670
01000100	44	0.585	1.170	340	680
01000101	45	0.590	1.180	345	690
01000110	46	0.595	1.190	350	700
01000111	47	0.600	1.200	355	710
01001000	48	0.605	1.210	360	720
01001001	49	0.610	1.220	365	730
01001010	4A	0.615	1.230	370	740
01001011	4B	0.620	1.240	375	750
01001100	4C	0.625	1.250	380	760
01001101	4D	0.630	1.260	385	770
01001110	4E	0.635	1.270	390	780
01001111	4F	0.640	1.280	395	790
01010000	50	0.645	1.290	400	800
01010001	51	0.650	1.300	405	810
01010010	52	0.655	1.310	410	820
01010011	53	0.660	1.320	415	830
01010100	54	0.665	1.330	420	840
01010101	55	0.670	1.340	425	850
01010110	56	0.675	1.350	430	860
01010111	57	0.680	1.360	435	870
01011000	58	0.685	1.370	440	880
01011001	59	0.690	1.380	445	890
01011010	5A	0.695	1.390	450	900
01011011	5B	0.700	1.400	455	910
01011100	5C	0.705	1.410	460	920
01011101	5D	0.710	1.420	465	930
01011110	5E	0.715	1.430	470	940
01011111	5F	0.720	1.440	475	950
01100000	60	0.725	1.450	480	960
01100001	61	0.730	1.460	485	970

TABLE 5. VR12/VR12.5 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
01100010	62	0.735	1.470	490	980
01100011	63	0.740	1.480	495	990
01100100	64	0.745	1.490	500	1000
01100101	65	0.750	1.500	505	1010
01100110	66	0.755	1.510	510	1020
01100111	67	0.760	1.520	515	1030
01101000	68	0.765	1.530	520	1040
01101001	69	0.770	1.540	525	1050
01101010	6A	0.775	1.550	530	1060
01101011	6B	0.780	1.560	535	1070
01101100	6C	0.785	1.570	540	1080
01101101	6D	0.790	1.580	545	1090
01101110	6E	0.795	1.590	550	1100
01101111	6F	0.800	1.600	555	1110
01110000	70	0.805	1.610	560	1120
01110001	71	0.810	1.620	565	1130
01110010	72	0.815	1.630	570	1140
01110011	73	0.820	1.640	575	1150
01110100	74	0.825	1.650	580	1160
01110101	75	0.830	1.660	585	1170
01110110	76	0.835	1.670	590	1180
01110111	77	0.840	1.680	595	1190
01111000	78	0.845	1.690	600	1200
01111001	79	0.850	1.700	605	1210
01111010	7A	0.855	1.710	610	1220
01111011	7B	0.860	1.720	615	1230
01111100	7C	0.865	1.730	620	1240
01111101	7D	0.870	1.740	625	1250
01111110	7E	0.875	1.750	630	1260
01111111	7F	0.880	1.760	635	1270
10000000	80	0.885	1.770	-640	-1280
10000001	81	0.890	1.780	-635	-1270
10000010	82	0.895	1.790	-630	-1260
10000011	83	0.900	1.800	-625	-1250
10000100	84	0.905	1.810	-620	-1240
10000101	85	0.910	1.820	-615	-1230
10000110	86	0.915	1.830	-610	-1220
10000111	87	0.920	1.840	-605	-1210
10001000	88	0.925	1.850	-600	-1200
10001001	89	0.930	1.860	-595	-1190

TABLE 5. VR12/VR12.5 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
10001010	8A	0.935	1.870	-590	-1180
10001011	8B	0.940	1.880	-585	-1170
10001100	8C	0.945	1.890	-580	-1160
10001101	8D	0.950	1.900	-575	-1150
10001110	8E	0.955	1.910	-570	-1140
10001111	8F	0.960	1.920	-565	-1130
10010000	90	0.965	1.930	-560	-1120
10010001	91	0.970	1.940	-555	-1110
10010010	92	0.975	1.950	-550	-1100
10010011	93	0.980	1.960	-545	-1090
10010100	94	0.985	1.970	-540	-1080
10010101	95	0.990	1.980	-535	-1070
10010110	96	0.995	1.990	-530	-1060
10010111	97	1.000	2.000	-525	-1050
10011000	98	1.005	2.010	-520	-1040
10011001	99	1.010	2.020	-515	-1030
10011010	9A	1.015	2.030	-510	-1020
10011011	9B	1.020	2.040	-505	-1010
10011100	9C	1.025	2.050	-500	-1000
10011101	9D	1.030	2.060	-495	-990
10011110	9E	1.035	2.070	-490	-980
10011111	9F	1.040	2.080	-485	-970
10100000	A0	1.045	2.090	-480	-960
10100001	A1	1.050	2.100	-475	-950
10100010	A2	1.055	2.110	-470	-940
10100011	A3	1.060	2.120	-465	-930
10100100	A4	1.065	2.130	-460	-920
10100101	A5	1.070	2.140	-455	-910
10100110	A6	1.075	2.150	-450	-900
10100111	A7	1.080	2.160	-445	-890
10101000	A8	1.085	2.170	-440	-880
10101001	A9	1.090	2.180	-435	-870
10101010	AA	1.095	2.190	-430	-860
10101011	AB	1.100	2.200	-425	-850
10101100	AC	1.105	2.210	-420	-840
10101101	AD	1.110	2.220	-415	-830
10101110	AE	1.115	2.230	-410	-820
10101111	AF	1.120	2.240	-405	-810
10110000	B0	1.125	2.250	-400	-800
10110001	B1	1.130	2.260	-395	-790

TABLE 5. VR12/VR12.5 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
10110010	B2	1.135	2.270	-390	-780
10110011	B3	1.140	2.280	-385	-770
10110100	B4	1.145	2.290	-380	-760
10110101	B5	1.150	2.300	-375	-750
10110110	B6	1.155	2.310	-370	-740
10110111	B7	1.160	2.320	-365	-730
10111000	B8	1.165	2.330	-360	-720
10111001	B9	1.170	2.340	-355	-710
10111010	BA	1.175	2.350	-350	-700
10111011	BB	1.180	2.360	-345	-690
10111100	BC	1.185	2.370	-340	-680
10111101	BD	1.190	2.380	-335	-670
10111110	BE	1.195	2.390	-330	-660
10111111	BF	1.200	2.400	-325	-650
11000000	C0	1.205	2.410	-320	-640
11000001	C1	1.210	2.420	-315	-630
11000010	C2	1.215	2.430	-310	-620
11000011	C3	1.220	2.440	-305	-610
11000100	C4	1.225	2.450	-300	-600
11000101	C5	1.230	2.460	-295	-590
11000110	C6	1.235	2.470	-290	-580
11000111	C7	1.240	2.480	-285	-570
11001000	C8	1.245	2.490	-280	-560
11001001	C9	1.250	2.500	-275	-550
11001010	CA	1.255	2.510	-270	-540
11001011	CB	1.260	2.520	-265	-530
11001100	CC	1.265	2.530	-260	-520
11001101	CD	1.270	2.540	-255	-510
11001110	CE	1.275	2.550	-250	-500
11001111	CF	1.280	2.560	-245	-490
11010000	D0	1.285	2.570	-240	-480
11010001	D1	1.290	2.580	-235	-470
11010010	D2	1.295	2.590	-230	-460
11010011	D3	1.300	2.600	-225	-450
11010100	D4	1.305	2.610	-220	-440
11010101	D5	1.310	2.620	-215	-430
11010110	D6	1.315	2.630	-210	-420
11010111	D7	1.320	2.640	-205	-410
11011000	D8	1.325	2.650	-200	-400
11011001	D9	1.330	2.660	-195	-390

TABLE 5. VR12/VR12.5 VID 8-BIT (Continued)

BINARY CODE	HEX CODE	VR12 VID (V)	VR12.5 VID (V)	VR12 OFFSET (mV)	VR12.5 OFFSET (mV)
11011010	DA	1.335	2.670	-190	-380
11011011	DB	1.340	2.680	-185	-370
11011100	DC	1.345	2.690	-180	-360
11011101	DD	1.350	2.700	-175	-350
11011110	DE	1.355	2.710	-170	-340
11011111	DF	1.360	2.720	-165	-330
11100000	E0	1.365	2.730	-160	-320
11100001	E1	1.370	2.740	-155	-310
11100010	E2	1.375	2.750	-150	-300
11100011	E3	1.380	2.760	-145	-290
11100100	E4	1.385	2.770	-140	-280
11100101	E5	1.390	2.780	-135	-270
11100110	E6	1.395	2.790	-130	-260
11100111	E7	1.400	2.800	-125	-250
11101000	E8	1.405	2.810	-120	-240
11101001	E9	1.410	2.820	-115	-230
11101010	EA	1.415	2.830	-110	-220
11101011	EB	1.420	2.840	-105	-210
11101100	EC	1.425	2.850	-100	-200
11101101	ED	1.430	2.860	-95	-190
11101110	EE	1.435	2.870	-90	-180
11101111	EF	1.440	2.880	-85	-170
11110000	F0	1.445	2.890	-80	-160
11110001	F1	1.450	2.900	-75	-150
11110010	F2	1.455	2.910	-70	-140
11110011	F3	1.460	2.920	-65	-130
11110100	F4	1.465	2.930	-60	-120
11110101	F5	1.470	2.940	-55	-110
11110110	F6	1.475	2.950	-50	-100
11110111	F7	1.480	2.960	-45	-90
11111000	F8	1.485	2.970	-40	-80
11111001	F9	1.490	2.980	-35	-70
11111010	FA	1.495	2.990	-30	-60
11111011	FB	1.500	3.000	-25	-50
11111100	FC	1.505	3.010	-20	-40
11111101	FD	1.510	3.020	-15	-30
11111110	FE	1.515	3.030	-10	-20
11111111	FF	1.520	3.040	-5	-10

Load-Line Regulation

Some microprocessor manufacturers require a precisely controlled output resistance. This dependence of output voltage on load current is often termed “droop” or “load-line” regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction, which works to achieve the load-line regulation required by these manufacturers.

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output voltage spike that results from fast load current demand changes.

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 11, a current proportional to the average current of all active channels, I_{AVG}, flows from FB through a load-line regulation resistor R_{FB}, i.e., R_1. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined, as shown in Equation 10:

$$V_{DROOP} = I_{AVG} \cdot R_{FB} \quad \text{(EQ. 10)}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP}. The output voltage as a function of load current is derived by combining Equation 10 with the appropriate sample current expression defined by the current sense method employed, as shown in Equation 11:

$$V_{OUT} = V_{REF} - \left(\frac{I_{LOAD}}{N} \frac{R_X}{R_{ISEN}} R_{FB} \right) \quad \text{(EQ. 11)}$$

where V_{REF} is the reference voltage (DAC), I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, and R_{FB} is the feedback resistor, N is the active channel number, and R_X is the DCR, or R_{SENSE} depending on the sensing method.

Therefore, the equivalent loadline impedance, i.e. Droop impedance, is equal to Equation 12:

$$R_{LL} = \frac{R_{FB}}{N} \frac{R_X}{R_{ISEN}} \quad \text{(EQ. 12)}$$

The major regulation error comes from the current sensing elements. To improve load-line regulation accuracy, a tight DCR tolerance of inductor or a precision sensing resistor should be considered.

In addition, the overall load-line can be programmed to fit the application needed by the PMBus registers: B0h[7:0] for load-line and E4h[9:5] for DC offset. Curve 3 shown in Figure 13, makes a steeper load-line than the target to fully utilize the total tolerance band, reduce the output capacitor count and cost.

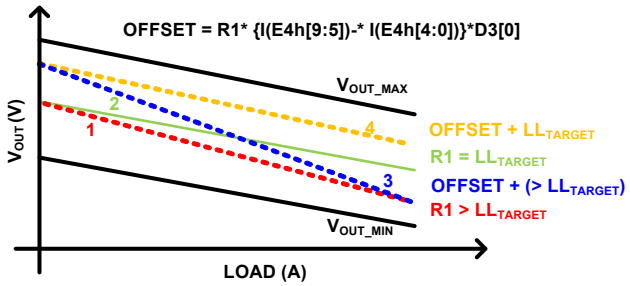


FIGURE 13. PROGRAMMABLE LOAD-LINE REGULATION

Dynamic VID

Modern microprocessors need to make changes to their voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID during regulator operation. The power management solution is required to monitor the DAC and respond to on-the-fly VID changes in a controlled manner. Supervising the safe output voltage transition within the DAC range of the processor without discontinuity or disruption is a necessary function of the core-voltage regulator.

Sixteen different slew rates can be selected during Dynamic VID (DVID) transition for VR, but during VR soft-start, the setVID SLOW rate is defaulted.

TABLE 6. SLEW RATE OPTIONS

FDVID F6h[4:0]	SetVID FAST (MINIMUM RATE) (mV/µs)	SVID 24h (SR_FAST)	SetVID SLOW (MINIMUM RATE) (mV/µs)	SVID 23h (SR_SLOW) PMBus DVID
0h	1.25	01h	0.315	00h
1h	2.5	02h	0.625	00h
2h	5	05h	1.25	01h
3h	10	0Ah	2.5	02h
4h	11.42	0Eh	2.85	02h
5h	12.3	11h	3.07	03h
6h	13.33	14h	3.33	03h
7h	14.54	0Eh	3.63	03h
8h	16.00	10h	4.0	04h
9h	17.77	11h	4.44	04h
Ah	20	14h	5.0	05h
Bh	22.85	16h	5.6	05h
Ch	26.66	1Ah	6.66	06h
Dh	32	20h	8.0	08h
Eh	40	28h	10	0A
Fh	53	35h	13.25	0Dh

During dynamic VID transition and VID step up, the overcurrent trip point increases by 140% to avoid falsely triggering OCP circuits, while the overvoltage trip point will follow the DAC+OVP level, programmable via PMBus (D8h[2:0]). If the dynamic VID occurs at PSI1/2/3/Decay (lower power state) asserted, the system should exit to PSI0 (full power state) and complete the transition, and will not resume the lowe power state operation unless the low power mode command is asserted again.

In addition to ramping down the output voltage with a controlled rate as previously described, VR can be programmed into decay mode via SVID's setDecay command. Whenever the Decay command is received, the VR will enter PSI2 mode. The VR will be in single-phase operation. If the DE register is selected to be "Enabled", the VR will operate in diode emulation mode and drop to the target voltage at a decay rate determined by the load impedance and output capacitive bank. The decay rate will be limited to 2.5mV/µs rate setting. If the "DE" register is selected to be "Disabled", then the VR will drop at 2.5mV/µs rate setting.

Operation Initialization

Prior to converter initialization, proper conditions must exist on the enable inputs and V_{CC}. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, VR_RDY asserts logic high.

Enable and Disable

In shutdown mode, the PWM outputs are held in a high-impedance state (or pulled to 28% of V_{CC}, PWMTRI = 3.3V, 40% of V_{CC}, PWMTRI = 5.0V) to assure the drivers remain off. The following input conditions must be met before the ISL6388 is released from shutdown mode.

1. The bias voltage applied at V_{CC} must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6388 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, ISL6388 will not inadvertently turn off unless the bias voltage drops substantially (see beginning of "Electrical Specifications" on page 10).
2. The ISL6388 features an enable input (EN_PWR_CFP) for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6388 in shutdown until the voltage at EN_PWR_CFP rises above 0.85V. The enable comparator has about 100mV of hysteresis to prevent bounce. It is important that the drivers reach their POR level before the ISL6388 becomes enabled. The schematic in Figure 14 demonstrates sequencing the ISL6388 with ISL99140 DrMOS and the ISL66xx family of Intersil MOSFET drivers.
3. The voltage on TM_EN_OTP must be higher than 1.05V (typically) to enable the controller. This pin is typically connected to an open drain signal. However, since the TM_EN_OTP pin is also used for thermal monitoring, it will assert SM_PMALERT# pin low due to thermal alert prior to start-up, therefore, it needs to use CLEAR_FAULT (03h) command to clear the SM_PMALERT# pin and STATUS_BYTE (78h) after power-up. There is no effect on normal operation if SM_PMALERT# and STATUS_BYTE are not used.

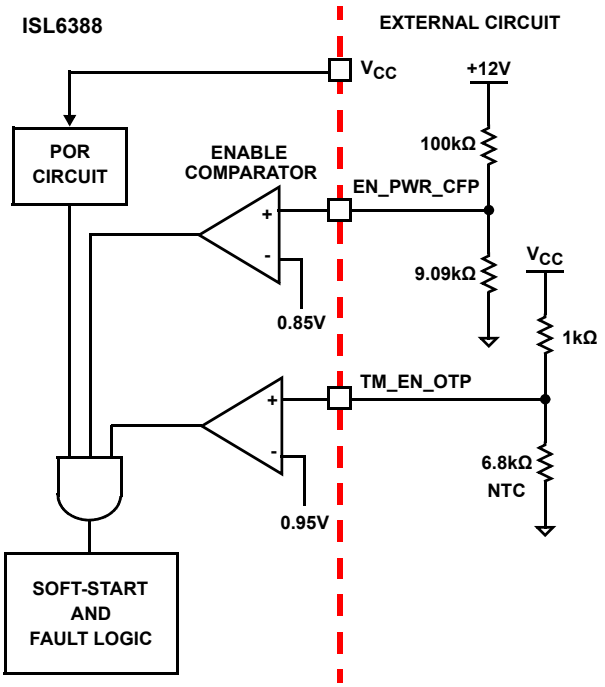


FIGURE 14. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

When all conditions previously mentioned are satisfied, the ISL6388 begins the soft-start and ramps the output voltage to the Boot Voltage set by hard-wired "BT" register or first setVID command if boot voltage set to zero volts. After remaining at the boot voltage for some time, ISL6388 receives the VID code via SVID bus. If the VID code is valid, ISL6388 will regulate the output to the final VID setting. If the VID code is "OFF" code (0V), the ISL6388 will remain shutdown.

Soft-Start

The ISL6388 based VR has 4 periods during soft-start, as shown in Figure 15. After V_{CC}, TM_EN_OTP and EN_PWR_CFP reach their POR/enable thresholds, the controller will have a fixed delay period t_{D1}. After this delay period, the VR will begin first soft-start ramp until the output voltage reaches the V_{BOOT} voltage at a fixed slew rate, one-quarter of setVID FAST rate as in Table 6. Then, the controller will regulate the VR voltage at V_{BOOT} for another period t_{D3} until SVID sends a new VID command. If the VID code is valid, ISL6388 will initiate the second soft-start ramp at a slew rate, set by SetDVID FAST or SLOW command in Table 6, until the voltage reaches the new VID voltage.

The soft-start time is the sum of the 4 periods, as shown in Equation 13.

$$t_{SS} = t_{D1} + t_{D2} + t_{D3} + t_{D4} \quad \text{(EQ. 13)}$$

t_{D1} is a fixed delay with the typical value as 20µs. t_{D3} is determined by the time to obtain a new valid VID voltage from SVID bus. If the VID is valid before the output reaches the boot voltage, the output will turn around to respond to the new VID code.

During t_{D2} and t_{D4}, ISL6388 digitally controls the DAC voltage change. The soft-start ramp time t_{D2} and t_{D4} can be calculated based on Equations 14 and 15:

$$t_{D2} = \frac{V_{BOOT}}{\text{SetVID SLOW RATE}}(\mu s) \quad \text{(EQ. 14)}$$

$$t_{D4} = \frac{V_{VID} - V_{BOOT}}{\text{SetVID RATE}}(\mu s) \quad \text{(EQ. 15)}$$

For example, when the V_{BOOT} is set at 1.1V and setVID rate is set at 10mV/µs, the first soft-start ramp time t_{D2} will be around 440µs and the second soft-start ramp time t_{D4} will be at maximum of 40µs if an setVID command for 1.5V is received after t_{D3}. However, if the V_{BOOT} is set at 0V, the first setVID command is for 1.5V, then t_{D2} will be around 150µs.

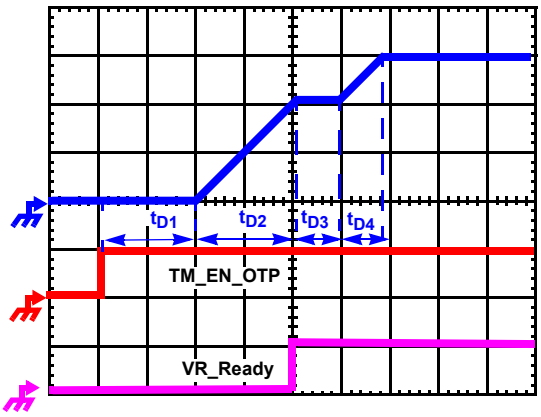


FIGURE 15. SOFT-START WAVEFORMS

Current Sense Output

The current flowing out of the IMON pin is equal to the sensed average current inside the ISL6388. In typical applications, a resistor is placed from the IMON pin to GND to generate a voltage, which is proportional to the load current and the resistor value, as shown in Equation 16:

$$V_{IMON} = \frac{R_{IMON}}{N}\frac{R_X}{R_{ISEN}}I_{LOAD} \quad \text{(EQ. 16)}$$

where V_{IMON} is the voltage at the IMON pin, R_{IMON} is the resistor between the IMON pin and GND, I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, and R_X is the DC resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method.

The resistor from the IMON pin to GND should be chosen to ensure that the voltage at the IMON pin is typically 2.5V at the maximum load current (not OCP level), corresponding to the I_{CCMAX} register. The IMON voltage is linearly digitized every 88µs and stored in the I_{OUT} register (15h). When the IMON voltage reaches 2.5V or higher, the digitized I_{OUT} reads the maximum and the SVALERT# and SM_PMALERT# pins are pulled low to alarm the CPU. SVID digital I_{OUT} (15h) will read lower than FFh if the negative OFFSET is set. i.e., it will read FBh if -4h offset is selected; IMAX register (21h in SVID, programmable by EAh) should set higher than the target (no less than +4A) when negative offset is needed.

A small capacitor can be placed between the IMON pin and GND to reduce the noise impact and provide averaging. The typical time constant is <200µs for VR12.5 Server Core (i.e., ~ 4.7nF for

a 30kΩ R_{IMON}) and 1ms to 2ms for Desktop Core applications. If this pin is not used, tie it to GND.

$$R_{IMON} = \frac{2.5V\ R_{ISEN}}{R_X}\ \frac{N}{I_{CC\_MAX\_21h}} \quad \text{(EQ. 17)}$$

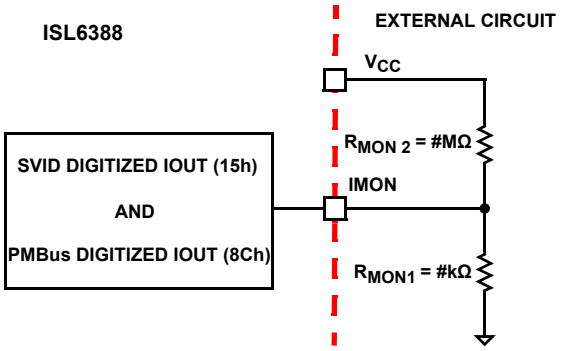


FIGURE 16. IMON NO LOAD OFFSET CALIBRATION

To deal with layout and design variation of different platforms, the ISL6388 is intentionally trimmed to the negative range at no load, thus, an offset can easily be added to calibrate the digitized IMON reading (15h in SVID and 8Ch in PMBus), whenever needed by PMBus (E4h) or the external pull-up resistor in Figure 16. Hence, the slope on the IMON pin is set by the equivalent impedance of $R_{MON1}//R_{MON2} = R_{IMON}$. Additional offset can be added by IOUT_CAL_OFFSET (E5h).

$$R_{MON2} = \frac{V_{CC}\ R_{IMON}}{V_{IMON\_OFFSET\_DESIRED}}$$

$$R_{MON1} = \frac{R_{IMON2}\ R_{IMON}}{R_{IMON2} - R_{IMON}} \quad \text{(EQ. 18)}$$

In addition, if the IMON pin voltage is higher than 3.0V, overcurrent shutdown will be triggered, in as described in "Overcurrent Protection" on page 28.

Fault Monitoring and Protection

The ISL6388 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power-good indicator (VR_RDY) is provided for linking to external system monitors. The schematic in Figure 17 outlines the interaction between the fault monitors and the VR_RDY signal.

VR_Ready Signal

The VR_RDY pin is an open-drain logic output which indicates that the soft-start period is complete and the output, voltage is within the regulated range. The VR_RDY is pulled low during shutdown and releases high after a successful soft-start. The VR_RDY will be pulled low when fault (OCP, OTP, UVP, or OVP) condition is detected, or the controller is disabled by a reset from EN_PWR_CFP, TM_EN_OTP, POR, or VID OFF-code. If the Multi_VR_config register is set to 01h, then the VR_Ready line will stay high when receiving a 00h VID code after the first soft-start. The defaulted Multi_VR_config is 00h.

Overvoltage Protection

Regardless of the VR being enabled or not, the ISL6388 overvoltage protection (OVP) circuit will be active after its POR. The OVP thresholds are different under different operation conditions. When VR is not enabled and during the soft-start intervals t_{D1}, the OVP threshold is programmable via PMBus (D8h[4:3]). Once the VR completes the soft-start, the OVP trip point will change to a tracking level of DAC+OVP, programmable via PMBus (D8h[2:0]).

Two actions are taken by the ISL6388 to protect the microprocessor load when an overvoltage condition occurs.

At the inception of an overvoltage event, all PWM outputs are commanded low instantly. This causes the Intersil drivers to turn on the lower MOSFETs and pull the output voltage below a level to avoid damaging the load. When the output voltage falls below the DAC plus 100mV, PWM signals enter a high-impedance state. The Intersil drivers respond to the high-impedance input by turning off both upper and lower MOSFETs. If the overvoltage condition reoccurs, the ISL6388 will again command the lower MOSFETs to turn on. The ISL6388 will continue to protect the load in this fashion as long as the overvoltage condition occurs.

Once an overvoltage condition is detected, the VR ceases the normal PWM operation and pulls its VR_Ready low until the ISL6388 is reset. Cycling the voltage V_{CC} below the POR-falling threshold will reset the controller. Cycling EN_PWR_CFP or TM_EN_OTP will NOT reset the controller.

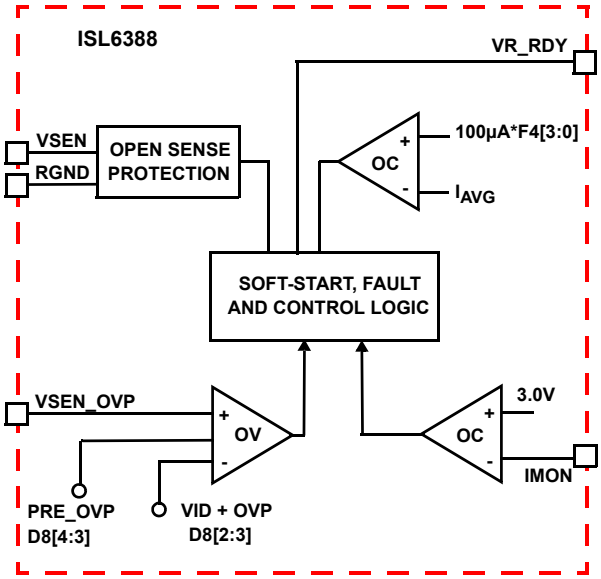
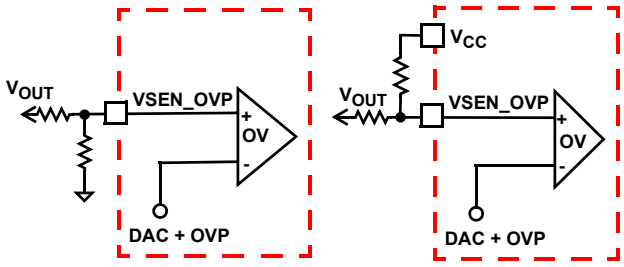


FIGURE 17. VR_RDY AND PROTECTION CIRCUITRY

In addition, the ISL6388 features open sensing protection to detect an open of the output voltage sensing as an OVP event, which suspends the controller operation. Without this protection, the VR can regulate up to maximum duty cycle and damage the load and power trains when the output sensing is broken open. Furthermore, since the regulation loop is sensed via the VSEN pin and the OVP is sensed via the VSEN_OVP pin, they are independent paths to keep output within target and below OVP level, respectively. Thus, the ISL6388 protects against a single point of failure.

Furthermore, since the regulation loop (VSEN pin) and the OVP sense (VSEN_OVP) are separated paths, the OVP level can be programmed higher or lower than the target, as in Figure 18. The OVP level cannot be scaled too close to DAC to ensure that the OVP is not triggered during transient response and start-up.

In addition, the ISL6388 also provides early OVP warning; when it is triggered, it asserts STATUS_WORD (79h Upper Byte, Bit7) and SM_PMALERT#. However It does not shutdown the system, assert STATUS_BYTE, or pull VR_RDY low. Disregard this if both STATUS_WORD and SM_PMALERT# are not used or disable OVP Warning as needed via DFh.



A. INCREASED OVP B. REDUCED OVP

FIGURE 18. EXTERNAL PROGRAMMABLE OVP

Overcurrent Protection

The ISL6388 has two levels of overcurrent protection. Each phase is protected from a sustained overcurrent condition by limiting its peak current, while the combined phase currents are protected on an instantaneous basis.

For the individual channel overcurrent protection, the ISL6388 continuously compares the sensed peak current (~50ns filter) signal of each channel with the reference current (I_{CL}, typically 125µA, programmable via F4[5:3] and F3[2:0]). If one channel-current exceeds the reference current, the ISL6388 will pull PWM signal of this channel to low for the rest of the switching cycle. This PWM signal can be turned on the next cycle if the sensed channel-current is less than the reference current. The peak current limit of individual channels will only use cycle-by-cycle current limiting and will not trigger the converter to shut down.

In instantaneous protection mode, the ISL6388 utilizes the sensed average current I_{AVG} to detect an overcurrent condition. See “Current Sensing” on page 18 for more details on how the average current is measured. The average current is continually compared with a constant reference current (typically 100µA, programmable via F2[2:0]), as shown in Figure 17. Once the average current exceeds the reference current, a comparator triggers the converter to shut down. In addition, the current out of the IMON pin is equal to the sensed average current I_{AVG}. With a resistor from IMON to GND, the voltage at IMON will be proportional to the sensed average current and the resistor value. The ISL6388 continuously monitors the voltage at the IMON pin. If the voltage at the IMON pin is higher than 3.0V, a precision comparator triggers the overcurrent shutdown. Since the internal current comparator has wider tolerance than the voltage comparator, the IMON voltage comparator is the preferred one for OCP trip. Therefore, the resistor between IMON and GND can be scaled such that the overcurrent protection threshold is tripping lower than 100µA. For example, the overcurrent threshold for the sensed average current I_{AVG} can be set to 95µA by using a 31.5kΩ resistor from IMON to GND. Thus, the internal 100µA comparator might only be triggered at its lower corner. However, IMON OCP trip should NOT be too far away from I_{CL}, which is used for cycle-by-cycle protection and inductor saturation.

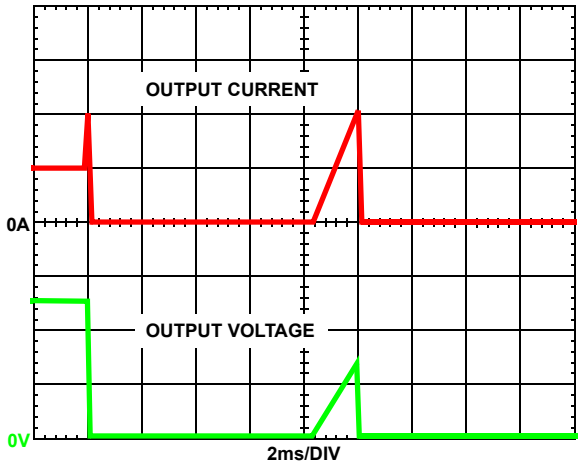


FIGURE 19. OVERCURRENT BEHAVIOR IN HICCUP MODE F_{SW} = 500kHz

At the beginning of overcurrent shutdown, the controller places all PWM signals in a high-impedance state, commanding the Intersil MOSFET driver ICs to turn off both upper and lower MOSFETs. The system remains in this state a period of 9ms. If the controller is still enabled at the end of this wait period, it will attempt a soft-start. If the fault remains, the trip-retry cycles will continue indefinitely (as shown in Figure 19) until either controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard during this kind of operation.

UnderVoltage Protection

When the output voltage drops below a level programmed by PMBus (E1[3:0]), the VR_RDY is pulled low. The controller can respond to UVP with two different options programmed by PMBus (E1[6]): 1) acts as a OCP event, hiccup the output with 9ms duration and pull VR_RDY low; or 2) acts like a PGOOD, pull VR_RDY low, monitor only. To avoid faulty triggering at transient/DVID events, the UVP delay is programmable by E1[5:4]. Furthermore, the UVP is not enabled during soft-start or SetVID/Decay to 0V and also can be disabled by DF[5]. The ISL6388 also provides early UVP warning; when it is triggered, it asserts STATUS_WORD (79h Upper Byte, Bit7) and SM_PMALERT#. However it does not shutdown the system, assert STATUS_BYTE or pull VR_RDY low. Disregard this if both STATUS_WORD and SM_PMALERT# are not used or disable UVP Warning as needed via DFh.

Thermal Monitoring (VR_HOT#)

VR_HOT# indicates the temperature status of the voltage regulator. VR_HOT# is an open-drain output, and an external pull-up resistor is required. This signal is valid only after the controller is enabled.

The VR_HOT# signal can be used to inform the system that the temperature of the voltage regulator is too high and the CPU should reduce its power consumption. The VR_HOT# signal may be tied to the CPU's PROC_HOT signal.

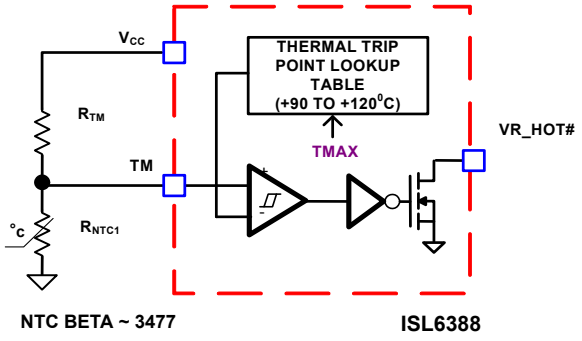


FIGURE 20. BLOCK DIAGRAM OF THERMAL MONITORING FUNCTION

The block diagram of thermal monitoring function is shown in Figure 20. One NTC resistor should be placed close to the respective power stage of the voltage regulator VR to sense the operational temperature, and pull-up resistors are needed to form the voltage dividers for the TM pins. As the temperature of the power stage increases, the resistance of the NTC will reduce, resulting in the reduced voltage at the TM pin. Figure 21 shows the TM voltage over the temperature for a typical design with a recommended 6.8kΩ NTC (P/N: NTHS0805N02N6801 from Vishay, b = 3477) and 1kΩ resistor R_{TM}. It is recommended to use those resistors for the accurate temperature compensation since the internal thermal digital code is developed based upon these two components. If a different value is used, the temperature coefficient must be close to 3477 and R_{TM} must be scaled accordingly. For instance, say NTC = 10kΩ (b = 3477), then R_{TM} should be 10kΩ/6.8kΩ*1kΩ = 1.47kΩ.

There is a comparator with hysteresis to compare the TM pin voltage to the threshold set by the TMAX register (programmable via PMBus E8[2:0]) for VR_HOT# signal. With TMAX set at +100°C, the VR_HOT# signal is pulled to GND when TM voltage is lower than 39.12% of V_{CC} voltage, and is open (pulled high through TM) when TM voltage increases to above 40.98% of V_{CC} voltage. The comparator trip point will be programmable by TMAX register. Figure 21 shows the operation of those signals.

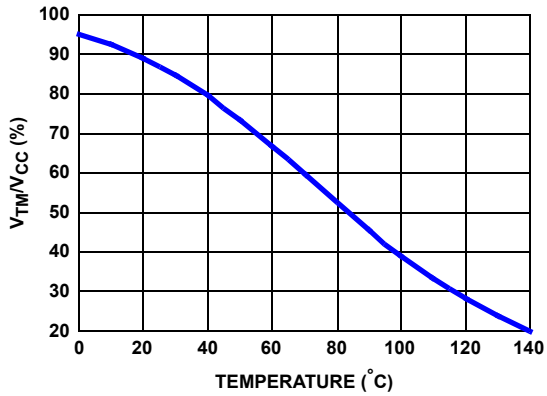


FIGURE 21. THE RATIO OF TM VOLTAGE TO NTC TEMPERATURE WITH RECOMMENDED PARTS

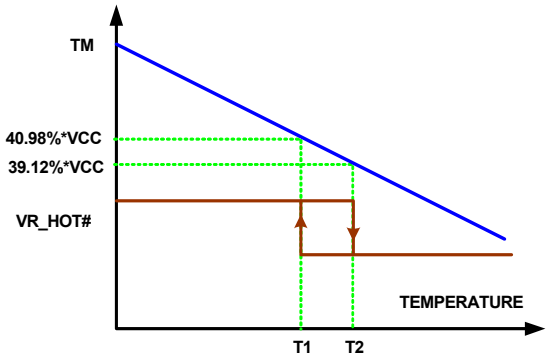


FIGURE 22. VR_HOT# SIGNAL (TMAX = 100°C) vs TM VOLTAGE

Based on the NTC temperature characteristics and the desired threshold of the VR_HOT# signal, the pull-up resistor R_{TM} of TM pin is given by Equation 19:

$$R_{TM} = 1.557 \times R_{NTC(T2)} \quad \text{(EQ. 19)}$$

$R_{NTC(T2)}$ is the NTC resistance at the VR_HOT# threshold temperature T2. The VR_HOT# is de-asserted at temperature T1, as shown in Table 7. The NTC directly senses the temperature of the PCB and not the exact temperature of the hottest component on the board due to airflow and varied thermal impedance. Therefore, the user should select a lower TMAX number, depending upon the mismatch between NTC and the hottest components, than such component to guarantee a safe operation.

TABLE 7. VR_HOT# TYPICAL TRIP POINT AND HYSTERESIS

TMAX (°C)	VR_HOT# LOW (°C; T2,%V_{CC})	VR_HOT# OPEN (°C; T1,%V_{CC})	HYSTERESIS (°C)
85	83.1; 48.94%	80.3; 51.04%	2.7
90	88.6; 45.52%	85.9; 47.56%	2.7
95	94.3; 42.26%	91.4; 44.20%	2.9
100	100.0; 39.12%	97.1; 40.98%	2.9
105	106.1; 36.14%	103.0; 37.92%	3.1
110	109.1; 33.32%	106.1; 35.00%	3.0
115	115.5; 30.68%	112.3; 32.24%	3.2
120	118.7; 28.24%	115.5; 29.7%	3.2

In addition, as the temperature increases, the voltage on the TM pin drops. The controller is disabled when the TM pin voltage drops below 0.95 (typically) and becomes active again when it is above 1.05V (typically).

Temperature Compensation

The ISL6388 supports inductor DCR sensing, or resistive sensing techniques. The inductor DCR has a positive temperature coefficient, which is about +0.385%/°C. Since the voltage across the inductor is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR.

In order to obtain the correct current information, there should be a way to correct the temperature impact on the current sense component.

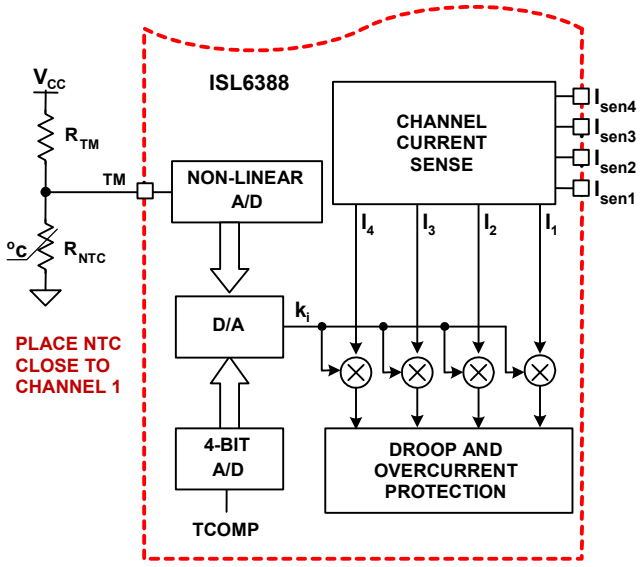


FIGURE 23. BLOCK DIAGRAM OF INTEGRATED TEMPERATURE COMPENSATION

The ISL6388 utilizes the voltage at the TM pin and "TCOMP" register to compensate the temperature impact on the sensed current. The block diagram of this function is shown in Figure 23.

When the NTC is placed close to the current sense component (inductor), the temperature of the NTC will track the temperature of the current sense component. Therefore, the TM voltage can be utilized to obtain the temperature of the current sense component. Since the NTC could pick up noise from phase node, a 0.1µF ceramic decoupling capacitor is recommended on the TM pin in close proximity to the controller.

Based on the V_{CC} voltage, the ISL6388 converts the TM pin voltage to a 6-bit TM digital signal for temperature compensation. With the non-linear A/D converter of ISL6388, the TM digital signal is proportional to the NTC temperature. For accurate temperature compensation, the ratio of the TM voltage to the NTC temperature of the practical design should be similar to that in Figure 21.

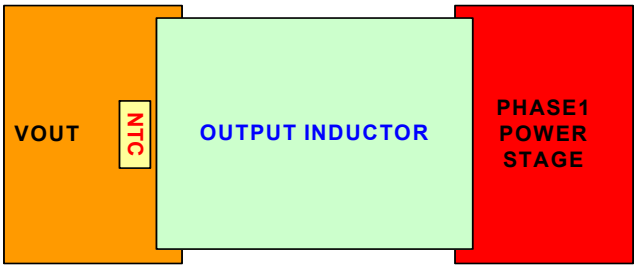


FIGURE 24. RECOMMENDED PLACEMENT OF NTC

Since the NTC attaches to the PCB, but not directly to the current sensing component, it inherits high thermal impedance between the NTC and the current sensing element. The "TCOMP" register values can be utilized to correct the temperature difference between NTC and the current sense component. Figure 24 shows that the NTC should be placed in proximity to the PSI channel and the output rail; DON'T place it close to the MOSFET side, which generates much more heat.

The ISL6388 multiplexes the "TCOMP" value with the TM digital signal to obtain the adjustment gain to compensate the temperature impact on the sensed channel-current. The compensated channel-current signal is used for droop and overcurrent protection functions.

TABLE 8. "TCOMP" VALUES

E9h	TCOMP (°C)	E9h	TCOMP (°C)
0h	OFF	8h	16
1h	-2.5	9h	18.9
2h	0	Ah	21.6
3h	2.5	Bh	24.3
4h	5	Ch	27
5h	7	Dh	29.7
6h	10	Eh	32.4
7h	13	Fh	35.1

When a different NTC type or different voltage divider is used for the TM function, the TCOMP voltage can also be used to compensate for the difference between the recommended TM voltage curve in Figure 21 and that of the actual design. If the same type NTC (β = 3477) but different value is used, the pull-up resistor needs to be scaled, as shown in Equation 20:

$$R_{TM} = \frac{1k\Omega \cdot R_{NTC\_NEW}}{6.8k\Omega} \quad \text{(EQ. 20)}$$

Below is the thermal compensation design procedure:

1. Properly choose the voltage divider for the TM pin to match the recommended curve in Figure 21.
2. Run the actual board under the full load and the desired cooling condition.
3. After the board reaches the thermal steady state, record the temperature (T_{CSC}) of the current sense component (inductor or R_{SENSE}) and the voltage at TM and V_{CC} pins.

4. Use Equation 21 to calculate the resistance of the NTC, and find out the corresponding NTC temperature T_{NTC} from the NTC datasheet or using Equation 22, where β is equal to 3477 for recommended NTC.

$$R_{NTC}(T_{NTC}) = \frac{V_{TM} \times R_{TM}}{V_{CC} - V_{TM}} \quad \text{(EQ. 21)}$$

$$T_{NTC} = \frac{\beta}{\ln\left(\frac{RTM}{R_{NTC}(T_{NTC})}\right) + \frac{\beta}{298.15}} - 273.15 \quad \text{(EQ. 22)}$$

5. Choose a number close to the result as in Equation 23 for the "TCOMP" register.

$$T_{COMP} = T_{CSC} - T_{NTC} \quad \text{(EQ. 23)}$$

6. Run the actual board under full load again.
7. Record the output voltage as V1 immediately after the output voltage is stable with the full load. Record the output voltage as V2 after the VR reaches the thermal steady state.
8. If the output voltage increases over 3mV as the temperature increases, i.e. V2 - V1 > 3mV, reduce "TCOMP" value; if the output voltage decreases over 3mV as the temperature increases, i.e. V1 - V2 > 3mV, increase "TCOMP" value.

Dynamic VID Compensation (DVC)

During DVID transitions, extra current builds up in the output capacitors due to the C*dv/dt. The current is sensed by the controller and fed across the feedback resistor creating extra droop (if enabled) and causing the output voltage not properly tracking the DAC voltage. An independent compensation for DVID up and DVID down are implemented to optimize the DVID transition (Patent Pending), programmable by D7 and D9, respectively.

Programmable Compensation

The ISL6388 controller utilizes Intersil's proprietary Advanced Linear EAPP Digital control scheme that is the best modulation scheme in the industry to achieve linear response for both transient and current balance and can process voltage and current information in real time for fast control and high speed protection and realize digital power management capability and flexibility. The digital compensation covers a wide range of poles and zeros, as in Figure 25, suitable for computing, networking, ASIC, and many general purpose applications. Refer the ISL6388 GUI and Table 15 for more details and advanced features.

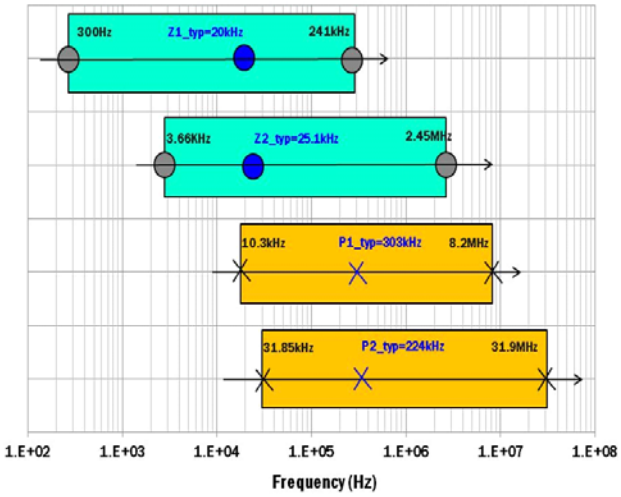


FIGURE 25. TYPE III COMPENSATION POLES AND ZERO RANGE

Catastrophic Fault Protection

A catastrophic failure is a failure that will result in an exothermic event if the power source is not removed. A predominate catastrophic failure is a high-side FET shorting, which can cause either output overvoltage or input overcurrent event. When the ISL6388 detects either event, an internal switch is turned on to pull the EN_PWR_CFP pin to V_{CC}, as an indication of a component failure in the regulator's power train. As shown in Figure 26, a CFP fault signal can be generated by using a resistor divider on this pin. To be able to apply the signal to the PS_ON# switch of an ATX power supply or a simply external switch (2N7002), the CFP fault signal should be lower than 0.8V at maximum input voltage, $V_{IN(max)}$ and higher than 3V at lowest normal operational V_{CC} (4.5V) when the input voltage (V_{IN}) is removed. Given these conditions, the equivalent (in parallel) impedance of the upper leg (R_{UP}) and lower leg ($R_{DW} = R_{DW1} + R_{DW1}$) should be higher than 1kΩ. For instance, if we select the total lower leg impedance (R_{DW}) as 9.39kΩ, then the R_{UP} is calculated as in Equation 25, 100kΩ for maximum POR of 10.72V, The lower leg impedance is then calculated by 2.74kΩ and 6.65kΩ, as in Equations 26 and 27, respectively.

$$R_{DW} = R_{DW1} + R_{DW2} \quad \text{(EQ. 24)}$$

$$R_{UP} = \frac{VIN(POR, max) - 0.92V}{0.92V} \cdot R_{DW} \quad \text{(EQ. 25)}$$

$$R_{DW1} = \frac{VIN(max)}{0.8V} \cdot (R_{UP} + R_{DW}) \quad \text{(EQ. 26)}$$

$$R_{DW2} = R_{DW} - R_{DW1} \quad \text{(EQ. 27)}$$

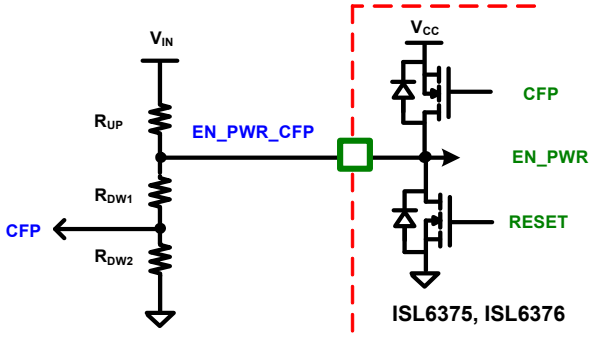


FIGURE 26. BI-DIRECTIONAL EN_PWR_CFP

Prior to an exothermic event, the fault signal (CFP) should be used on the platform to remove the power source either by firing a shunting SCR to blow a fuse or by turning off the AC power supply.

Input Current Sensing

The input current sensing uses Intersil patented technique to overcome the high common-mode input requirement challenge. An R-C network with thermal compensation across the inductor (LIN) extracts the DCR voltage, as shown in Figure 27, while the C might need to be split into 2, one close the LIN and one close to the controller. The input inductor can be used for current sensing and has benefit of isolating noise from the rest of the board. However, when there are insufficient bulk capacitors on the power-stage side, a resonant tank can be formed by input ceramic capacitors and the inductor, yielding oscillation or audio noise during audio frequency range of heavy load transient. In addition, since Z_{NTC} network steals portion of sensed current from R_{IN1}, input current reading will have offset.

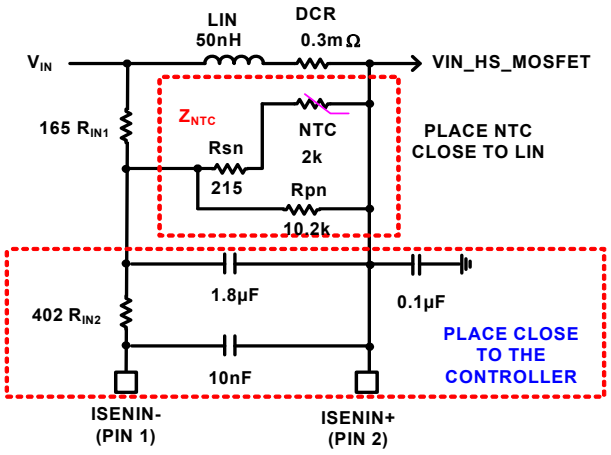


FIGURE 27. INPUT DCR-SENSING CONFIGURATION

In many cases, a narrow input-rail PCB trace (but wide enough to carry DC current) is sufficient to serve as the isolation path. Thus, the input current sensing can simply be realized with dedicated power resistor, as shown in Figure 28.

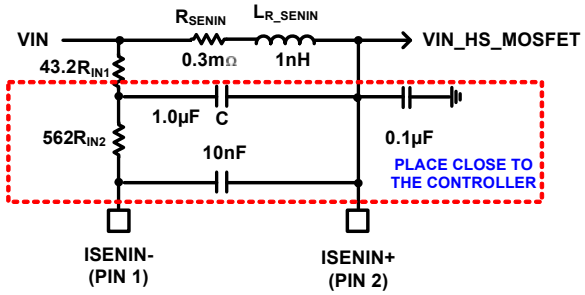


FIGURE 28. INPUT R-SENSING CONFIGURATION

The full scale of input current sensing is 10µA, read 1Fh with READ_IIN(89h), via PMBus, while the input over-current trip point is at 15µA (Programmable via F6[6:5]). A greater than 40 µs time constant $[C*R_{IN1}*R_{IN2})/(R_{IN1}+R_{IN2})]$ might be needed if the average input current reporting is preferred; and it also reduces chance to trigger CFP during heavy load transient depending upon the input filter. A design worksheet to select these components is available for use. Please contact Intersil Application support at www.intersil.com/design.

When not used, connect ISENIN+ to VIN and a resistor divider with a ratio of 1/3 on ISENIN± pin, (say 499kΩ) in between ISENIN± pins and then 1.5MΩ from ISENIN- to ground (see Figure 29).

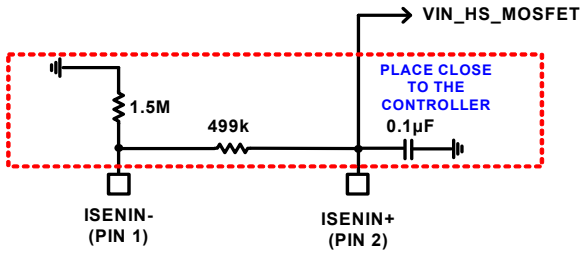


FIGURE 29. DISABLE PIN AND IIN CONFIGURATION

Auto-Phase Shedding

In addition to low power mode (PSI#) operation, the ISL6388 also incorporates auto-phase shedding feature to improve light to medium load range. The phase current dropping threshold is programmable with the resistor on AUTO pin. The efficiency-optimized current trip point (I1) from 1-Phase to 2-Phase operation is approximated with Equation 28, which is kx larger than the efficiency-optimized current trip step (dI = I3 - I2) in between from 2-phase to 3-phase (I2) and from 3-phase to 4-phase (I3). The optimized-efficiency current trip point difference between phases remain constant I1/k, as expressed in Equation 29 and Figure 30.

$$I1 \approx \sqrt{\frac{2 \cdot (P_{QG} + P_{CORE} + P_{COSS})}{ESR_{IN} \cdot D + R_{ON} + L_{DS} \cdot F_{SW}}} \quad \text{(EQ. 28)}$$

$$R_{ON} = D \cdot r_{DS(ON)\_UP} + (1 - D) \cdot r_{DS(ON)\_LOW} + DCR$$

where P_{QG} is the per-phase gate charge loss, P_{CORE} is the inductor core loss, P_{QOSS} is the sum of high-side and low-side MOSFETs' output charge loss.

$$R_{AUTO} = \frac{1.2V}{I_{IMON\_OPTIMIZED\_1\_PHASE}} \quad \text{(EQ. 30)}$$

$$I_{IMON\_OPTIMIZED\_1\_PHASE} \approx \frac{64 \cdot DCR \cdot I1}{N_{MAX} \cdot R_{SET}} \quad \text{(EQ. 31)}$$

$$R_{AUTO} \approx \frac{1.2V \cdot N_{MAX} \cdot R_{SET}}{64 \cdot DCR \cdot I1} \quad \text{(EQ. 32)}$$

$$I_{(N)} \approx I1 \cdot \left(1 + \frac{1}{K} \cdot (N-1)\right) \quad \text{(EQ. 29)}$$

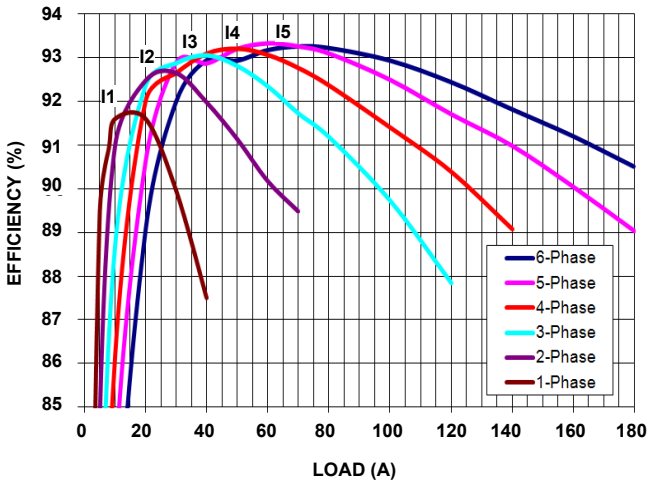


FIGURE 30. EFFICIENCY vs PHASE NUMBER

Equations 30 and 32 helps approximate the AUTO resistor, while the trip point hysteresis can be programmed via PMBus D1[5:4]. Typically, the higher the inductor ripple current, the higher percentage of hysteresis and k it requires. Following is an easy way to estimate R_{AUTO} value:

1. Before AUTO trip point tuning, calibrate IMON current close to zero with PMBus E4[4:0].
2. Disable AUTO mode via D4[2] or by tying AUTO pin GND
3. Obtain efficiency curve for 1 to 6-phase, programmed via D0,with appropriate load (~25A/Phase. 0.5A step); and APA disabled via D4h as needed.
4. Determine I1 from the above test result.
5. Short AUTO pin to ground with a current meter to measure the IMON current ($I_{IMON\_OPTIMIZED\_1\_PHASE}$) when VR is at I1 load.
6. Calculate R_{AUTO} as in Equation 32.
7. Solder down R_{AUTO} and enable AUTO mode.
8. Take efficiency curve and compare it with the 1- to 6-Phase Efficiency Curves.
9. Tweak R_{AUTO} and D1 (K, I1, Hysteresis) as needed for optimal efficiency performance at targeted operating input and output voltage as well as airflow.
10. Obtain efficiency curve for couple boards and tweak R_{AUTO} to re-center overall efficiency of these boards.

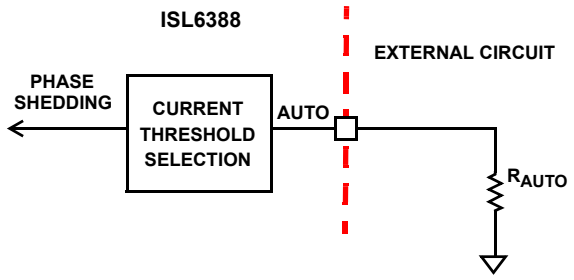


FIGURE 31. SIMPLIFIED AUTO-PHASE SHEDDING CIRCUIT

In addition, the SMBus, PMBus, or I^2C gives flexibility to program Auto K-factor (D1[3:2]), hysteresis (D1[5:4]), I1 (D1[7:6]), and number of operating phases after soft-start and when Auto mode is disabled by D4[2]. However, all phases will be added back when APA is triggered; and if APA is disabled, all phase are added back only after reset or OCP retry.

The minimum of auto-phase shedding is defaulted by NPSI in PSI1 mode and can be programmed by the bus command code D1h[1:0], as in Table 15. The phase dropping sequence is summarized in Table 9.

TABLE 9. PHASE DROPPING SEQUENCE

N	PWM# TIED TO V_{CC} (VCORE)	PHASE SEQUENCE PSI# = PSI0
6	NONE	6-3-5-2-4-1
5	PWM6	5-4–2-3-1
4	PWM5	4-2-3-1
3	PWM4	3-2-1
2	PWM3	2-1

To ensure dropped phases have sufficient energy to turn on high-side MOSET and sustain instant load apply after VR0 staying in light load condition for a long time (hours to days), a boot-refresh circuit turns on low-side MOSFET of each dropped phase to refresh the boot capacitor at a rate of slightly above 20kHz. The boot-fresh circuit is automatically turned off to boot efficiency when DAC drops to 0.60V.

SVID Operation

The device is compliant with Intel VR12.5/VR12/IMVP7 SVID protocol. To ensure proper CPU operation, refer to this document for SVID bus design and layout guidelines; each platform requires different pull-up impedance on the SVID bus, while impedance matching and spacing among DATA, CLK, and ALERT# signals must be followed. Common mistakes are insufficient spacing among signals and improper pull-up impedance. When SVID is not used, simply leave the respective pull-up on their pins and not connect to the bus.

TABLE 10. SVID SUPPORTED REGISTERS

INDEX	NAME	DESCRIPTION	ACCESS	DEFAULT
00h	Vendor ID	Intel Assigned VR Vendor ID	R	12h
01h	Product ID	Intersil Unique Product ID	R	58h
02h	Product Revision		R	04h
05h	Protocol ID	VR12 = 01h VR12.5 = 02h	R	"VRSEL" Pin
06h	Capability	VR capability Register 0h = not supported; 1h = supported Bit0 = I_{OUT}(15h) = 1 Bit1 = V_{OUT} (16h) = 1 Bit2 = POUT (18h) = 1 Bit3 = I Input (19h) = 1 Bit4 = V Input (1Ah) = 1 Bit5 = P Input (1Bh) = 1 Bit6 = Temperature (17h) = 0 Bit7 = 1 (1 if 15h is formatted FFh = ICC_MAX; 0 if 15h is formatted 1A per_LSB) ISENIN± IN USE = BFh ISENIN± NOT USED = 97h (NOT SUPPORT IIN and PIN 1/3 Divider on These Pins)	R	BFh or 97h
10h	Status_1	At End of Soft-Start	R	01h
11h	Status_2		R	00h
12h	TempZone		R	00h
15h	I_{OUT}	Digital Reading of IMON	R	00h
1Ch	Status_last Read	A copy of the Status_2 data that was last read with GetReg (11h) command.	R	00h
21h	ICC_MAX	Programmable via PMBus EA[7:0] 0A to 255A	R	NVM
22h	Temp_max	Programmable via PMBus E8[2:0]	R	NVM
24h	SR_Fast	Programmable via PMBus F6[4:0] 1.25mV/µ to 53 mV/µ	R	NVM
25h	SR_Slow	1/4 of SR_Fast	R	NVM
26h	V_{BOOT}	Programmable via "BT" pin; or via PMBus E6h[7:0] prior to Enable High	RW	NVM
30h	V_{OUT}_MAX	Maximum Allowable DAC	RW	FFh
31h	VID Setting		RW	V_{BOOT}
32h	Power State		RW	00h
33h	Offset		RW	00h
34h	Multi_VR_Config	Set VR_Ready State when SetVID 0V after first Boot	RW	00h
35h	SetRegADR		RW	00h

NOTE: Programmable ICC_MAX, TMAX, V_{BOOT} via PMBus.

Resistor Reader (Patented)

Intersil has developed a high resolution ADC using a patented technique with simple 1%, 100ppm/k or better temperature coefficient resistor divider. The same type of resistors are preferred so that it has similar change over-temperature. In addition, the divider is compared to the internal divider off V_{CC} and GND nodes and therefore must refer to VCC and GND pins, not through any RC decoupling network.

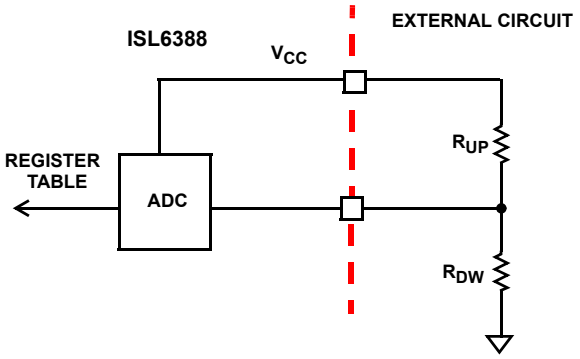


FIGURE 32. SIMPLIFIED RESISTOR DIVIDER ADC

The NVM_BANK_BT pin is designed to allow the user to select different NVM Banks (Pre configured IC) and/or Boot Voltage Level even without PMBus communications; while VRSEL_ADDR is to select different operation mode (VR12 or VR12.5 Mode), indirectly control Boot Voltage Level and DAC resolution, VOUT_MAX, and SVID/PMBus addresses. The programmed values of resistor reader are stored in 0C/DC and 0D/DD of SVID/PMBus.

Table 11 shows the R_{UP} and R_{DW} values of each pin for a specific system design; DATA for corresponding registers can be read out via SVID's Get(reg) command or PMBus command (DC and DD). In addition, some tie-high and tie-low options are available for easy programming (save resistor dividers) and can be used to validate the VR operation during In-Circuit Test (ICT). For instance, when the system boot voltage is required at 0V, the NVM_BANK_BT pin can be set to different voltage level, prior to power-up, to get a known boot voltage to check VR operation with ICT. Resistor reader calculator is available, please contact Intersil Application support at www.intersil.com/design.

TABLE 11. RESISTOR READER EXAMPLE

SVID/PMBus (0C/DC)	R_{UP} (kΩ)	R_{DW} (kΩ)	SVID/PMBus 8-Bit ADDRESS	RECOMMENDED APPLICATIONS
00h	OPEN	10	0/80	VR12.5 Vcore
01h	49.9	12.4	0/82	VR12.5 Vcore
02h	45.3	12.7	0/84	VR12.5 Vcore
03h	43.2	13.3	0/86	VR12.5 Vcore
08h	29.4	15	2/C0	VR12.5, Vmem
09h	28	15.4	2/C2	VR12.5, Vmem
0Ch	24.3	17.4	4/C8	VR12.5, Vmem
0Dh	23.2	17.8	4/CA	VR12.5, Vmem
10h	20	19.6	6/E0	VR12.5, Vmem

TABLE 11. RESISTOR READER EXAMPLE (Continued)

SVID/PMBus (0C/DC)	R_{UP} (kΩ)	R_{DW} (kΩ)	SVID/PMBus 8-Bit ADDRESS	RECOMMENDED APPLICATIONS
11h	19.6	20.5	6/E2	VR12.5, Vmem
14h	17.4	23.2	8/E8	VR12.5, Vmem
15h	16.9	24.3	8/EA	VR12.5, Vmem
80h	OPEN	10	0/80	VR12 Vcore
81h	374	93.1	0/82	VR12 Vcore
82h	340	95.3	0/84	VR12 Vcore
83h	316	100	0/86	VR12 Vcore
88h	221	113	2/C0	VR12 Vmem
89h	210	115	2/C2	VR12 Vmem
8Ch	182	130	4/C8	VR12 Vmem
8Dh	174	133	4/CA	VR12 Vmem
90h	150	147	6/E0	VR12 Vmem
91h	147	154	6/E2	VR12 Vmem
94h	130	174	8/E8	VR12 Vmem
95h	127	182	8/EA	VR12 Vmem
SVID/PMBus (0D/DD)	**R_{UP} (kΩ)**	**R_{DW} (kΩ)**	**NVM**	**BT**
00h	OPEN	10	NVM0	NVM_BT
20h	118	26.1	NVM1	NVM_BT
40h	196	43.2	INVM2	NVM_BT
60h	294	64.9	NVM3	NVM_BT
80h	422	93.1	NVM4	NVM_BT
A0h	590	130	NVM5	NVM_BT
C0h	825	182	NVM6	NVM_BT
E0h	OPEN	499	NVM7	NVM_BT
01h	49.9	12.4	NVM0	0.0V
10h	20	19.6	NVM0	1.7V, VR12.5
09h	28	15.4	NVM0	0.6V, VR12 1.2V, 12.5
32h	40.2	45.3	NVM1	0.9V, VR12 1.8V, VR12.5
55h	59	84.5	NVM2	1.0V, VR12 2.0V, VR12.52
79h	78.7	163	NVM3	1.2V, VR12 2.4V, VR12.5
9Fh	95.3	367	NVM4	1.5V, VR12 2.0V, VR12.5
B2h	196	226	NVM5	1.8V, VR12.5
DAh	215	475	NVM6	2.5V, VR12.5

NOTE: More options in resistor reader calculator. NVM_BT = Boot Voltage Loaded from the Bank, not fixed by resistor reader.

Memory Banks

The ISL6388 has 8 memory banks to store up (STORE_USER_ALL, 15h) to 8 different configurations, selectable via PMBus (DEh) or resistor to GND on the NVM_BANK pin, as in Table 12. No decoupling capacitor is allowed on the pin. Prior to the soft-start, the selection of memory bank is stored in the data register of SVID (0Dh) or PMBus (DDh), respectively. They are reset by VCC POR. In addition, the selected memory bank can be overridden by PMBus (DEh). Only the selected memory bank's configuration is loaded (RESTORE_USER_ALL,16h) into the operating memory to have control on the VR system prior to issuing soft-start.

TABLE 12. MEMORY BANK (SVID/PMBus, 0D/DD)

DEh	MEMORY BANK NAME	RECOMMENDED USAGE
00h	USER_NVM0	User Vcore
01h	USER_NVM1	User Vmem
02h	USER_NVM2	User Vcore
03h	USER_NVM3	User Vmem
04h	USER_NVM4	User Vcore
05h	USER_NVM5	User Vmem
06h	USER_NVM6	Factory or User Vcore
07h	USER_NVM7	Factory or User Vmem

Other than device's SVID/PMBus Addresses and VR operation mode (VR12 or VR12.5), all system design parameters are programmed by PMBus, as summarized in Table 13 and detailed in Table 15.

TABLE 13. SYSTEM PARAMETER SUMMARY

CODE	SVID REG	PMBus REG	DESCRIPTION	RANGE
SV_ADDR	N/A	N/A	SVID Address (in Pair with PMBus Address)	0, 1, 2, 4, 6, 8, A
PM_ADDR	N/A	N/A	PMBus Address (In Pair with SVID Address)	80-8E, C0-CE, E0-EE, F0-FE
VR_MODE	05	N/A	By "VRSEL" Pin	VR12 or VR12.5
BT	26	E6	VR12 Boot Voltage	0, 0.25 to 1.52V
			VR12.5 Boot Voltage	0, 0.5, 0.51 to 3.04V
FDVID	24	F6	setVID Fast Slew Rate	1.25 to 53mV/µs
	N/A	D7	DVID UP Compensation	Offset, Gain, Slope
	N/A	D9	DVID Down Compensation	Offset, Gain, Slope
TMAX	22	E8	Maximum Operating Temperature	+85°C to +120°C (5°C/Step)
IMAX	21	EA	I_{CCMAX} of Platforms	0-255A, 1A/LSB
DE	N/A	D4	Diode Emulation Option	Enable or Disable
NPSI	N/A	D2	Number of Operational Phases in PSI1 Mode	SI1, SI2, CI1, CI2
Protection	N/A	D2	Frequency Limiter	$2F_{SW}$, $1.5F_{SW}$, Infinity
	N/A	E1	SET_UV	105mV to 402mV
	N/A	D8	SET_OV	136mV to 549mV
	N/A	24	Maximum Output Voltage	Up to 3.11V
	N/A	DF	PROTECTION_DISABLE	All Faults
	N/A	F6	INPUT OCP	100% to 130%
	N/A	E9	Thermal APA	75% to 100%
	N/A	F4	AVG_OCP CYCLE_LIMITING	1.0 to 1.6 125% to 70%
	N/A	F7-FC	Current Balance	-12% to +9%
DIGITAL I_{OUT} (SV, 15h) (PM, 8Ch)	N/A	E4	IMON_TRIM	-4µA to +3.75µA
	N/A	E5	IOUT_CAL_OFFSET	-4h to 3h

TABLE 13. SYSTEM PARAMETER SUMMARY (Continued)

CODE	SVID REG	PMBus REG	DESCRIPTION	RANGE
LOOP	N/A	D8	UP Ramp Amplitude	0.75, 1.0, 1.2, 1.5V
	N/A	DE	NVM_BANK	Up to 8 Banks
	N/A	D4	Dither Enable	Enable or Disable
	N/A	E9	Mismatching Temperature Compensation between sensing element and NTC	OFF, -2.5°C to +35.1°C
	N/A	E2	PSI Mode Transition Compensation	PS and Decay Mode Transition
	N/A	E2, E3	High Frequency Transient Compensation	E2[4:3]: 20m- 80mV E3: Phase Count Original Speedup
	N/A	F5	SET_FREQ	120k to 2.025MHz
	N/A	B0-BF	COMPENSATION	R1-R3 and C1-C3
	N/A	F3	SP_VdBand_K	Original, 2p-16pF 25mV - 200mV 0 to 0.75, Disable
Output Voltage Regulation	N/A	D6	Lock_SVID	0h to 3h
	31	DA	Set_VID	up to 3.04V
	33	DB	Set_OFFSET	up to 1.270V
	N/A	D3	Droop Enable	Enable or Disable
	N/A	D3	Negative Droop	100% to 5%
	N/A	D3	Positive Droop	0mV, 4mV to 32mV
	N/A	E4	IDROOP_TRIM	-4µA to +3.75µA
	N/A	E4	Output Offset Trim	-4µA to +3.75µA
AUTO	N/A	D0	NPHASE	1 to 6-PHASE
	N/A	D1	AUTO_K	1.0, 1.25, 1.5, 1.7
	N/A	D1	AUTO_HYS	12.5, 16.6, 25, 50%
	N/A	D1	AUTO_I1	80, 90, 100, 110%
	N/A	D1	Minimum Phase	1 to 4-PHASE
	N/A	D2	AUTO Blanking	0.6ms to 4.6ms
	N/A	D2	APA Time Constant	$t_{sw}/8$ to t_{sw}
	N/A	D2	APA_Stackup_Delay	0 to 300ns
	N/A	D4	APA LEVEL	10 to 70mV
	N/A	D4	BOOT REFRESH	Enable or Disable
	N/A	D4	AUTO Enable	Enable or Disable
USER	N/A	99	MFR_ID	2 BYTES
	N/A	9A	MFR_MODEL	2 BYTES
	N/A	9B	MFR_REV	2 BYTES
	N/A	9D	MFR_DATE	3 BYTES

SMBus, PMBus, AND I²C Operation

There are 32 pairs of SVID/PMBus address, which can be programmed by a resistor divider on VRSEL_ADDR pin, as shown in Figure 32. It includes 7 SVID addresses and 32 SMBus/PMBus/I²C addresses combination, as in Table 14.

The ISL6388 features SMBus, PMBus, and I²C with programmable address via VRSEL_ADDR pin, as in Table 14, while SMBus/PMBus includes an Alert# line and Packet Error Check (PEC) to ensure data properly transmitted. In addition, the output voltage, droop slope, enable, operating phase number, overvoltage setpoint, and the priority of SVID and SMBus/PMBus/I²C can be written and read via this bus, as summarized in Table 15. The input, output, fault, and temperature telemetries can be read as summarized in Table 16. For proper operation, users should follow the SMBus, PMBus, and I²C protocol, as shown Figure 36. Note that STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of register, as shown in Figure 36.

The supported SMBus/PMBus/I²C addresses are in 8-bit format (including write and read bit): 80-8E, E0- EE, C0-CE. F0-FE. The least significant bit of the 8-bit address is for write (0h) and read

(1h). For reference purpose, the 7-bit format addresses are also summarized in Table 14. There are a series set of write and read commands as summarized in Tables 15 and 16, respectively.

SMBus/PMBus/I²C allows to program the registers as in Table 13, except for SVID and SMBus/PMBus/I²C addresses, 16ms after V_{CC} above POR and prior to Enable pins (EN_PWR_CFP) high. The bus can also program default contents during this period. If all Enable pins are high before the NVM configuration is loaded completely, the controller will issue soft-start 16ms after VCC above its POR. When device’s PMBus is not used, simply ground their pins and not connect them to the bus.

TABLE 14. SMBus/PMBus/I²C 8-BIT AND 7-BIT FORMAT ADDRESS (HEX)

SVID	8-BIT	7-BIT	SVID	8-BIT	7-BIT	SVID	8-BIT	7-BIT
0	80/81	40	4	C8/C9	64	A	F0/F1	78
0	82/83	41	4	CA/CB	65	A	F2/F3	79
0	84/85	42	4	CC/CD	66	A	F4/F5	7A
0	86/87	43	4	CE/CF	67	A	F6/F7	7B
0	88/89	44	6	E0/E1	70	1	F8/F9	7C
0	8A/8B	45	6	E2/E3	71	1	FA/FB	7D
0	8C/8D	46	6	E4/E5	72	1	FC/FD	7E
0	8E/8F	47	6	E6/E7	73	1	FE/FF	7F
2	C0/C1	60	8	E8/E9	74			
2	C2/C3	61	8	EA/EB	75			
2	C4/C6	62	8	EC/ED	76			
2	CE/CF	63	8	EE/EF	77			

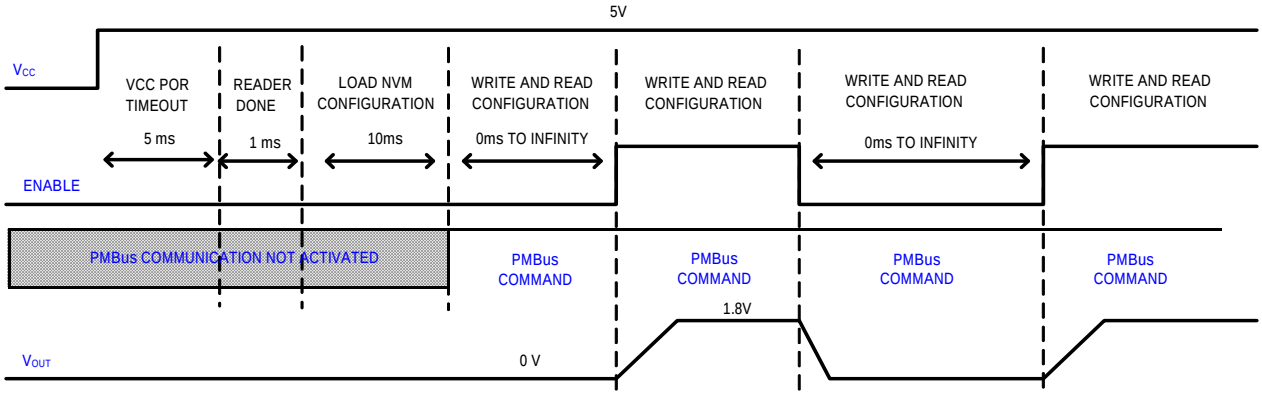


FIGURE 33. SIMPLIFIED SMBus/PMBus/I²C INITIALIZATION TIMING DIAGRAM

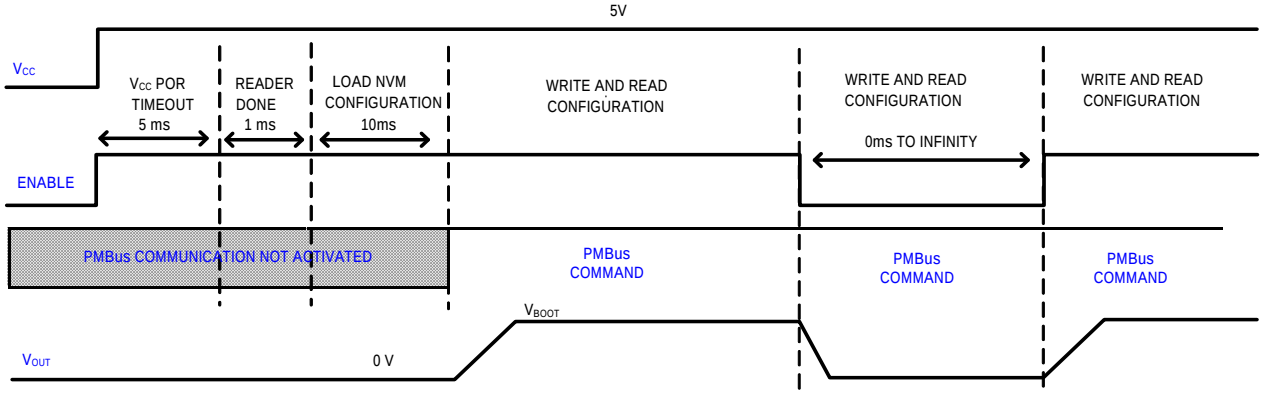
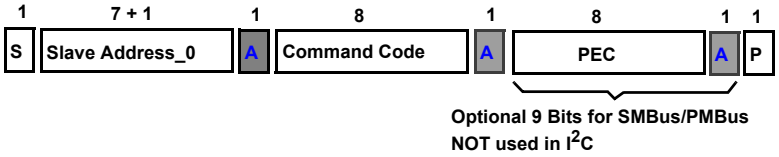


FIGURE 34. SIMPLIFIED SMBus/PMBus/I²C INITIALIZATION TIMING DIAGRAM WITH ENABLE HIGH BEFORE COMPLETING NVM LOADING

1. Send Byte Protocol

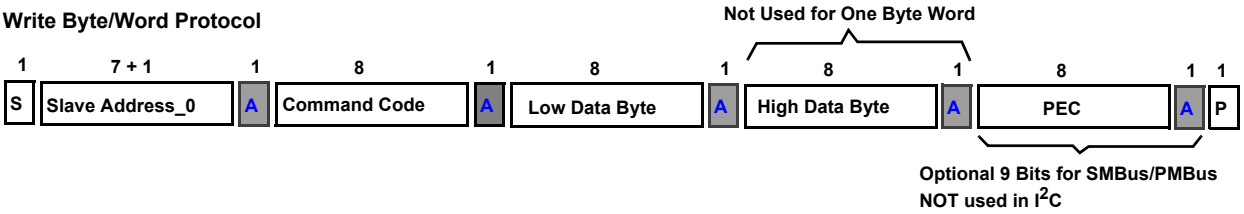


Example command: 03h Clear Faults
(This will clear all of the bits in Status Byte for the selected Rail)

S: Start Condition
A: Acknowledge (“0”)
N: Not Acknowledge (“1”)
W: Write (“0”)
RS: Repeated Start Condition
R: Read (“1”)
PEC: Packet Error Checking
P: Stop Condition

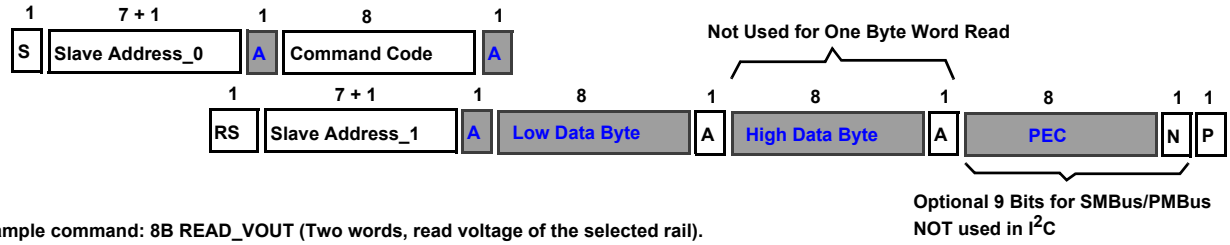
Acknowledge or DATA from Slave, ISL6388

2. Write Byte/Word Protocol



Example command: DAh SET_VID (one word, High Data Byte and ACK are not used)

3. Read Byte/Word Protocol

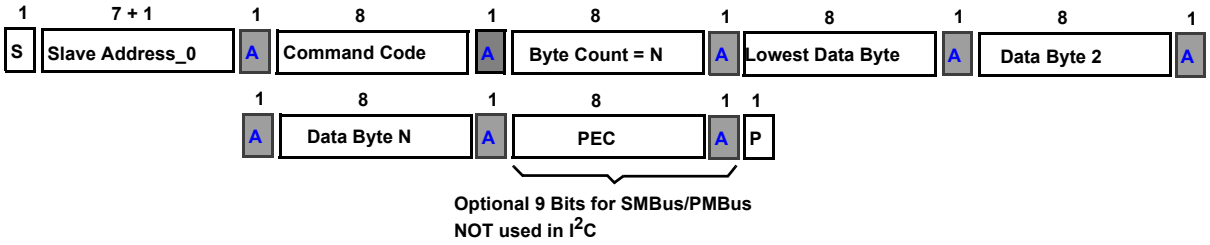


Example command: 8B READ_VOUT (Two words, read voltage of the selected rail).

NOTE: That all Writable commands are read with one byte word protocol.

STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of a register.

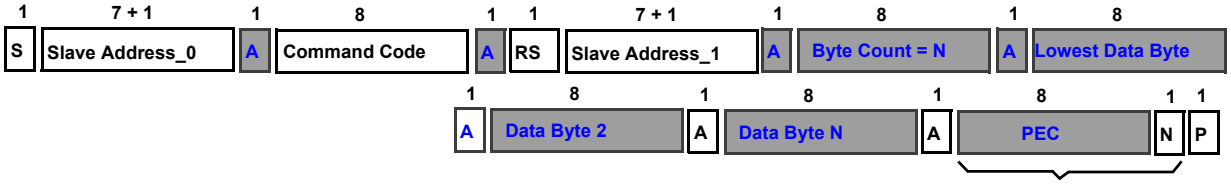
4. Block Write Protocol



Example command: 9Dh MFR_DATA (3 Data Byte)

FIGURE 35. SMBus/PMBus/I2C PROTOCOL

5. Block Read Protocol

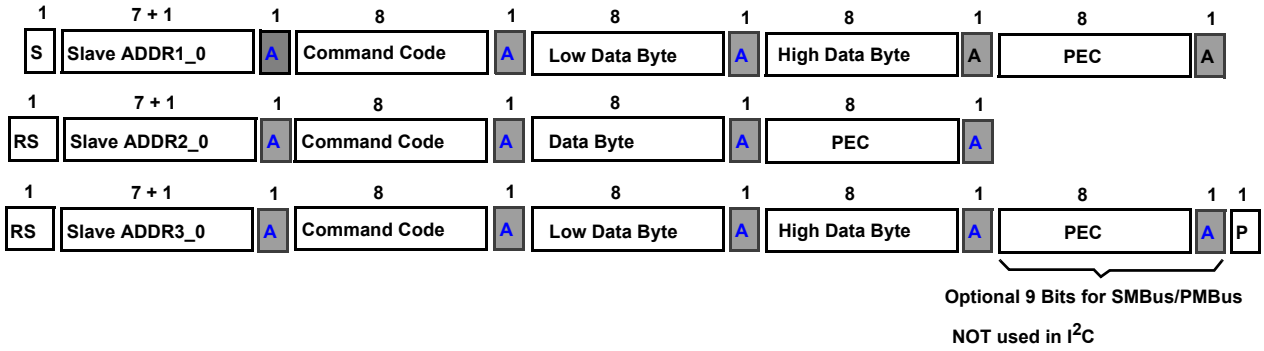


Example command: 8B READ_VOUT (Two words, read voltage of the selected rail).

NOTE: That all Writable commands are read with one byte word protocol.

STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of a register.

6. Group Command Protocol - No more than one command can be sent to the same Address



7. Alert Response Address (ARA, 0001_1001, 19h) for SMBus and PMBus, not used for I^2C

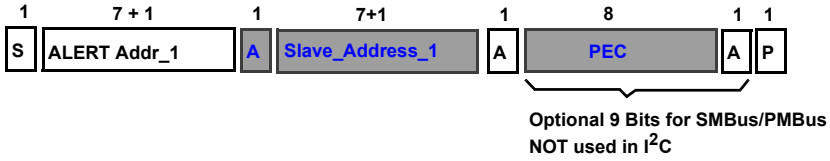


FIGURE 36. SMBus/PMBus/I^2C PROTOCOL

TABLE 15. SMBus, PMBus, AND I^2C WRITE AND READ REGISTERS

COMMAND CODE	ACCESS	WRITE PROTECT LEVEL	DEFAULT	COMMAND NAME	DESCRIPTION
01h[2:0]	R/W	40h	EN pin	OPERATION (or ENABLE)	Bit[7]: 0 = OFF (0-F); 1 = ON (80-8Fh) Bit[6:4] = 0; Bit[3:0] = Don't care
10h[7:5]	R/W	NOT	80h	WRITE_PROTECT_ISL	80h = Disable all standard writes (including send bytes) except for WRITE_PROTECT_ISL command. 40h = Disable all standard writes (including send bytes), all compensation registers and some Intersil defined commands, BUT NOT WRITE_PROTECT, OPERATION, CLEAR_FAULT and some Intersil defined commands. 20h = Disable all standard writes, all compensation registers and some Intersil defined commands, BUT NOT WRITE_PROTECT, OPERATION, CLEAR_FAULT and some Intersil defined commands: Lock VID, Set_VID, Set_OFFSET. 10h = Disable all compensation registers and some Intersil defined commands, BUT not WRITE_PROTECT, OPERATION, CLEAR_FAULT and some Intersil defined commands: Lock VID, Set_VID, Set_OFFSET, Configurations (UVP, OVP, OCP, CFP, IMAX, TMAX, AUTO, NPHASE, BAL_XX, FREQ, BOOT_VOLTAGE, etc). 00h = Enable all write commands. Reject all command code except for 80h, 40h, 20h, 10h, 0h Not support PAGE and ON_OFF_CONFIG; Equivalent VOUT_COMAND is Set_VID, Set_OFFSET, LOCK_SVID "WRITE PROTECT LEVEL" = ANYTHING SPECIFIED IN THIS LEVEL OR BELOW IS ALLOWED TO BE WRITTEN.
15h	SEND	00h	N/A	STORE_USER_ALL	Store user configuration (operating memory) into selected USER_NVM#. The device will declare busy at the assertion of this command, a new command addressed to this device should be sent 300ms afterward.
16h	SEND	00h	N/A	RESTORE_USER_ALL	Restore user configuration (USER_NVM#) into operating memory. The device will declare busy at the assertion of this command, a new command addressed to this device should be sent 6ms afterward.
24h[8:0]	R/W	00h	NVM_BANK	VOUT_MAX	Set maximum output voltage that VR can command (VOUT_MAX = VID+OFFSET > BOOT_Voltage). VR12 Mode: Up to 2.155 (H Byte: 01h; L Byte 7Eh, see Table 19); VR12.5 Mode: Up to 3.11V (High Byte: 01h; Low Byte 06h).
99[15:0]	BLOCK R/W	00h		MFR_ID	User stores ID.
9A[15:0]	BLOCK R/W	00h		MFR_MODEL	User stores model number.
9B[15:0]	BLOCK R/W	00h		MFR_REVISION	User stores board and/or configuration revision number.
9D[23:0]	BLOCK R/W	00h		MFR_DATE	User stores date.
AD[15:0]	BLOCK R	N/A		IC_DEVICE_ID	Intersil Device ID: product ID (update byte, content of 01h in SVID, hardcoded) + ISL configuration revision (lower byte).
AE[15:0]	BLOCK R	N/A		IC_DEVICE_REV	Intersil Device Revision: Silicon revision (upper byte, content of 02h in SVID, hardcoded) + ISL configuration revision (lower byte).
D0h[2:0]	R/W	00h	N_{PHASE} By Pin	OPERATE_PHASE_NUMBER	0h = 7h = N_{MAX}; 1h = 1 Phase;2h = 2 Phases; 3h = 3 Phases; 4h = 4 Phases; 5h = 5 Phases; 6h = 6 Phases. N_{MAX} set by PWMx hard wired; for instance if PWM6 = V_{CC}, N_{MAX} = 5 Phases. D0 should NOT be written until 50ms after soft-start and re-written after DVID. When AUTO (R to GND, not shorted to GND) function is enabled, D0h cannot use to program phase number but it reports the operating phase number.

TABLE 15. SMBus, PMBus, AND I^2C WRITE AND READ REGISTERS

COMMAND CODE	ACCESS	WRITE PROTECT LEVEL	DEFAULT	COMMAND NAME	DESCRIPTION
D1h[7:0]	R/W	00h	NVM_BANK	NMIN_AUTOK_HYS_I1	Bit[1:0] - Minimum Number of Auto Phase Shedding 0h = 1-Phase; 1h = 2-Phase; 2h = 3-Phase; 3h = 4-Phase; Default = N_{PSI} Bit[3:2] - AUTO Mode K Factor: 0h = 1.25; 1h = 1.5; 2h = 1.75; 3h = 1.0 Bit[5:4] - AUTO Mode Hysteresis Factor 0h = 50%; 1h = 25%; 2h = 16.6%; 3h = 12.5%; Bit[7:6] - AUTO Mode I1 Factor: 0h = 100%; 1h = 80%; 2h = 90%; 3h = 110% of AUTO pin
D2h[9:0]	R/W	00h	NVM_BANK	NPSI_ATBLK_FLIM_APATCDLY	Bit[1:0] - Lower Power State Phase Number: 0h = SI1, 1-Phase in PSI1; 1-Phase in PSI2/3/4/Decay; 1h = SI2, 2-Phase in PSI1; 1-Phase in PSI2/3/4/Decay; 2h = CI1, 1-Phase in PSI1; 1-Phase in PSI2/3/4/Decay; 3h = CI2, 2-Phase in PSI1; 1-Phase in PSI2/3/4/Decay; Bit[3:2] - Time between subsequent phase drops: 0h = 4.6ms; 1h = 2.3ms; 2h = 1.2ms; 3h = 0.6ms Bit[5:4] - Maximum PWM frequency under repetitive Load: 0h = 2 Fsw; 1h = 3/2 Fsw; 2h = 3h = Infinity Bit[7:6] - APA Time Constant: 0h = Tsw; 1h = Tsw/2; 2h = Tsw/4; 3h = Tsw/8 Bit[9:8] - APA Stackup Delay: 0h = 0ns; 1h = 100ns; 2h = 200ns; 3h = 300ns
D3h[6:0]	R/W	10h	NVM_BANK	NEGLL_POSLL	Bit[0] - Droop Enable: 0h = Disabled, 1h = Enabled; Bit[3:1] Droop Trim (NEGLL) of Full Scale: 0h = 100%, 1h = 75%, 2h = 50%, 3h = 25%, 4h = 5%; Adjust R1 for finer resolution Bit[4]: Positive Load-Line Enable: 0h = Disabled; 1h = Enabled Bit[6:5]: Positive Load-Line Range (POSLL): 0h = 4mV, 1h = 8mV, 2h =16mV, 3h = 32mV at IMON Full Scale
D4h[6:0]	R/W	10h	NVM_BANK	BTR_DE_AUTO_DITHER_APALVL	Bit[0] - Boot-Refresh Enable: 0h = Disabled; 1h = Enabled. Boot refresh circuits is automatically turned off when DAC is lower than 0.605V Bit[1] - Diode Emulation Enable 0h = Disabled; 1h = Enabled Bit[2] - AUTO Enable: 0h = Disabled; 1h = Enabled Bit[3] - DITHER Enable: 0h = OFF, 1h = -15kHz, 0, 15kHz Bit[6:4] - APA Level: 0h = Disable; 1h = 10mV; 2h = 20mV; 3h = 30mV; 4h = 40mV; 5h = 50mV; 6h = 60mV; 7h = 70mV
D5h[1:0]	R/W	00h	NVM_BANK	PWMTRI-LEVEL	Bit[0] - PWM Support: 0h = Compatible with 3.3V PWM Tri-State (Mid) Level (PWM High is still V_{CC}, 5V); 1h = Compatible with 5.0V PWM Tri-State (Mid) Level. The 5.0V PWM Driver is also compatible with “0h”, but not vice versa.
D6h[1:0]	R/W	20h	00h	LOCK_SVID	set SVID and SMBus/PMBus/I^2C Priority (see Table 17 for details).

TABLE 15. SMBus, PMBus, AND I^2C WRITE AND READ REGISTERS

COMMAND CODE	ACCESS	WRITE PROTECT LEVEL	DEFAULT	COMMAND NAME	DESCRIPTION
D7h[13:0]	BLOCK R/W	10h	NVM_BANK	DVID_UP_OS_GAIN_SLP	BIT[5:0] - DVID_UP_OFFSET (Fix Offset regardless DVID step) 00h = 0mV 01h = 5mV 02h = 10mV ... 3Fh = 315mV BIT[8:6] - DVID_UP_GAIN (Proportional to DVID Step - deltavid) 00 = deltavid*0 01h = deltavid/32 02h = deltavid/16 ... 07h = deltavid * 7/32 BIT[13:9] - DVID_UP_SLOPE (Offset overshoot back to Target) 00h = every 4 clocks(125ns per step - 40mV/µs) 01h = every 8 clocks(250ns per step - 20mV/µs) ... 1Fh = every 128 clocks (4µs per step - 1.25mV/µs)
D8h[6:0]	R/W	10h	NVM_BANK	SET_OV_VRAMP	Bit[2:0] - OVP above VID during normal operation: 0h = 135mV, 1h = 177mV, 2h = 218V, 3h = 260mV, 4h = 342mV, 5h = 425mV, 6h = 460mV, 7h = 549mV; OVP = VID+Bit[2:0] with hysteresis of 83mV. OVP_WARNING = VID+Bit[2:0]-80mV with hysteresis of 42mV (See “Electrical Specifications” on page 10 for more details). The OVP and OVP Warning can be disabled via DFh. Bit [4:3], soft-start OVP (with 110mV Hysteresis): 0h = 1.58V, 1h = 1.86V; 2h = 2.29V; 3h = 3.32V Bit[6:5] - VRAMP 0h = 0.75V; 1h = 1.0V; 2h = 1.2V; 3h = 1.5V
D9h[13:0]	BLOCK R/W	10h	NVM_BANK	DVID_DW_OS_GAIN_SLP	BIT[5:0] - DVID_DW_OFFSET (Fix Offset regardless DVID step 00h = 0mV 01h = 5mV 02h = 10mV ... 3Fh = 315mV BIT[8:6] - DVID_DW_GAIN (Proportional to DVID Step - deltavid 00 = deltavid*0 01h = deltavid/32 02h = deltavid/16 ... 07h = deltavid * 7/32 BIT[13:9] - DVID_DW_SLOPE (Offset undershoot back to Target) 00h = every 4 clocks (125ns per step - 40mV/µs) 01h = every 8 clocks (250ns per step - 20mV/µs) ... 1Fh = every 128 clocks(4µs per step - 1.25mV/µs)
DAh[7:0]	R/W	20h	00h	SET_VID	SVID Bus VID Code (See Table 5)
DBh[7:0]	R/W	20h	00h	SET_OFFSET	SVID Bus VID Code (See Table 5, use E4[9:5] for finer step)
DCh[4:0]	R	N/A	PIN	Config Register	Reference to Resistor Reader. DC maps to config_0C
DDh[7:0]	R	N/A	PIN	Config Register	Reference to Resistor Reader. DD maps to config_0D
DEh[2:0]	R/W	20h	PIN	NVM_BANK	Bit[2:0]: 0h = USER_NVM#0 1h = USER_NVM#1 2h = USER_NVM#2 3h = USER_NVM#3 4h = USER_NVM#4 5h = USER_NVM#5 6h = USER_NVM#6 (Copy of NVM#0, otherwise, overwritten) 7h = USER_NVM#7 (Copy of NVM#1, otherwise, overwritten) Select which memory bank to store or restore the configuration.

TABLE 15. SMBus, PMBus, AND I^2C WRITE AND READ REGISTERS

COMMAND CODE	ACCESS	WRITE PROTECT LEVEL	DEFAULT	COMMAND NAME	DESCRIPTION
DFh[8:0]	R/W	10h	NVM_BANK	PROTECTION_DISABLE	[UV_WARN, OV_WARN,OTP, UVP, IPH_LIMIT, OCP_V, OCP_I, IIN_OCP, OVP]; OCP_V = IMON_3V Trip; OCP_I = 100uA trip; IIN_OCP = input OCP; OVP = Output overvoltage trip; IPH_LIMIT = Phase Current Limiting; UVP = UnderVoltage Protection; OTP = TMAX Trip; OV_WARN = Overvoltage Warning; UV_WARN = UnderVoltage Warning.
E1h[6:0]	R/W	10h	NVM_BANK	SET_UVP_DLY_ACTION	Bit[3:0] - Output UnderVoltage Protection Level: 0h = 105mV, 1h = 141mV; 2h = 178mV; 3h = 214mV; 4h = 252mV; 5h = 291mV; 6h = 328V; 7h = 402mV; UVP = DAC - UVP Level with 19mV hysteresis; UVP_WARNING = DAC-UVP+66mV (or higher) with 17mV Hysteresis (See “Electrical Specifications” on page 10 for more details). UVP and UVP Warning can be disabled via DFh Bit[5:4]: Output UnderVoltage Protection delay: 0h = 10µs, 1h = 20µs, 2h = 40µs, 3h = 120µs Bit[6] - UVP_Actions: 0h = Monitor Only; 1h = Hiccup (same as OCP timing)
E2[11:0]	R/W	10h	NVM_BANK	ADVANCED_PSCOMP_CONFIG	Bit[2:0] PS2 to PS1/0 DCM OFFSET, but make PS0/1 to 2 transition worse, which can help with Bit[8:6]. C2_pop1 momentarily offsets it back up so no dip if C2_pop1 > = bit[2:0]. 0h = 0mV, 1h = 20mV.....7h = 140mV. Bit[4:3]: High-Frequency Transient VCOMP Bottom Clamp; the lower the better. 0h = 20mV, 1h = 40mV, 2h = 60mV, 3h = 80mV Bit[5] - DECAY_COMP_OFFSET, higher is better) 0h = 100mV, 1h = 200mV Bit[8:6] - PS0/1 to PS2 Offset (C2_pop1), This likely will take the same value as Bit[2:0] or higher. This improve PS0/1 to PS2 transition, no affect on PS2 to PS1/0. 0h = 0mV, 1h = 20mV.....7h = 140mV Bit[10:9] PS1 to PS0 Offset (C2_pop2), no affect on other transitions. 0h = 0, 1h = 20mv, 2h = 40mV, 3h = 60mV
E3[13:0]	R/W	10h	NVM_BANK	ADVANCED_MOD_CONFIG	Use these registers to Optimize High Frequency Transient Response at Different Phase Count with Original Speedup (F3[2:0] = 0h = Original) Bit[0]: 1 PHASE dBAND: 0h = normal dBand; 1h = reduced dBand (faster); Bit[2:1]: 1 PHASE SPEEDUP 0h = 3h = 1/2 decay; 1h = normal decay; 2h = 1/4 decay (faster); Bit[3]: 2 PHASE dBAND; 0h = normal dBand; 1h = reduced dBand (faster); Bit[5:4]: 2 PHASE SPEEDUP 0h = 3h = 1/2 decay; 1h = normal decay; 2h = 1/4 decay (faster); Bit[6]: 3+ PHASE dBAND: 0h = normal dBand; 1h = reduced dBand (faster); Bit[8:7]: 3+ PHASE SPEEDUP 0h = 3h = 1/2 decay; 1h = normal decay; 2h = 1/4 decay (faster); Bit[10:9]: Peak-Detect CAP 0h = 1pF, 1h = 2pF, 2h = 3pF; 3h = 4pF (smaller cap is less sensitive) Bit[12:11]: High-pass CAP 0h = 1pF, 1h =2pF, 2h = 3pF; 3h = 4pF (bigger cap, more sensitive) Bit[13]: High-Frequency Balance Gain 0h = 1x; 1h = 2x gain

TABLE 15. SMBus, PMBus, AND I^2C WRITE AND READ REGISTERS

COMMAND CODE	ACCESS	WRITE PROTECT LEVEL	DEFAULT	COMMAND NAME	DESCRIPTION
E4[9:0]	R/W	20h	NVM_BANK	IMON_IDROOP_TRIM	Bit[4:0] - No Load IMON Trim (-4.0 µA to 3.75µA), add current through R1 at droop enabled and out of IMON pin together 0h = 0µA.....10h = -0.25µA 1h = 0.25µA.....11h = -0.50µA 2h = 0.50µA.....12h = -0.75µA 3h = 0.75µA.....13h = -1.00µA 4h = 1.00µA.....14h = -1.25µA 5h = 1.25µA.....15h = -1.50µA 6h = 1.50µA.....16h = -1.75µA 7h = 1.75µA.....17h = -2.00µA 8h = 2.00µA.....18h = -2.25µA 9h = 2.25µA.....19h = -2.50µA Ah = 2.50µA.....1Ah = -2.75µA Bh = 2.75µA.....1Bh = -3.00µA Ch = 3.00µA.....1Ch = -3.25µA Dh = 3.25µA.....1Dh = -3.50µA Eh = 3.50µA.....1Eh = -3.75µA Fh = 3.75µA.....1Fh = -4.00µA Bit[9:5] - No Load IDROOP Trim (-4.0 µA to 3.75µA), add current through R1 regardless droop enabled or disabled; use it to fine tune DC offset 0h = 0µA .....10h = -0.25µA 1h = 0.25µA.....11h = -0.50µA 2h = 0.50µA.....12h = -0.75µA 3h = 0.75µA.....13h = -1.00µA 4h = 1.00µA.....14h = -1.25µA 5h = 1.25µA.....15h = -1.50µA 6h = 1.50µA.....16h = -1.75µA 7h = 1.75µA.....17h = -2.00µA 8h = 2.00µA.....18h = -2.25µA 9h = 2.25µA.....19h = -2.50µA Ah = 2.50µA.....1Ah = -2.75µA Bh = 2.75µA.....1Bh = -3.00µA Ch = 3.00µA.....1Ch = -3.25µA Dh = 3.25µA.....1Dh = -3.50µA Eh = 3.50µA.....1Eh = -3.75µA Fh = 3.75µA.....1Fh = -4.00µA
E5[8:0]	R/W	20h	NVM_BANK	IOUT_CAL_OFFSET	OFFSETfor SVID Digital IOUT (15h) and PMBus READ_IOUT (8Ch): Bit[2:0] 1-Phase: 0h = 0h; 1h = 1h; 2h = 2h; 3h = 3h; 4h = -4h; 5h = -3h; 6h = -2h; 7h = -1h; Bit[5:3] 2-Phase = 0h = 0h; 1h = 1h; 2h = 2h; 3h = 3h; 4h = -4h; 5h = -3h; 6h = -2h; 7h = -1h; Bit[8:6] 3-6Phase = 0h = 0h; 1h = 1h; 2h = 2h; 3h = 3h; 4h = -4h; 5h = -3h; 6h = -2h; 7h = -1h; SVID digital I_{OUT} (15h) will read lower than FFh if the negative OFFSET is set. I.E., it will read FBh if -4h offset is selected. Therefore, IMAX register (21h in SVID, programmable by EAh) should set slightly higher than the target when negative offset is needed.
E6[7:0]	R/W	10h	NVM_BANK	BOOT_Voltage	VR12.5: 0, 0.5V, 0.51 to 3.04V (10mV/step); VR12: 0, 0.25, 0.255 To1.52V (5mV/step) (see Table 5). The data in this register does not represent the boot voltage programmed by “BT” pin, which can be read via SET_VID.

TABLE 15. SMBus, PMBus, AND I^2C WRITE AND READ REGISTERS

COMMAND CODE	ACCESS	WRITE PROTECT LEVEL	DEFAULT	COMMAND NAME	DESCRIPTION
E8[6:0]	R/W	10h	NVM_BANK	TMAX_IINMAX	Bit[2:0] - TMAX: 0h: 100°C 1h: 105°C 2h: 110°C 3h: 115°C 4h: 120°C 5h: 85°C 6h: 90°C 7h: 95°C Bit[5:3] - IINMAX (Scale IIN_READ): 0h = 31A; 1h = 15A; 2h = 7A; 3h = 3A; 4h = 1A
E9[5:0]	R/W	10h	NVM_BANK	THERMAL_TCOMP_APA	Bit[3:0] - Thermal Compensation Offset: 0h: OFF 1h: -2.5°C 2h: 0.0°C 3h: 2.5°C 4h: 5.0°C 5h: 7.0°C 6h: 10.0°C 7h: 13.0°C 8h: 16.0°C 9h: 18.9°C Ah: 21.6°C Bh: 24.3°C Ch: 27.0°C Dh: 29.7°C Eh: 32.4°C Fh: 35.1°C Bit[5:4]- Thermal APA: 0h = 75%; 1h = 82%; 2h = 91%; 3h = 100% of TMAX
EA[7:0]	R/W	10h	NVM_BANK	IMAX	Scale Digital IOUT (IMON=2.5V will read IMAX) [0h, 1h:FFh] = [0A, 1A: 255A], 1A/step SVID digital IOUT (15h) will read lower than FFh if the negative OFFSET is set. I.E., it will read FBh if -4h offset is selected. Therefore, IMAX register (21h in SVID, programmable by EAh) should set slightly higher than the target when negative offset is needed.
F2h[1:0]	R	N/A	N/A	PS	VR Operating Power Stage: 0h = PSI0; 1h = PSI1; 2h = PSI2 (or Decay); 3h = PSI3
F3h[8:0]				SPUP_dBAND_K	For Advanced User ONLY. Speedup (other than Bit[2:0] = Original) will disable frequency limiter so the switching frequency could increase with the load repetitive rate. The higher the capacitance, the faster the speed, which could lead to PSI1/2 to PS0 transition oscillation. Use with caution. Bit[2:0] Speed UP 0h = Original; 1h = 2pF; 2h = 4pF; 3h = 6pF; 4h = 8pF; 5h = 10pF; 6h = 12pF; 7h = 16pF Bit[5:3] VCOMP-dBand 0h = 25mV; 1h = 50mV; 2h =75mv; 3h = 100mV; 4h = 125mV; 5h = 150mV; 6h = 175mV; 7h = 200mV; Bit[7:6] K-Factor 0h = 0; 1h = 0.25; 2h = 0.5; 3h = 0.75 Bit[8] K-Disabled in DCM 0h = Enable; 1h=Disable
F4[5:0]	R/W	10h	NVM_BANK	OCP_ICL_TRIM	Bit [3:0]- OCP Level (IOCP_AVG and ICL): 0h = 1.0, 1h = 1.1, 2h = 1.2; 3h = 1.4, 4h = 1.5, 5h = 1.6 of IMON Bit [5:4]- Output Current Cycle Limiting (ICL): 0h = 125%, 01h = 110%, 2h = 100%; 3h = 95%, 4h = 0%, 5h = 85%, 6h = 80%, 7h = 70%
F5h[6:0]	R/W	10h	NVM_BANK	SET_FREQ	0h- 7Fh = 120kHz to 2025kHz, 15kHz/Step. F3[]

TABLE 15. SMBus, PMBus, AND I^2C WRITE AND READ REGISTERS

COMMAND CODE	ACCESS	WRITE PROTECT LEVEL	DEFAULT	COMMAND NAME	DESCRIPTION
F6h[6:0]	R/W	10h	NVM_BANK	FDVID_CFP	Bit[4:0] - Fast DVID Rate, Slow/Soft-Start Rate = 1/4 of these 0h = 1.25mV/µs; 1h = 2.5mV/µs; 2h = 5mV/µs; 3h = 10mV/µs; 4h = 11.4mV/µs; 5h = 12.3mV/µs; 6h = 13.3mV/µs; 7h = 14.5mV/µs; 8h = 16mV/µs; 9h = 17.7mV/µs; Ah = 20mV/µs; Bh = 22.8mV/µs; Ch = 26mV/µs, Dh = 32mV/µs, Eh = 40 mV/µs; Fh = 53mV/µs Bit[6:5] - IN_OCP 0h = 100%, 1h = 110%, 2h = 120%, 3h = 130%
F7h[2:0] F8h[2:0] F9h[2:0] FAh[2:0] FBh[2:0] FCh[2:0]	R/W	10h	NVM_BANK	F7 = BAL_TRIM_PHASE1 F8 = BAL_TRIM_PHASE2 F9 = BAL_TRIM_PHASE3 FA = BAL_TRIM_PHASE4 FB = BAL_TRIM_PHASE5 FC = BAL_TRIM_PHASE6	0h = -12% of full scale 1h = -9% of full scale 2h = -6% of full scale 3h = -3% of full scale 4h = No Offset 5h = +3% of full scale 6h = +6% of full scale 7h = +9% of full scale
FD[15:0]	R		N/A	CHECK_SUM	Read Calculated CheckSum for individual NVM Bank CheckSum 10ms after execute EEh(80h) command and 60ms for the total checkSum after execute EEh(40h).
03h	W	40h		CLEAR_FAULTS	Clear “Latched” Fault Registers in 78h For Selected Rail
ARA	R			ALERT_RESPONSE_ADDRESS	8-bit Address: 0001_1001, 19h; 7-bit Address: 0C
COMPENSATION REGISTERS					
B0h[7:0]	R/W	00h	NVM_BANK	R1	250 Steps: 1.01018x 00h = 599.0 01h = 605.1 … F9h = 7471
B1h[4:0]	R/W	00h	NVM_BANK	R2	30 Steps: 1.1x 00h = 2K 01h = 2.2 … 1Dh = 32K
B2h[4:0]	R/W	00h	NVM_BANK	R3_6PHASE	30 Steps: 1.1x 00h = 50k 01h = 55 … 1Dh =790 B2 = 1Fh, will Remove R3/C3 for all Phase Count. Larger R3 and/or smaller C3 help reduce output noise coupling. Recommend to keep R3/C3 the same values for highest phase count (Nmax) and Nmax-1 phase count for smoother transition.
B3h[4:0]	R/W	00h	NVM_BANK	R3_5PHASE	
B4h[4:0]	R/W	00h	NVM_BANK	R3_4PHASE	
B5h[4:0]	R/W	00h	NVM_BANK	R3_3PHASE	
B6h[4:0]	R/W	00h	NVM_BANK	R3_2PHASE	
B7h[4:0]	R/W	00h	NVM_BANK	R3_1PHASE	
B8h[5:0]	R/W	00h	NVM_BANK	C1	42 Steps: 1.1x 00h = 10pF 01h = 11pF … 29h = 500pF
B9h[5:0]	R/W	00h	NVM_BANK	C2	42 Steps: 1.1x 00h = 330pF 01h = 363pF … 29h = 16.4nF

TABLE 15. SMBus, PMBus, AND I^2C WRITE AND READ REGISTERS

COMMAND CODE	ACCESS	WRITE PROTECT LEVEL	DEFAULT	COMMAND NAME	DESCRIPTION
BAh[5:0]	R/W	00h	NVM_BANK	C3_6PHASE	42 Steps: 1.1x 00h = 100pF 01h = 110pF ... 29h = 5.0nF
BBh[5:0]	R/W	00h	NVM_BANK	C3_5PHASE	
BCh[5:0]	R/W	00h	NVM_BANK	C3_4PHASE	
BDh[5:0]	R/W	00h	NVM_BANK	C3_3PHASE	
BEh[5:0]	R/W	00h	NVM_BANK	C3_2PHASE	
BFh[5:0]	R/W	00h	NVM_BANK	C3_1PHASE	
DIRECT ACCESS TO EEPROM (ADVANCED USER AND TEST MODE ONLY)					
EC[7:0]	R/W	00h	00h	EEP_ADDR_REG	Give user access to EEPROM Address
ED[31:0]	BLOCK R/W	00h	ALL ZEROs	EEP_DATA_REG	User Write 4-bytes (32-bits) of data into called address by EC
EE[7:0]	R/W	00h	0000h	EEP_ACTIVATE	EEPROM Control Register Bit[0] = 1h, Start EEPROM Read Procedure Bit[1] = 1h, Start EEPROM Write Procedure Bit[5:2] - Reserved Bit[6] = 1h, Generate Total Checksum (FD data). Bit[7] = 1h, Generate Individual NVM BANK Checksum (FD data). The device will declare busy at the assertion of this command, a new command addressed to this device should be sent 300ms afterward.

NOTE: When the controller is reset by the Enable pins (TM_EN_OTP or EN_PWR_CFP), (not V_{CC}), the programmed registers will be stored in operating memory.

TABLE 16. SMBus, PMBus, AND I^2C TELEMETRIES

CODE	WORD LENGTH (BYTE)	COMMAND NAME	DESCRIPTION	TYPICAL RESOLUTION
88h[15:0]	TWO	READ_VIN	Input Voltage (25.5V = FF) Formula: HEX2DEC(Readout)*0.1V	8-BIT, 100mV
89h[15:0]	TWO	READ_IIN	Input Current (1Fh = 10µA)	5-BIT, IIN_FULL/31
8Bh[15:0]	TWO	READ_VOUT	VR Output Voltage (HEX2DEC(Readout)*0.05V)	9-BIT, 5mV
8Ch[15:0]	TWO	READ_IOUT	VR Output Current (2.5V IMON = ICCMAX) HEX2DEC(Readout)*ICCMAX/255	8-BIT, ~1A
8Dh[15:0]	TWO	READ_TEMPERATURE_1	TM Temperature (See Table 18) Approximation Formula for Table 18 (T in °C): $-0.0000221*T^3 + 0.0094935*T^2 - 1.876*T + 213.75$	8-BIT, ~1°C
96h[15:0]	TWO	READ_POUT	Output Power	~ 2W (~1A LSB @ 2V)
97h[15:0]	TWO	READ_PIN	Input Power	~12W (~1A LSB @ 12V)
78h[8:0]	ONE	STATUS_BYTE	Fault Reporting: Bit7 = Busy Bit6 = 0 Bit5 = Overvoltage; Bit4 = overcurrent, $\geq I_{MAX}$; Bit3 = 0 Bit2 = Over-temperature, $\geq T_{MAX}$; Bit1 = PMBus communication error Bit0 = SVID communication error	[BUSY, 0, OV, OC, 0, OT, PM_CML, SV_CML]
79h[15:0]	TWO	STATUS_WORD	Lower Byte Fault Reporting (78h): Bit7 = Busy Bit6 = 0 Bit5 = Overvoltage; Bit4 = overcurrent, $\geq I_{MAX}$; Bit3 = 0 Bit2 = Over-temperature, $\geq T_{MAX}$; Bit1 = PMBus communication error Bit0 = SVID communication error Upper Byte Fault Reporting: Bit7 = VOUT OV, UV, and OV/UV Warning Bit6 = IOUT OC Bit5 = INPUT OCP $\geq$ 1F (10µA); Bit[4:0] = 0	Upper Byte: [VOUT, IOUT, IIN_OCP, 0, 0, 0,0, 0] Lower Byte: [BUSY, 0, OV, OC, 0, OT, PM_CML, SV_CML]

TABLE 17. LOCK_SVID

D6h	SVID			SMBus, PMBus or I^2C		FINAL DAC	TARGETED APPLICATIONS
	setVID	setPS (1/2/3) & setDecay	set OFFSET	setVID	set OFFSET		
00h	Yes	Yes	Yes	Not	Not	SV_VID + SV_OFFSET	Not Over-clocking
00h	Yes	Yes	ACK ONLY	Not	Yes	SV_VID + PM_OFFSET	Not Over-clocking
02h	Yes	ACK ONLY	ACK ONLY	Not	Yes	SV_VID + PM_OFFSET	Over-clocking
03h	ACK ONLY	ACK ONLY	ACK ONLY	Yes	Yes	PM_VID + PM_OFFSET	Over-clocking

NOTE: The ISL6388 controller is designed to be such that all SVID commands are always acknowledged as if the SMBus, PMBus or I^2C does not exist. To avoid the conflict between SMBus/PMBus/I^2C and SVID bus during operation, the user should execute this command prior to Enable (TM_EN_OTP and EN_PWR_CFP) high or during the boot period. When operating in 01h option, SMBus/PMBus/I^2C's OFFSET should only adjust slightly higher or lower (say ±20mV) than SVID OFFSET for margining purpose or PCB loss compensation so that CPU will not draw significantly more power in PSI1/2/3/Decay mode. To program full range of PM_OFFSET for over-clocking applications, the user should select 02h or 03h options. 03h option gives users full control of the output voltage (VID+OFFSET) via SMBus/PMBus/I^2C, commonly used in over-clocking applications. Prior to a successful written PMBus VID or OFFSET, the controller will continue executing SVID VID or OFFSET command.

TABLE 18. TYPICAL TEMPERATURE (8Dh and 8Eh)

TEMPERATURE (°C)	$V_{TM(S)}$ of V_{CC} (%)	CODE (HEX)	TEMPERATURE (°C)	$V_{TM(S)}$ of V_{CC} (%)	CODE (HEX)
0	95.0	F2	71	58.9	96
1	94.8	F1	72	58.2	94
2	94.6	F1	73	57.5	92
3	94.4	F0	74	56.7	90
4	94.1	F0	75	56.0	8E
5	93.9	EF	76	55.3	8D
6	93.6	EE	77	54.6	8B
7	93.4	EE	78	53.9	89
8	93.1	ED	79	53.2	87
9	92.8	EC	80	52.4	85
10	92.6	EC	81	51.7	83
11	92.3	EB	82	51.0	82
12	92.0	EA	83	50.3	80
13	91.6	E9	84	49.6	7E
14	91.3	E8	85	48.9	7C
15	91.0	E7	86	48.2	7B
16	90.7	E7	87	47.6	79
17	90.3	E6	88	46.9	77
18	89.9	E5	89	46.2	75
19	89.6	E4	90	45.5	74
20	89.2	E3	91	44.9	72
21	88.8	E2	92	44.2	70
22	88.4	E1	93	43.5	6F
23	88.0	E0	94	42.9	6D
24	87.6	DF	95	42.3	6B
25	87.2	DE	96	41.6	6A
26	86.7	DD	97	41.0	68
27	86.3	DC	98	40.4	66
28	85.8	DA	99	39.7	65
29	85.4	D9	100	39.1	63
30	84.9	D8	101	38.5	62
31	84.4	D7	102	37.9	60
32	83.9	D6	103	37.3	5F
33	83.4	D4	104	36.7	5D
34	82.9	D3	105	36.1	5C
35	82.4	D2	106	35.5	5A
36	81.9	D0	107	35.0	59
37	81.3	CF	108	34.4	57
38	80.8	CD	109	33.9	56

TABLE 18. TYPICAL TEMPERATURE (8Dh and 8Eh) (Continued)

TEMPERATURE (°C)	$V_{TM(S)}$ of V_{CC} (%)	CODE (HEX)	TEMPERATURE (°C)	$V_{TM(S)}$ of V_{CC} (%)	CODE (HEX)
39	80.2	CC	110	33.3	54
40	79.7	CB	111	32.8	53
41	79.1	C9	112	32.2	52
42	78.5	C8	113	31.7	50
43	77.9	C6	114	31.2	4F
44	77.3	C5	115	30.7	4E
45	76.7	C3	116	30.2	4D
46	76.1	C2	117	29.7	4B
47	75.5	C0	118	29.2	4A
48	74.8	BE	119	28.7	49
49	74.2	BD	120	28.2	48
50	73.5	BB	121	27.8	46
51	72.9	B9	122	27.3	45
52	72.2	B8	123	26.9	44
53	71.6	B6	124	26.4	43
54	70.9	B4	125	26.0	42
55	70.2	B3	126	25.5	41
56	69.5	B1	127	25.1	40
57	68.8	AF	128	24.7	3E
58	68.2	AD	129	24.3	3D
59	67.5	AC	130	23.9	3C
60	66.8	AA	131	23.5	3B
61	66.1	A8	132	23.1	3A
62	65.4	A6	133	22.7	39
63	64.6	A4	134	22.3	38
64	63.9	A3	135	21.9	37
65	63.2	A1	136	21.6	36
66	62.5	9F	137	21.2	36
67	61.8	9D	138	20.8	35
68	61.1	9B	139	20.5	34
69	60.3	99	140	20.1	33
70	59.6	98			

TABLE 19. V_{OUT}_MAX (24h) VR12 MODE

V_{OUT} (V)	Code (HEX)	V_{OUT} (V)	Code (HEX)	V_{OUT} (V)	Code (HEX)
0.000	0	0.885	80	1.525	100
0.250	1	0.890	81	1.530	101
0.255	2	0.895	82	1.535	102
0.260	3	0.900	83	1.540	103
0.265	4	0.905	84	1.545	104
0.270	5	0.910	85	1.550	105
0.275	6	0.915	86	1.555	106
0.280	7	0.920	87	1.560	107
0.285	8	0.925	88	1.565	108
0.290	9	0.930	89	1.570	109
0.295	A	0.935	8A	1.575	10A
0.300	B	0.940	8B	1.580	10B
0.305	C	0.945	8C	1.585	10C
0.310	D	0.950	8D	1.590	10D
0.315	E	0.955	8E	1.595	10E
0.320	F	0.960	8F	1.600	10F
0.325	10	0.965	90	1.605	110
0.330	11	0.970	91	1.610	111
0.335	12	0.975	92	1.615	112
0.340	13	0.980	93	1.620	113
0.345	14	0.985	94	1.625	114
0.350	15	0.990	95	1.630	115
0.355	16	0.995	96	1.635	116
0.360	17	1.000	97	1.640	117
0.365	18	1.005	98	1.645	118
0.370	19	1.010	99	1.650	119
0.375	1A	1.015	9A	1.655	11A
0.380	1B	1.020	9B	1.660	11B
0.385	1C	1.025	9C	1.665	11C
0.390	1D	1.030	9D	1.670	11D
0.395	1E	1.035	9E	1.675	11E
0.400	1F	1.040	9F	1.680	11F
0.405	20	1.045	A0	1.685	120
0.410	21	1.050	A1	1.690	121
0.415	22	1.055	A2	1.695	122
0.420	23	1.060	A3	1.700	123
0.425	24	1.065	A4	1.705	124
0.430	25	1.070	A5	1.710	125
0.435	26	1.075	A6	1.715	126

TABLE 19. V_{OUT}_MAX (24h) VR12 MODE (Continued)

V_{OUT} (V)	Code (HEX)	V_{OUT} (V)	Code (HEX)	V_{OUT} (V)	Code (HEX)
0.440	27	1.080	A7	1.720	127
0.445	28	1.085	A8	1.725	128
0.450	29	1.090	A9	1.730	129
0.455	2A	1.095	AA	1.735	12A
0.460	2B	1.100	AB	1.740	12B
0.465	2C	1.105	AC	1.745	12C
0.470	2D	1.110	AD	1.750	12D
0.475	2E	1.115	AE	1.755	12E
0.480	2F	1.120	AF	1.760	12F
0.485	30	1.125	B0	1.765	130
0.490	31	1.130	B1	1.770	131
0.495	32	1.135	B2	1.775	132
0.500	33	1.140	B3	1.780	133
0.505	34	1.145	B4	1.785	134
0.510	35	1.150	B5	1.790	135
0.515	36	1.155	B6	1.795	136
0.520	37	1.160	B7	1.800	137
0.525	38	1.165	B8	1.805	138
0.530	39	1.170	B9	1.810	139
0.535	3A	1.175	BA	1.815	13A
0.540	3B	1.180	BB	1.820	13B
0.545	3C	1.185	BC	1.825	13C
0.550	3D	1.190	BD	1.830	13D
0.555	3E	1.195	BE	1.835	13E
0.560	3F	1.200	BF	1.840	13F
0.565	40	1.205	C0	1.845	140
0.570	41	1.210	C1	1.850	141
0.575	42	1.215	C2	1.855	142
0.580	43	1.220	C3	1.860	143
0.585	44	1.225	C4	1.865	144
0.590	45	1.230	C5	1.870	145
0.595	46	1.235	C6	1.875	146
0.600	47	1.240	C7	1.880	147
0.605	48	1.245	C8	1.885	148
0.610	49	1.250	C9	1.890	149
0.615	4A	1.255	CA	1.895	14A
0.620	4B	1.260	CB	1.900	14B
0.625	4C	1.265	CC	1.905	14C
0.630	4D	1.270	CD	1.910	14D

TABLE 19. V_{OUT}_MAX (24h) VR12 MODE (Continued)

V_{OUT} (V)	Code (HEX)	V_{OUT} (V)	Code (HEX)	V_{OUT} (V)	Code (HEX)
0.635	4E	1.275	CE	1.915	14E
0.640	4F	1.280	CF	1.920	14F
0.645	50	1.285	D0	1.925	150
0.650	51	1.290	D1	1.930	151
0.655	52	1.295	D2	1.935	152
0.660	53	1.300	D3	1.940	153
0.665	54	1.305	D4	1.945	154
0.670	55	1.310	D5	1.950	155
0.675	56	1.315	D6	1.955	156
0.680	57	1.320	D7	1.960	157
0.685	58	1.325	D8	1.965	158
0.690	59	1.330	D9	1.970	159
0.695	5A	1.335	DA	1.975	15A
0.700	5B	1.340	DB	1.980	15B
0.705	5C	1.345	DC	1.985	15C
0.710	5D	1.350	DD	1.990	15D
0.715	5E	1.355	DE	1.995	15E
0.720	5F	1.360	DF	2.000	15F
0.725	60	1.365	E0	2.005	160
0.730	61	1.370	E1	2.010	161
0.735	62	1.375	E2	2.015	162
0.740	63	1.380	E3	2.020	163
0.745	64	1.385	E4	2.025	164
0.750	65	1.390	E5	2.030	165
0.755	66	1.395	E6	2.035	166
0.760	67	1.400	E7	2.040	167
0.765	68	1.405	E8	2.045	168
0.770	69	1.410	E9	2.050	169
0.775	6A	1.415	EA	2.055	16A
0.780	6B	1.420	EB	2.060	16B
0.785	6C	1.425	EC	2.065	16C
0.790	6D	1.430	ED	2.070	16D
0.795	6E	1.435	EE	2.075	16E
0.800	6F	1.440	EF	2.080	16F
0.805	70	1.445	F0	2.085	170
0.810	71	1.450	F1	2.090	171
0.815	72	1.455	F2	2.095	172
0.820	73	1.460	F3	2.100	173
0.825	74	1.465	F4	2.105	174

TABLE 19. V_{OUT}_MAX (24h) VR12 MODE (Continued)

V_{OUT} (V)	Code (HEX)	V_{OUT} (V)	Code (HEX)	V_{OUT} (V)	Code (HEX)
0.830	75	1.470	F5	2.110	175
0.835	76	1.475	F6	2.115	176
0.840	77	1.480	F7	2.120	177
0.845	78	1.485	F8	2.125	178
0.850	79	1.490	F9	2.130	179
0.855	7A	1.495	FA	2.135	17A
0.860	7B	1.500	FB	2.140	17B
0.865	7C	1.505	FC	2.145	17C
0.870	7D	1.510	FD	2.150	17D
0.875	7E	1.515	FE	2.155	17E
0.880	7F	1.520	FF		

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs, which include schematics, bills of materials, and example board layouts for common microprocessor applications.

Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily upon the cost analysis, which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power supply circuitry. Generally speaking, the most economical solutions are those in which each phase handles between 15A and 25A. All surface mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat dissipating surfaces.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow.

Lower MOSFET Power Calculation

The calculation for heat dissipated in the lower MOSFET is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). Equation 33, I_M is the maximum continuous output current; I_{P-P} is the peak-to-peak inductor current (see Equation 1 on page 15); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance.

$$P_{LOW,1} = r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 + \frac{I_{P-P}^2}{12}\right]\cdot(1-d) \quad \text{(EQ. 33)}$$

An additional term can be added to the lower MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, F_{SW}; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)}F_{SW}\left[\left(\frac{I_M}{N}+\frac{I_{P-P}}{2}\right)t_{d1} + \left(\frac{I_M}{N}-\frac{I_{P-P}}{2}\right)t_{d2}\right] \quad \text{(EQ. 34)}$$

Finally, the power loss of output capacitance of the lower MOSFET is approximated in Equation 35:

$$P_{LOW,3} \approx \frac{2}{3}\cdot V_{IN}^{1.5}\cdot C_{OSS\_LOW}\cdot\sqrt{V_{DS\_LOW}}\cdot F_{SW} \quad \text{(EQ. 35)}$$

where C_{OSS_LOW} is the output capacitance of lower MOSFET at the test voltage of V_{DS_LOW}. Depending on the amount of ringing, the actual power dissipation will be slightly higher than this.

Thus, the total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$, $P_{LOW,2}$ and $P_{LOW,3}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper-0MOSFET losses can be divided into separate components involving the upper MOSFET switching times; the lower MOSFET body-diode reverse-recovery charge, Q_{rr}; and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 36, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{N}+\frac{I_{P-P}}{2}\right)\left(\frac{t_1}{2}\right)F_{SW} \quad \text{(EQ. 36)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 37, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{N}-\frac{I_{P-P}}{2}\right)\left(\frac{t_2}{2}\right)F_{SW} \quad \text{(EQ. 37)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower MOSFET's body diode can draw all of Q_{rr}, it is conducted through the upper MOSFET across V_{IN}. The power dissipated as a result is $P_{UP,3}$ and is approximated in Equation 38:

$$P_{UP,3} = V_{IN}Q_{rr}F_{SW} \quad \text{(EQ. 38)}$$

The resistive part of the upper MOSFET's is given in Equation 39 as $P_{UP,4}$.

$$P_{UP,4} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 + \frac{I_{P-P}^2}{12}\right]\cdot d \quad \text{(EQ. 39)}$$

Equation 40 accounts for some power loss due to the drain-source parasitic inductance (L_{DS}, including PCB parasitic inductance) of the upper MOSFETs, although it is not the exact:

$$P_{UP,5} \approx L_{DS}\left(\frac{I_M}{N}+\frac{I_{P-P}}{2}\right)^2 \quad \text{(EQ. 40)}$$

Finally, the power loss of output capacitance of the upper-MOSFET is approximated in Equation 41:

$$P_{UP,6} \approx \frac{2}{3}\cdot V_{IN}^{1.5}\cdot C_{OSS\_UP}\cdot\sqrt{V_{DS\_UP}}\cdot F_{SW} \quad \text{(EQ. 41)}$$

where C_{OSS_UP} is the output capacitance of lower MOSFET at test voltage of V_{DS_UP}. Depending on the amount of ringing, the actual power dissipation will be slightly higher than this.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 36 to 41. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Current Sensing Resistor

The resistors connected to the ISEN+ pins determine the gains in the load-line regulation loop and the channel current balance loop as well as setting the overcurrent trip point. Select values for these resistors by using Equation 42:

$$R_{ISEN} = \frac{R_X}{100\times10^{-6}}\frac{I_{OCP}}{N} \quad \text{(EQ. 42)}$$

where R_{ISEN} is the sense resistor connected to the ISEN+ pin, N is the active channel number, R_X is the resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method, and I_{OCP} is the desired overcurrent trip point. Typically, I_{OCP} can be chosen to be 1.2 times the maximum load current of the specific application.

With integrated temperature compensation, the sensed current signal is independent of the operational temperature of the power stage, i.e. the temperature effect on the current sense element R_X is cancelled by the integrated temperature compensation function. R_X in Equation 42 should be the resistance of the current sense element at room temperature.

When the integrated temperature compensation function is disabled by selecting "OFF" TCOMP code, the sensed current will be dependent on the operational temperature of the power stage, since the DC resistance of the current sense element may be changed according to the operational temperature. R_X in Equation 42 should be the maximum DC resistance of the current sense element at the all operational temperature.

In certain circumstances, especially for a design with an unsymmetrical layout, it may be necessary to adjust the value of one or more ISEN resistors for VR. When the components of one or more channels are inhibited from effectively dissipating their heat so that the affected channels run cooler than the average, choose new, larger values of R_{ISEN} for the affected phases (see the section entitled "Current Sensing" on page 18). Choose $R_{ISEN,2}$ in proportion to the desired increase in temperature rise in order to cause proportionally more current to flow in the cooler phase, as shown in Equation 43:

$$R_{ISEN,2} = R_{ISEN}\frac{\Delta T_2}{\Delta T_1} \quad \text{(EQ. 43)}$$

$$\Delta R_{ISEN} = R_{ISEN,2} - R_{ISEN}$$

In Equation 43, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. Since all channels' R_{ISEN} are integrated and set by one RSET, a resistor (ΔR_{ISEN}) can be in series with the cooler channel's ISEN+ pin to raise this phase current. However, the ISL6388 can adjust the thermal/current balance of the VR via registers F7 to FC.

Load-Line Regulation Resistor

The load-line regulation resistor is labelled R_{FB} in Figure 11. Its value depends on the desired loadline requirement of the application.

The desired loadline can be calculated using Equation 44:

$$R_{LL} = \frac{V_{DROOP}}{I_{FL}} \quad \text{(EQ. 44)}$$

where I_{FL} is the full load current of the specific application, and VR_{DROOP} is the desired voltage droop under the full load condition.

Based on the desired loadline R_{LL}, the loadline regulation resistor can be calculated using Equation 45:

$$R_{FB} = \frac{N \cdot R_{ISEN} \cdot R_{LL}}{R_X} \quad \text{(EQ. 45)}$$

where N is the active channel number, R_{ISEN} is the sense resistor connected to the ISEN+ pin, and R_X is the resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method.

If one or more of the current sense resistors are adjusted for thermal balance (as in Equation 43), the load-line regulation resistor should be selected based on the average value of the current sensing resistors, as given in Equation 46:

$$R_{FB} = \frac{R_{LL}}{R_X}\sum_n R_{ISEN(n)} \quad \text{(EQ. 46)}$$

where $R_{ISEN(n)}$ is the current sensing resistor connected to the n^{th} ISEN+ pin.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, DI; the load current slew rate, di/dt; and the maximum allowable output voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount, as shown in Equation 47:

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 47)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.The ESR of the bulk capacitors also creates the majority of the output voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see "Interleaving" on page 15 and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C(P-P)}$ (ESR).

Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance, as shown in Equation 48.

$$L \geq ESR \cdot \frac{V_{OUT} \cdot K_{RCM}}{F_{SW} \cdot V_{IN} \cdot V_{P\text{-}P(MAX)}} \quad \text{(EQ. 48)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 49 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 50 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_{OUT}}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right] \quad \text{(EQ. 49)}$$

$$L \leq \frac{1.25 \cdot N \cdot C}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right]\left(V_{IN} - V_{OUT}\right) \quad \text{(EQ. 50)}$$

Switching Frequency Selection

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper-MOSFET loss calculation. These effects are outlined in "MOSFETs" on page 51, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output voltage ripple as outlined in "Output Filter Design" on page 53. Choose the lowest switching frequency that allows the regulator to meet the transient-response and output voltage ripple requirements.

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases. The input RMS current can be calculated with Equation 51.

$$I_{IN,\,RMS} = \sqrt{K_{IN,\,CM}^2 \bullet Io^2 + K_{RAMP,\,CM}^2 \bullet I_{Lo,\,PP}^2} \quad \text{(EQ. 51)}$$

$$K_{IN,\,CM} = \sqrt{\frac{(N \bullet D - m + 1) \bullet (m - N \bullet D)}{N^2}} \quad \text{(EQ. 52)}$$

$$K_{RAMP,\,CM} = \sqrt{\frac{m^2(N \bullet D - m + 1)^3 + (m-1)^2(m - N \bullet D)^3}{12N^2D^2}} \quad \text{(EQ. 53)}$$

For a 2-phase design, use Figure 37 to determine the input capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the per-phase peak-to-peak inductor current ($I_{L(P\text{-}P)}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25x greater than the maximum input voltage.

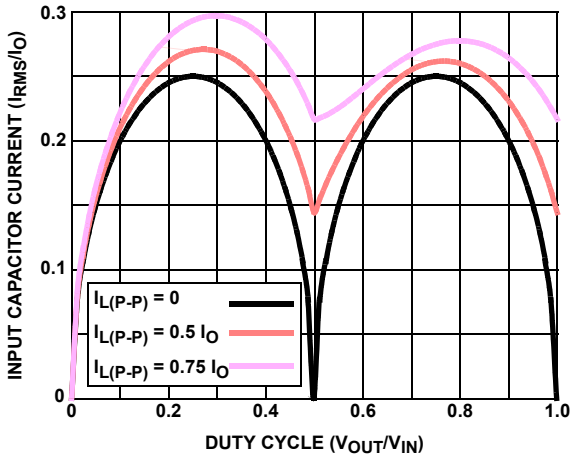


FIGURE 37. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

Figures 38 and 39 provide the same input RMS current information for 3 and 4-phase designs respectively. Use the same approach to selecting the bulk capacitor type and number as previously described.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result from the high current slew rates produced by the upper MOSFETs turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize noise suppression.

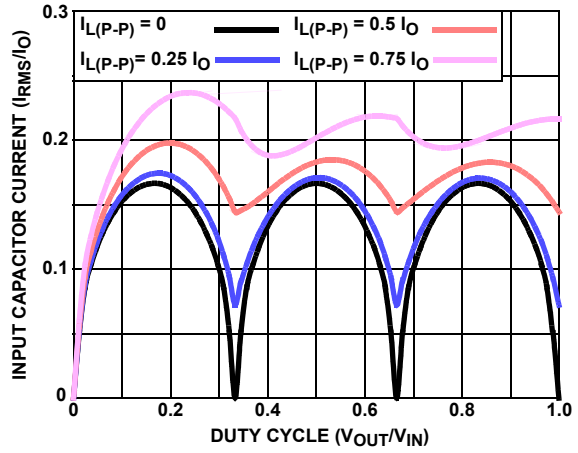


FIGURE 38. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER

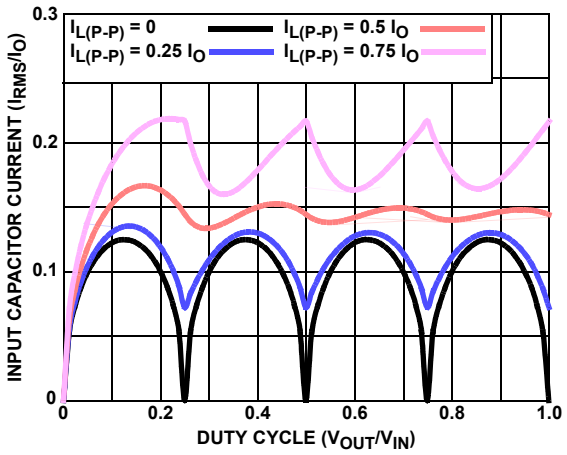


FIGURE 39. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

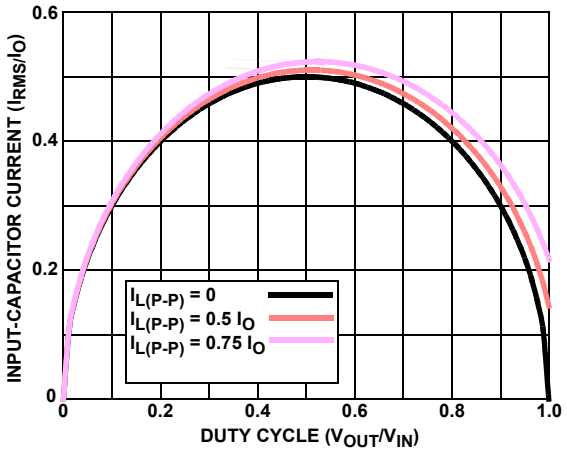


FIGURE 40. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

Figure 40 is provided as a reference to demonstrate the dramatic reductions in input capacitor RMS current upon the implementation of the multiphase topology. For example, compare the input RMS current requirements of a 2-phase converter versus that of a single phase. Assume both converters have a duty cycle of 0.25, maximum sustained output current of 40A, and a ratio of $I_{L(P-P)}$ to I_O of 0.5. The single phase converter would require 17.3A_{RMS} current capacity while the 2-phase converter would only require 10.9A_{RMS}. The advantages become even more pronounced when output current is increased and additional phases are added to keep the component cost down relative to the single phase approach.

Layout and Design Considerations

The following layout and design strategies are intended to minimize the noise coupling, the impact of board parasitic impedances on converter performance and to optimize the heat dissipating capabilities of the printed circuit board. This section highlights some important practices which should be followed during the layout process. A layout check list is available for use.

Pin Noise Sensitivity, Design and Layout Consideration

Table 20 shows the noise sensitivity of each pin and their design and layout consideration. All pins and external components should NOT be across switching nodes and should be placed in general proximity to the controller.

TABLE 20. PIN DESIGN AND/OR LAYOUT CONSIDERATION

PIN NAME	NOISE SENSITIVE	DESCRIPTION
ISENIN-	Yes	Connect to input supply side of the input inductor or resistor pin with L/DCR or ESL/R matching network in close proximity to the controller. Place NTC in the close proximity to input inductor for thermal compensation. A local 10nF decoupling capacitor between ISENIN+ and ISENIN- is preferred. DCR sensing with thermal compensation will yield no load offset reading. Resistor sensing is preferred for accurate input current reporting. > 40µs time constant $[C*R_{IN1}*R_{IN2})/(R_{IN1}+R_{IN2})]$ might be needed if the average input current reporting is preferred; and it also reduces chance to trigger CFP during heavy load transient.
ISENIN+	Yes	Connects to the Drain of High-side MOSFET side of the input inductor or resistor pin. A local 0.1µF ceramic capacitor is recommended. When not used, connect ISENIN+ to VIN and a resistor divider with a ratio of 1/3 on ISENIN± pin, say 499kΩ in between ISENIN± pins and then 1.5MΩ from ISENIN- to ground (see Figure 29). The voltage of this pin is used feed-forward compensation.
EN_PWR_CFP	Yes	There is an internal 1µs filter. Decoupling capacitor is NOT needed, but if needed, use a low time constant one to avoid too long of a shutdown delay. It is be the output of CFP function: 34Ω strong pull-up. The 25 mils spacing from other traces.
RGND	Yes	Pair up (within 20 mils) with the positive rail remote sensing line that connected to VSEN pin, and routing them to the load sensing points.
VSEN	Yes	Pair up (within 20 mils) with the negative rail of remote sensing line that connected to RGND, and route them to the load sensing points. It is the APA level input sensing as well.
VSEN_OVP	Yes	Used for Overvoltage protection sensing.

TABLE 20. PIN DESIGN AND/OR LAYOUT CONSIDERATION (Continued)

PIN NAME	NOISE SENSITIVE	DESCRIPTION
VRSEL_ADDR NVM_BANK_BT	No	Register setting is locked prior to soft-start. Since the external resistor-divider ratio compares with the internal resistor ratio of the V_{CC}, their rail should be exactly tied to the same point as VCC pin, not through an RC filter. DO NOT use decoupling capacitors on these pins.
VR_RDY	No	Open drain and high dv/dt pin. Avoid its pull-up higher than V_{CC}. Leave it open or tie it ground when not used.
IMON	Yes	Refer to GND, not RGND. Place R and C in general proximity to the controller. The time constant of RC is typically ~ 150µs for VR12.5 server core 1-2ms for desktop core applications, as an averaging function for the digital I_{OUT}.
SVDATA; SVCLK	Yes	Greater than 13MHz signals when the SVID bus is sending commands, pairing up with SVALERT# and routing carefully back to CPU socket. 20 mils spacing within SVDATA, SVALERT#, and SVCLK; and more than 30 mils to all other signals. Refer to the Intel individual platform design guidelines and place proper termination (pull-up) resistance for impedance matching. Local decoupling capacitor is needed for the pull-up rail. Ground them when not used.
SVALERT#	No	Open drain and high dv/dt pin during transitions. Route it in the middle of SVDATA and SVCLK. Also see above. Leave it open or tie it ground when not used.
VR_HOT#	No	Open drain and high dv/dt pin during transitions. Avoid its pull-up rail higher than V_{CC}. 30 mils spacing from other traces.
SM_PM_I2CL SM_PM_I2DA	Yes	50kHz to 1.5MHz signal when the SMBus, PMBus, or I^2C is sending commands, pairing up with PMALERT# and routing carefully back to SMBus, PMBus or I^2C. The 20 mils spacing within I2DATA, PMALERT#, and I2CLK; and more than 30 mils to all other signals. Refer to the SMBus, PMBus or I^2C design guidelines and place proper terminated (pull-up) resistance for impedance matching. Ground them when not used.
PMALERT#	No	Open drain and high dv/dt pin during transitions. Route it in the middle of I2DATA and I2LK. Also see above. Leave it open or tie it ground when not used.
BUF_COMP	Yes	Buffer output of internal Comp Signal.

TABLE 20. PIN DESIGN AND/OR LAYOUT CONSIDERATION (Continued)

PIN NAME	NOISE SENSITIVE	DESCRIPTION
TM_EN_OTP	Yes	Place NTC in close proximity to the output inductor of Channel 1 and to the output rail, not close to MOSFET side (see Figure 24); the return trace should be 25 mils away from other traces. Place 1kΩ pull-up and decoupling capacitor (typically 0.1µF) in close proximity to the controller. The pull-up resistor should be exactly tied to the same point as VCC pin, not through an RC filter. If not used, connect this pin to 1MΩ/2MΩ resistor divider, or tie to V_{CC}.
AUTO	Yes	Program number of operational phases in PSI1 mode and AUTO phase shedding threshold a resistor from this pin to GND. AUTO phase shedding is disabled when this pin tied to GND.
RSET	Yes	Place the R in close proximity to the controller. DON'T use decoupling capacitor on this pin.
VCC	Yes	Place a high quality ceramic capacitor (~ 1µF) in close proximity to the controller.
PWM1-6	NO	Avoid the respective PWM routing across or under other phase's power trains/planes and current sensing network. Don't make them across or under external components of the controller. Keep them at least 20 mils away from any other traces.
ISEN[6:1]+	Yes	Connect to the output rail side of the respective channel's output inductor or resistor pin. Decoupling is optional and might be required for long sense traces and a poor layout.
ISEN[6:1]-	Yes	Connect to the phase node side of the respective channel's output inductor or resistor with L/DCR or ESL/R_{SEN} matching network in close proximity to the ISEN± pins of VR. Differentially routing back to the controller by paring with respective ISEN+; at least 20 mils spacing between pairs and away from other traces. Each pair should not cross or go under the other channel's switching nodes [PHASE, UGATE, LGATE] and power planes even though they are not in the same layer.
GND	Yes	This EPAD is the return of PWM output drivers and SVID bus. Use 4 or more vias to directly connect the EPAD to the power ground plane. Avoid using only single via or 0Ω resistor connection to the power ground plane.
General Comments		The layer next to the Top or Bottom layer is preferred to be ground players, while the signal layers can be sandwiched in the ground layers if possible.

Component Placement

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized while creating the PHASE plane. Place the Intersil MOSFET driver IC as close as possible to the MOSFETs they control to reduce the parasitic impedances due to trace length between critical driver input and output signals. If possible, duplicate the same placement of these components for each phase.

Next, place the input and output capacitors. Position the high-frequency ceramic input capacitors next to each upper-MOSFET drain. Place the bulk input capacitors as close to the upper-MOSFET drains as dictated by the component size and dimensions. Long distances between input capacitors and MOSFET drains result in too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductors and the load, while keeping ceramic capacitors in close proximity to the microprocessor socket.

To improve the chance of first pass success, it is very important to take time to follow the above outlined design guidelines and Intersil generated layout check list, see more details in “Voltage-Regulator (VR) Design Materials” on page 57. Proper planning for the layout is as important as designing the circuits. Running things in a hurry, you could end up spending weeks and months to debug a poorly designed and improperly laid out board.

Powering Up And Open-Loop Test

The ISL6388 features very easy debugging and powering up. For first time powering up, an open-loop test can be done by applying sufficient voltage (current limiting to 0.25A) to V_{CC}, proper pull-up to SVID bus, and signal high to TM_EN_OTP (>1.05V) and EN_PWR_CFP (>0.9V and less than 3.5V) pins with the input voltage (V_{IN}) disconnected.

1. Each PWM output should operate at maximum duty cycle and correct switching frequency.
2. Read data in 0C/DC and 0D/DD of SVID/PMBus to confirm its proper setting.
3. If 5V drivers are used and share the same rail as VCC, the proper switching on UGATEs and LGATEs should be seen.
4. If 12V drivers are used and can be disconnected from VIN and sourced by an external 12V supply, the proper switching on UGATEs and LGATEs should be observed.
5. If the above is not properly operating, you should check soldering joint, resistor register setting, Power Train connection or damage, i.e, shorted gates, drain and source. Sometimes the gate might measure short due to residual gate charge. Therefore, a measured short gate with ohmmeter cannot validate if the MOSFET is damaged unless the Drain to Source is also measured short.
6. When re work is needed for the L/DCR matching network, use an ohmmeter across the C to see if the correct R value is measured before powering the VR up; otherwise, the current imbalance due to improper re-work could damage the power trains.
7. After everything is checked, apply low input voltage (1-5V) with appropriate current limiting (~0.5A). All phases should be switching evenly when AUTO disabled.
8. Remove the pull-up from EN_PWR_CFP pin, using bench power supplies, power-up VCC with current limiting (typically ~ 0.25A if 5V drivers included) and slowly increase input voltage with current limiting. For typical application, V_{CC} limited to 0.25A, V_{IN} limited to 0.5A should be safe for powering up with no load. High core-loss inductors likely need to increase the input current limiting. All phases should be switching evenly.

Voltage-Regulator (VR) Design Materials

To support VR design and layout, Intersil also developed a set of worksheets and evaluation boards, as listed in Tables 21 and 22, respectively. The tolerance band calculation (TOB) worksheets for VR output regulation and IMON have been developed using the Root-Sum-Squared (RSS) method with 3 sigma distribution point of the related components and parameters. Note that the “Electrical Specifications” on page 10 specifies no less than 6 sigma distribution point, not suitable for RSS TOB calculation. Contact Intersil’s local office or field support for the latest available information.

TABLE 21. AVAILABLE DESIGN ASSISTANCE MATERIALS

ITEM	DESCRIPTION
0	VR12.5 Design and Validation
1	VR12.5 Design Worksheet for Component Selection
2	SMBus/PMBus/I^2C Communication Tool with Software
3	Resistor Register Calculator
4	Layout Design Guidelines
5	Evaluation Board Schematics in OrCAD Format and Layout in Allegro Format

NOTE: For worksheets, please contact Intersil Application support at www.intersil.com/design/.

TABLE 22. AVAILABLE EVALUATION BOARDS

EVALUATION BOARDS	PIN-TO-PIN	PACKAGE	SOCKET	TARGETED APPLICATIONS	SMBus/ PMBus/I^{2}C	PEAK EFFICIENCY	ICCMAX (A)
ISL6388EVAL1Z		40Ld 5x5	R3	High-End Desktop/Server with DrMOS Digital Compensation with NVM	Yes	95%, 1.8V at 50A	215A
ISL6376EVAL2Z		48Ld 6x6	R3	VR12.5 High-End Desktop and Server with DrMOS	Yes	95%, 1.8V at 50A	215A
ISL6374EVAL1Z	ISL6375/73	40Ld 5x5	H3	VR12.5 Desktop/Server with Dual PowerPak and DPAK Footprint	No	89%, 1.8V at 40A	120A
ISL6373EVAL1Z	ISL6374/75	5x5 40Ld	DDR4	VR12/VR12.5 Memory with Discrete Drivers and Dual MOSFETs (Configured to 2-Phase for Memory)	Yes	93%, 1.2V at 40A	74A
ISL6373EVAL2Z	ISL6374/75	40Ld 5x5	DDR4	VR12/VR12.5 Memory with DrMOS (Configured to 2-Phase for Memory)	Yes	93%, 1.2V at 40A	60A
ISL6367_67HEVAL1Z		60Ld 7x7	R	VR12/VR12.5 High-End Desktop and Server with Discrete Drivers and MOSFETs	Yes	94%, 1.8V at 50A 93%, 1.2V at 50A	220A +25A
ISL6367_67HEVAL2Z		60Ld 7x7	R1	VR12/VR12.5 High-End Desktop and Server with DrMOS	Yes	95%, 1.8V at 50A 93%,1.2V at 50A	220A +25A
ISL6364AEVAL1Z		48Ld 6x6	H1	VR12 Desktop/Server (Vcore or Memory)	No	88%, 1.2V at 50A	120A +35A
ISL6363EVAL1Z		60Ld 7x7	H1	Desktop/Memory	No	88%, 1.2V at 50A	120A +35A
ISL6353EVAL1Z		40Ld 5x5	DDR3	Memory	No	94%, 1.5V at 25A	100A

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
April 15, 2014	FN8571.0	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

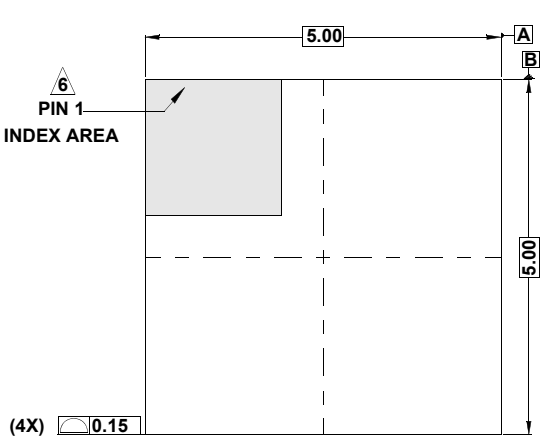
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

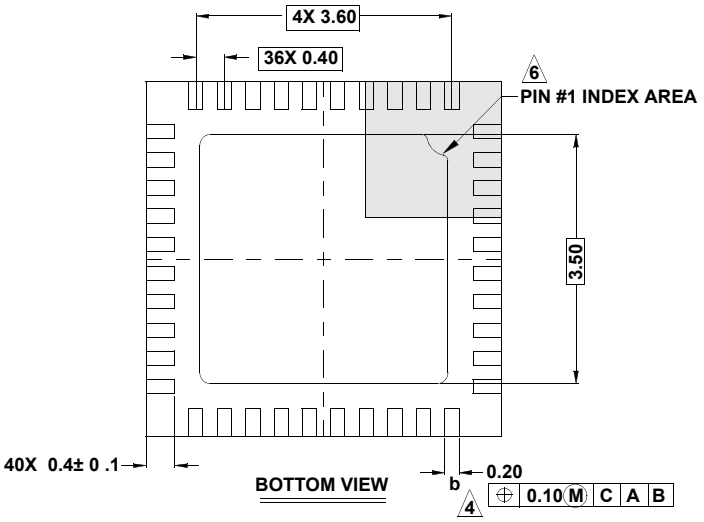
Package Outline Drawing

L40.5x5

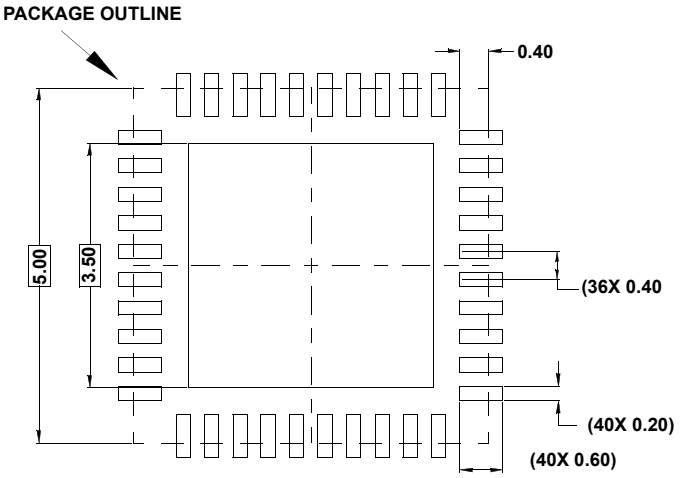
40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 9/10



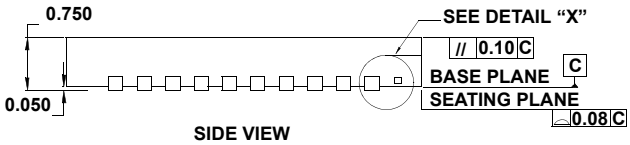
TOP VIEW



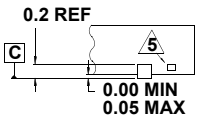
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220WHHE-1