

N-Channel Enhancement-Mode Power Field-Effect Transistor

August 1991

Features

- 19A, 100V
- $r_{DS(on)} = 0.1\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

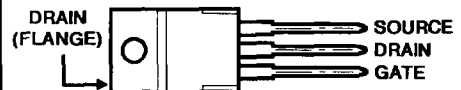
Description

The BUZ21 is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ21 is supplied in the JEDEC TO-220AB plastic package.

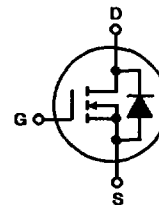
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	BUZ21	UNITS
Drain-Source Voltage	100	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)	100	V
Continuous Drain Current $T_C = +55^\circ\text{C}$	19	A
Pulsed Drain Current $T_C = +25^\circ\text{C}$	75	A
Single Pulse Avalanche Energy*, EAS	230	mj
Gate-Source Voltage	± 20	V
Maximum Power Dissipation $T_C = +25^\circ\text{C}$	75	W
Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$
DIN Humidity Category - DIN 40040	E	
IEC Climatic Category - DIN IEC 68-1	55/150/56	

* $V_{DD} = 25\text{V}$, starting $T_j = 25^\circ\text{C}$, $L = 440\mu\text{H}$, $R_{GS} = 50\Omega$, $I_{peak} = 28\text{A}$, see Figures 14 and 15.

Specifications BUZ21

ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTICS		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BVDSS	VGS = 0 V ID = 0.25 mA	100	-	-	V
Gate-Threshold Voltage	VGS(th)	VDS = VGS ID = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	IDSS	Tj = 25°C Tj = 125°C VDS = 100 V, VGS = 0 V	-	20 100	250 1000	μA
Gate-Source Leakage Current	IGSS	VGS = 20 V VDS = 0 V	-	10	100	nA
Drain-Source on Resistance	rDS(on)	VGS = 10 V ID = 9 A	-	0.09	0.1	Ω
Forward Transconductance	gfs	VDS = 25 V ID = 9 A	4	8	-	S
Input Capacitance	Ciss	VGS = 0 V	-	1500	2000	pF
Output Capacitance	Coss	VDS = 25 V	-	450	700	
Reverse Transfer Capacitance	Crss	f = 1 MHz	-	150	240	
Turn-On Time ton (ton = td(on) + tr)	td(on) tr	Vcc = 30 V ID = 3 A	-	30 50	45 75	ns
Turn-Off Time toff (toff = td(off) + tr)	td(off) tr	VGS = 10 V RGS = 50 Ω	-	170 80	220 110	
Thermal Resistance, Junction-to-Case	RθJC		≤ 1.67			
Thermal Resistance, Junction-to-Ambient	RθJA		≤ 75			

*VDD = 25 V, starting Tj = 25°C, L = 440 μHy, Rgs = 50 Ω, Ipeak = 28 A, see figure 14 & 15.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	IDR	Tc = 25°C	-	-	19	A
Pulsed Reverse Drain Current	IDRM		-	-	75	
Diode Forward Voltage	VSD	IF = 2 x IDR VGS = 0 V, Tj = 25°C	-	1.5	2.1	V
Reverse Recovery Time	trr	Tj = 25°C, IF = IDR	-	200	-	ns
Reverse Recovered Charge	QRR	dIF/dt = 100 A/μs, VR = 30 V	-	0.25	-	μC

4
N-CHANNEL
POWER MOSFETs

BUZ21

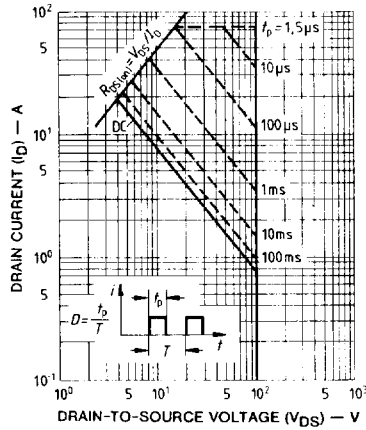


Figure 1 - Maximum safe operating areas for all types.

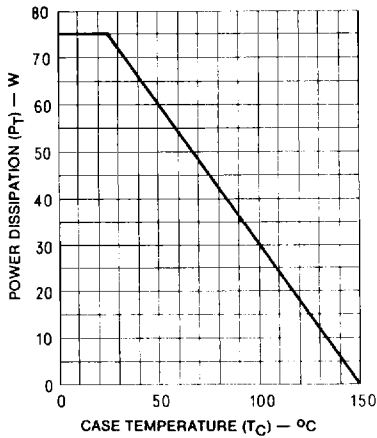


Figure 2 - Power vs temperature derating curve for all types.

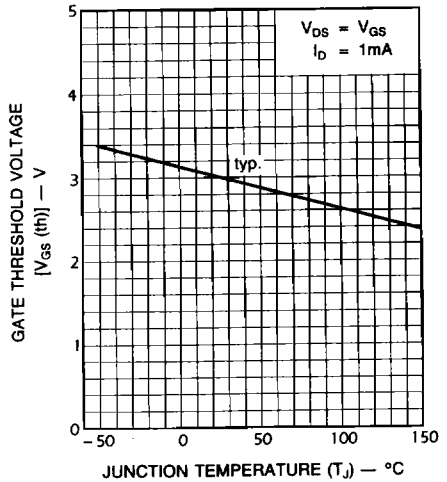


Figure 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

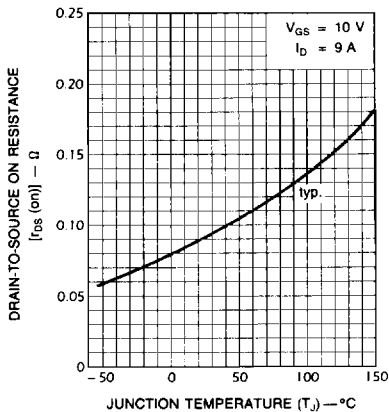


Figure 4 - Normalized drain-to-source on resistance to junction temperature for all types.

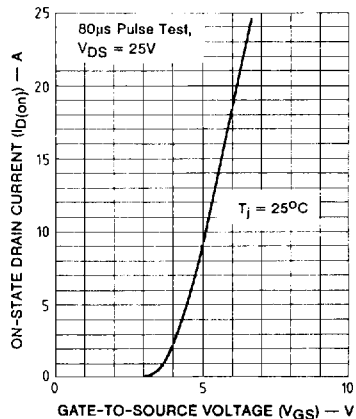


Figure 5 - Typical transfer characteristics for all types.

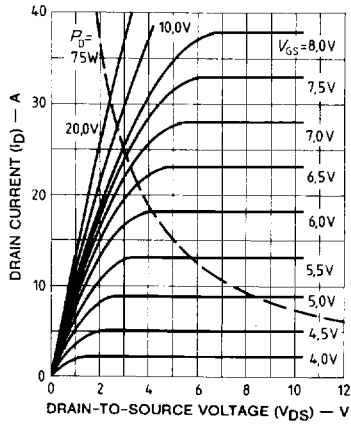


Figure 6 - Typical output characteristics.

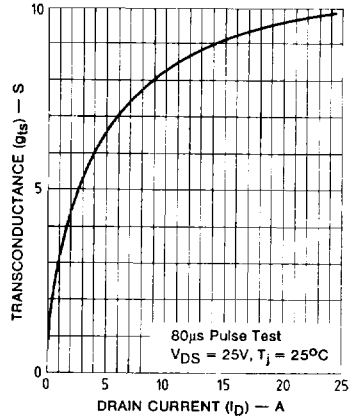


Figure 7 - Typical transconductance vs drain current.

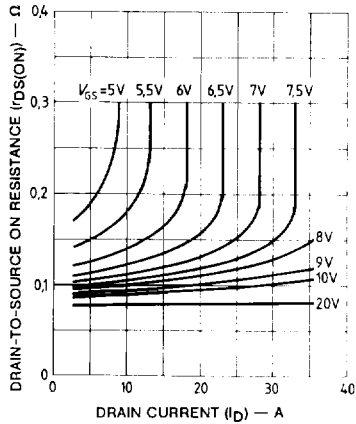


Figure 8 - Typical on-resistance vs drain current.

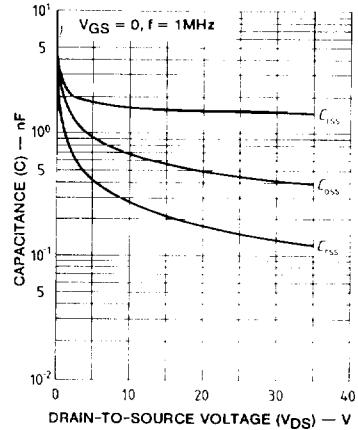


Figure 9 - Typical capacitance vs drain-to-source voltage.

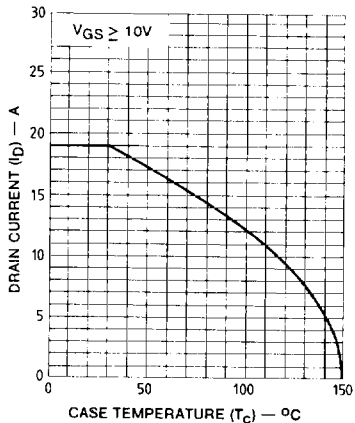


Figure 10 - Maximum drain current vs case temperature.

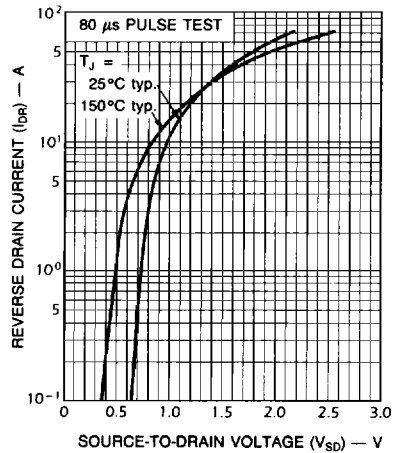


Figure 11 - Typical source-drain diode forward voltage.

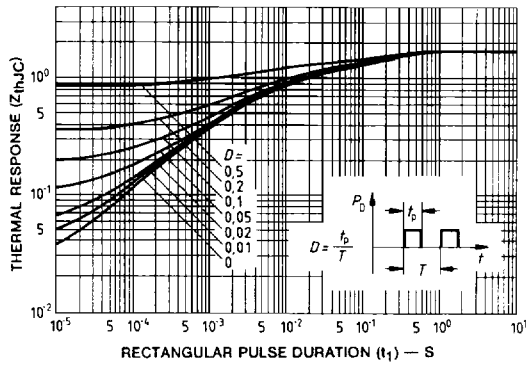


Figure 12 - Maximum effective transient thermal impedance, junction-to-case vs pulse duration

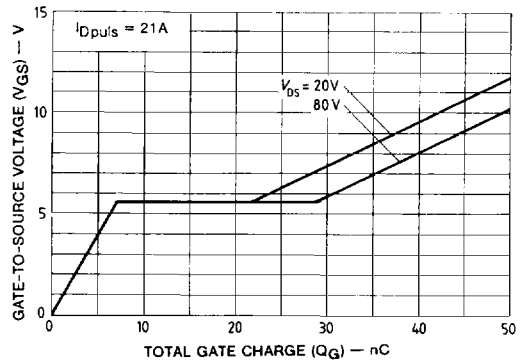


Figure 13 - Typical gate charge vs gate-to-source voltage.

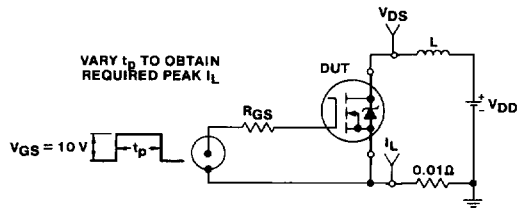


Figure 14 - Unclamped energy test circuit.

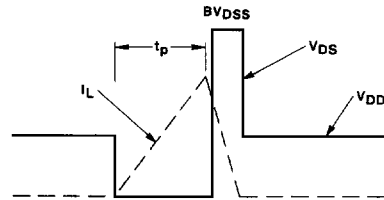


Figure 15 - Unclamped energy test waveforms.