

**FEATURES**

**Four Complete Voltage Output DACs**  
**Data Register Readback Feature**  
**"Reset to Zero" Override**  
**Multiplying Operation**  
**Double-Buffered Latches**  
**Surface Mount and DIP Packages**  
**MIL-STD-883 Compliant Versions Available**

**APPLICATIONS**

**Automatic Test Equipment**  
**Robotics**  
**Process Control**  
**Disk Drives**  
**Instrumentation**  
**Avionics**

**PRODUCT DESCRIPTION**

The AD664 is four complete 12-bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double-buffered input latch structure and a data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port.

The I/O port accommodates 4-, 8- or 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response by the outputs to the input data.

The analog portion of the AD664 consists of four DAC cells, four output amplifiers, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range, with a gain of one or two times the reference voltage. All DACs are operated from a single external reference.

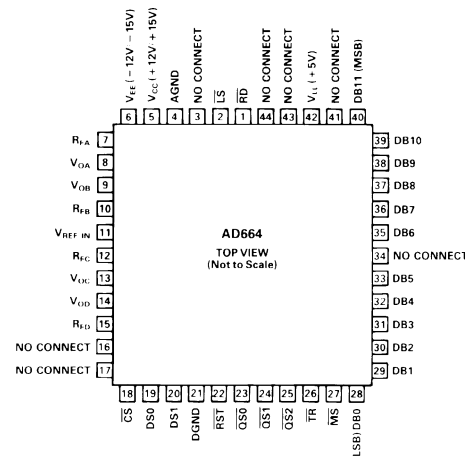
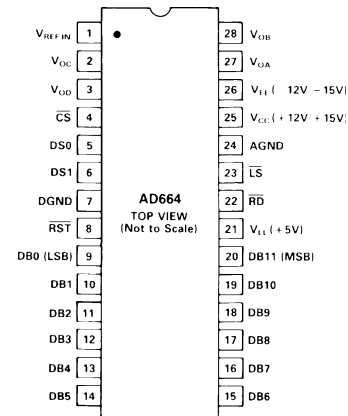
The functional completeness of the AD664 results from the combination of Analog Devices' BiMOS II process, laser-trimmed thin-film resistors and double-level metal interconnects.

**PRODUCT HIGHLIGHTS**

1. The AD664 provides four voltage-output DACs on one chip offering the highest density 12-bit D/A function available.
2. The output range of each DAC is fully and independently programmable.
3. Readback capability allows verification of contents of the internal data registers.

**REV. C**

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**PIN CONFIGURATIONS**
**44-Pin Package**

**28-Pin DIP Package**


4. The asynchronous RESET control returns all D/A outputs to zero volts.
5. DAC-to-DAC matching performance is specified and tested.
6. Linearity error is specified to be 1/2 LSB at room temperature and 3/4 LSB maximum for the K, B and T grades.
7. DAC performance is guaranteed to be monotonic over the full operating temperature range.
8. Readback buffers have tristate outputs.
9. Multiplying-mode operation allows use with fixed or variable, positive or negative external references.
10. The AD664 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD664/883B data sheet for detailed specifications.

# AD664—SPECIFICATIONS ( $V_{LL} = +5\text{ V}$ , $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $V_{REF} = +10\text{ V}$ , $T_A = +25^\circ\text{C}$ unless otherwise noted)

Model	JN/JP/AD/AJ/SD			KN/KP/BD/BJ/BE/TD/TE			Units
	Min	Typ	Max	Min	Typ	Max	
RESOLUTION		12	12		*	*	Bits
ANALOG OUTPUT							
Voltage Range <sup>1</sup>							
UNI Versions	0		$V_{CC} - 2.0^2$	*		*	Volts
BIP Versions	$V_{EE} + 2.0^2$		$V_{CC} - 2.0^2$	*		*	Volts
Output Current	5			*			mA
Load Resistance		2			*		k $\Omega$
Load Capacitance			500			*	pF
Short-Circuit Current		25	40		*	*	mA
ACCURACY							
Gain Error	-7	$\pm 3$	7	-5	$\pm 2$	5	LSB
Unipolar Offset	-2	$\pm 1/2$	2	-1	$\pm 1/4$	1	LSB
Bipolar Zero <sup>3</sup>	-3	$\pm 3/4$	3	-2	$\pm 1/2$	2	LSB
Linearity Error <sup>4</sup>	-3/4	$\pm 1/2$	3/4	-1/2	$\pm 1/4$	1/2	LSB
Linearity $T_{MIN}$ to $T_{MAX}$	-1	$\pm 3/4$	1	-3/4	$\pm 1/2$	3/4	LSB
Differential Linearity	-3/4		3/4	-1/2		1/2	LSB
Differential Linearity $T_{MIN}$ to $T_{MAX}$	<b>Monotonic @ All Temperatures</b>			<b>Monotonic @ All Temperatures</b>			
Gain Error Drift							
Unipolar 0 V to +10 V Mode	-12	$\pm 7$	12	-10	$\pm 5$	10	ppm of FSR <sup>5</sup> /°C
Bipolar -5 V to +5 V Mode	-12	$\pm 7$	12	-10	$\pm 5$	10	ppm of FSR/°C
Bipolar -10 V to +10 V Mode	-12	$\pm 7$	12	-10	$\pm 5$	10	ppm of FSR/°C
Unipolar Offset Drift							
Unipolar 0 V to +10 V Mode	-3	$\pm 1.5$	3	-2	$\pm 1$	2	ppm of FSR/°C
Bipolar Zero Drift							
Bipolar -5 V to +5 V Mode	-12	$\pm 7$	12	-10	$\pm 5$	10	ppm of FSR/°C
Bipolar -10 V to +10 V Mode	-12	$\pm 7$	12	-10	$\pm 5$	10	ppm of FSR/°C
REFERENCE INPUT							
Input Resistance	1.3		2.6	*		*	k $\Omega$
Voltage Range <sup>6</sup>	$V_{EE} + 2.0^2$		$V_{CC} - 2.0^2$	*		*	Volts
POWER REQUIREMENTS							
$V_{LL}$	4.5	5.0	5.5	*	*	*	Volts
$I_{LL}$							
@ $V_{IH}$ , $V_{IL} = 5\text{ V}$ , 0 V		0.1	1		*	*	mA
@ $V_{IH}$ , $V_{IL} = 2.4\text{ V}$ , 0.4 V		3	6		*	*	mA
$V_{CC}/V_{EE}$	$\pm 11.4$		$\pm 16.5$	*		*	Volts
$I_{CC}$		12	15		*	*	mA
$I_{EE}$		15	19		*	*	mA
Total Power		400	525		*	*	mW
ANALOG GROUND CURRENT <sup>7</sup>	-600	$\pm 400$	+600	*	*	*	$\mu\text{A}$
MATCHING PERFORMANCE							
Gain <sup>8</sup>	-6	$\pm 3$	6	-4	$\pm 2$	4	LSB
Offset <sup>9</sup>	-2	$\pm 1/2$	2	-1	$\pm 1/4$	1	LSB
Bipolar Zero <sup>10</sup>	-3	$\pm 1$	3	-2	$\pm 1$	2	LSB
Linearity <sup>11</sup>	-1.5	$\pm 1/2$	1.5	-1	$\pm 1/2$	1	LSB
CROSSTALK							
Analog			-90			*	dB
Digital			-60			*	dB
DYNAMIC PERFORMANCE ( $R_L = 2\text{ k}\Omega$ , $C_L = 500\text{ pF}$ )							
Settling Time to $\pm 1/2$ LSB							
Off $\leftarrow$ Bits $\rightarrow$ On, GAIN = 1, $V_{REF} = 10$		8	10		*	*	$\mu\text{s}$
Settling Time to $\pm 1/2$ LSB							
-10 $\leftarrow$ $V_{REF}$ $\rightarrow$ 10 V, GAIN = 1, Bits On		10			*		$\mu\text{s}$
Glitch Impulse			500			*	nV-sec
MULTIPLYING MODE PERFORMANCE							
Reference Feedthrough @ 1 kHz		-75			*		dB
Reference -3 dB Bandwidth		70			*		kHz
POWER SUPPLY GAIN SENSITIVITY							
11.4 V $\leftarrow$ $V_{CC}$ $\rightarrow$ 16.5 V		$\pm 2$	$\pm 5$		*	*	ppm/%
-16.5 V $\leftarrow$ $V_{EE}$ $\rightarrow$ -11.4 V		$\pm 2$	$\pm 5$		*	*	ppm/%
4.5 V $\leftarrow$ $V_{LL}$ $\rightarrow$ 5.5 V		$\pm 2$	$\pm 5$		*	*	ppm/%

Model	JN/JP/AD/AJ/SD			KN/KP/BD/BJ/BE/TD/TE			Units
	Min	Typ	Max	Min	Typ	Max	
<b>DIGITAL INPUTS</b>							
$V_{IH}$	<b>2.0</b>			*			Volts
$V_{IL}$	0		0.8	*		*	Volts
Data Inputs							
$I_{IH} @ V_{IN} = V_{LL}$	<b>-10</b>	$\pm 1$	<b>10</b>	*	*	*	$\mu A$
$I_{IL} @ V_{IN} = DGND$	<b>-10</b>	$\pm 1$	<b>10</b>	*	*	*	$\mu A$
$\overline{CS}/DS0/DS1/\overline{RST}/RD/\overline{LS}$							
$I_{IH} @ V_{IN} = V_{LL}$	<b>-10</b>	$\pm 1$	<b>10</b>	*	*	*	$\mu A$
$I_{IL} @ V_{IN} = V_{LL}$	<b>-10</b>	$\pm 1$	<b>10</b>	*	*	*	$\mu A$
$\overline{MS}/\overline{TR}^{12}$							
$I_{IH} @ V_{IN} = V_{LL}$	<b>-10</b>	5	<b>10</b>	*	*	*	$\mu A$
$I_{IL} @ V_{IN} = DGND$	<b>-10</b>	-5	<b>0</b>	*	*	*	$\mu A$
$\overline{QS0}/\overline{QS1}/\overline{QS2}^{12}$							
$I_{IH} @ V_{IN} = V_{LL}$	<b>-10</b>	5	<b>10</b>	*	*	*	$\mu A$
$I_{IL} @ V_{IN} = DGND$	<b>-10</b>	$\pm 1$	<b>10</b>	*	*	*	$\mu A$
<b>DIGITAL OUTPUTS</b>							
$V_{OL} @ 1.6 \text{ mA Sink}$			<b>0.4</b>			*	Volts
$V_{OH} @ 0.5 \text{ mA Source}$	<b>2.4</b>			*			Volts
<b>TEMPERATURE RANGE</b>							
JN/JP/KN/KP	<b>0</b>		<b>+70</b>	*		*	$^{\circ}C$
AD/AJ/BD/BJ/BE	<b>-40</b>		<b>+85</b>	*		*	$^{\circ}C$
SD/TD/TE	<b>-55</b>		<b>+125</b>	*		*	$^{\circ}C$

**NOTES**

<sup>1</sup>A minimum power supply of  $\pm 12.0 \text{ V}$  is required for 0 V to +10 V and  $\pm 10 \text{ V}$  operation. A minimum power supply of  $\pm 11.4 \text{ V}$  is required for -5 V to +5 V operation.

<sup>2</sup>For  $V_{CC} < +12 \text{ V}$  and  $V_{EE} > -12 \text{ V}$ . Voltage not to exceed 10 V maximum.

<sup>3</sup>Bipolar zero error is the difference from the ideal output (0 volts) and the actual output voltage with code 100 000 000 000 applied to the inputs.

<sup>4</sup>Linearity error is defined as the maximum deviation of the actual DAC output from the ideal output (a straight line drawn from 0 to F.S. - 1 LSB).

<sup>5</sup>FSR means Full-Scale Range and is 20 V for  $\pm 10 \text{ V}$  range and 10 V for  $\pm 5 \text{ V}$  range.

<sup>6</sup>A minimum power supply of  $\pm 12.0 \text{ V}$  is required for a 10 V reference voltage.

<sup>7</sup>Analog Ground Current is input code dependent.

<sup>8</sup>Gain error matching is the largest difference in gain error between any two DACs in one package.

<sup>9</sup>Offset error matching is the largest difference in offset error between any two DACs in one package.

<sup>10</sup>Bipolar zero error matching is the largest difference in bipolar zero error between any two DACs in one package.

<sup>11</sup>Linearity error matching is the difference in the worst case linearity error between any two DACs in one package.

<sup>12</sup>44-pin versions only.

\*Specifications same as JN/JP/AD/AJ/SD.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

**ABSOLUTE MAXIMUM RATINGS\***

$V_{LL}$ to DGND	0 V to +7 V
$V_{CC}$ to DGND	0 V to +18 V
$V_{EE}$ to DGND	-18 V to 0 V
Soldering	+300 $^{\circ}C$ , 10 sec
Power Dissipation	1000 mW
AGND to DGND	-1 V to +1 V
Reference Input	$V_{REF} \leq \pm 10 \text{ V}$ and $V_{REF} \leq (V_{CC} - 2 \text{ V}, V_{EE} + 2 \text{ V})$
$V_{CC}$ to $V_{EE}$	0 to +36 V

Digital Inputs	-0.3 V to +7 V
Analog Outputs	Indefinite Shorts to $V_{CC}, V_{LL}, V_{EE}$ and GND

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



# AD664

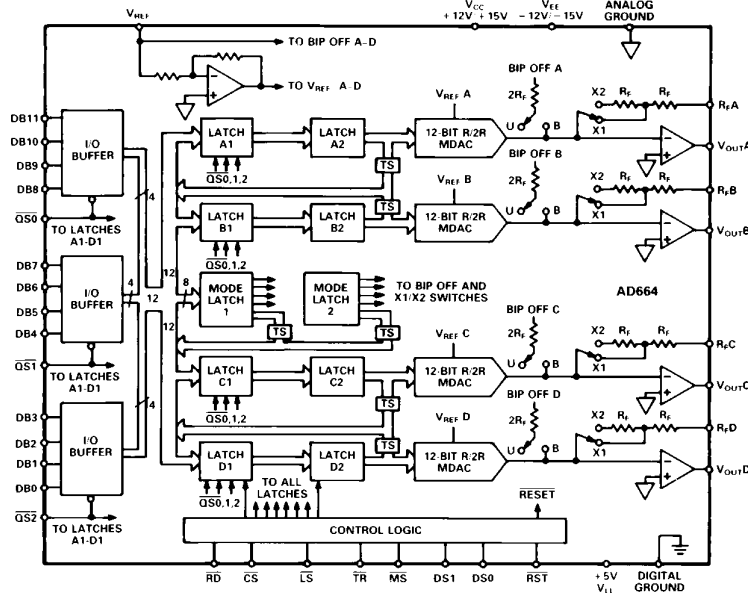


Figure 1a. 44-Pin Block Diagram

## FUNCTIONAL DESCRIPTION

The AD664 combines four complete 12-bit voltage output D/A converters with a fast, flexible digital input/output port on one monolithic chip. It is available in two forms, a 44-pin version shown in Figure 1a and a 28-pin version shown in Figure 1b.

### 44-Pin Versions

Each DAC offers flexibility, accuracy and good dynamic performance. The R-2R structure is fabricated from thin-film resistors which are laser-trimmed to achieve 1/2 LSB linearity and guaranteed monotonicity. The output amplifier combines the best features of the bipolar and MOS devices to achieve good dynamic performance and low offset. Settling time is under 10  $\mu$ s and each output can drive a 5 mA, 500 pF load. Short-circuit protection allows indefinite shorts to  $V_{LL}$ ,  $V_{CC}$ ,  $V_{EE}$  and GND. The output and span resistor pins are available separately. This feature allows a user to insert current-boosting elements to increase the drive capability of the system, as well as to overcome parasitics.

Digital circuitry is implemented in CMOS logic. The fast, low power, digital interface allows the AD664 to be interfaced with most microprocessors. Through this interface, the wide variety of features on each chip may be accessed. For example, the input data for each DAC is programmed by way of 4-, 8-, 12- or 16-bit words. The double-buffered input structure of this latch allows all four DACs to be updated simultaneously. A readback feature allows the internal registers to be read back through the same digital port, as either 4-, 8- or 12-bit words. When disabled, the readback drivers are placed in a high impedance (tristate) mode. A TRANSPARENT mode allows the input data to pass straight through both ranks of input registers and appear at the DAC with a minimum of delay. One D/A may be placed in the transparent mode at a time, or all four may be made transparent at once. The MODE SELECT feature allows the output range and mode of the DACs to be selected via the data bus inputs. An internal mode select register stores the selec-

tions. This register may also be read back to check its contents. A RESET-TO-ZERO feature allows all DACs to be reset to 0 volts out by strobing a single pin.



Figure 1b. 28-Pin Block Diagram

### 28-Pin Versions

The 28-pin versions are dedicated versions of the 44-pin AD664. Each offers a reduced set of features from those offered in the 44-pin version. This accommodates the reduced number of package pins available. Data is written and read with 12-bit words only. Output range and mode select functions are also not available in 28-pin versions. As an alternative, users specify either the UNI (unipolar, 0 to  $V_{REF}$ ) models or the BIP (bipolar,  $-V_{REF}$  to  $V_{REF}$ ) models depending on the application requirements. Finally, the transparent mode is not available on the 28-pin versions.

**Table I. Transfer Functions**

	Mode = UNI	Mode = BIP
Gain = 1	000000000000 = 0 V	000000000000 = $-V_{REF}/2$
	100000000000 = $V_{REF}/2$	100000000000 = 0 V
	111111111111 = $V_{REF} - 1$ LSB	111111111111 = $V_{REF}/2 - 1$ LSB
Gain = 2	000000000000 = 0 V	000000000000 = $V_{REF}$
	100000000000 = $V_{REF}$	100000000000 = 0 V
	111111111111 = $2 \times V_{REF} - 1$ LSB	111111111111 = $+V_{REF} - 1$ LSB

### DEFINITIONS OF SPECIFICATIONS

**LINEARITY ERROR:** Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS - 1 LSB) for any bit combination. This is also referred to as relative accuracy. The AD664 is laser-trimmed to typically maintain linearity errors at less than  $\pm 1/4$  LSB.

**MONOTONICITY:** A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD664 are monotonic over their full operating temperature range.

**DIFFERENTIAL LINEARITY:** Monotonic behavior requires that the differential linearity error be less than 1 LSB both at 25°C as well as over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code. For example, for a 10 V full-scale output, a change of 1 LSB in digital input code should result in a 2.44 mV change in the analog output ( $V_{REF} = 10$  V, Gain = 1, 1 LSB =  $10 \text{ V} \times 1/4096 = 2.44$  mV). If in actual use, however, a 1 LSB change in the input code results in a change of only 0.61 mV (1/4 LSB) in analog output, the differential nonlinearity error would be -1.83 mV, or  $-3/4$  LSB.

**GAIN ERROR:** DAC gain error is a measure of the difference between the output span of an ideal DAC and an actual device.

**UNIPOLAR OFFSET ERROR:** Unipolar offset error is the difference between the ideal output (0 V) and the actual output of a DAC when the input is loaded with all “0s” and the MODE is unipolar.

**BIPOLAR ZERO ERROR:** Bipolar zero error is the difference between the ideal output (0 V) and the actual output of a DAC when the input code is loaded with the MSB = “1” and the rest of the bits = “0” and the MODE is bipolar.

**SETTLING TIME:** Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

**CROSSTALK:** Crosstalk is the change in an output caused by a change in one or more of the other outputs. It is due to capacitive and thermal coupling between outputs.

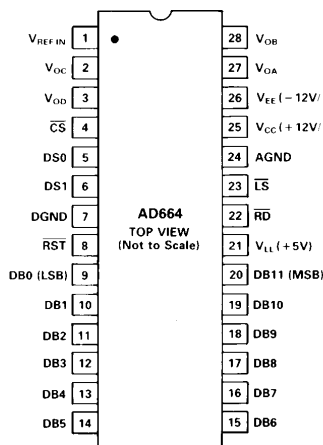
**REFERENCE FEEDTHROUGH:** The portion of an ac reference signal that appears at an output when all input bits are low. Feedthrough is due to capacitive coupling between the reference input and the output. It is specified in decibels at a particular frequency.

**REFERENCE 3 dB BANDWIDTH:** The frequency of the ac reference input signal at which the amplitude of the full-scale output response falls 3 dB from the ideal response.

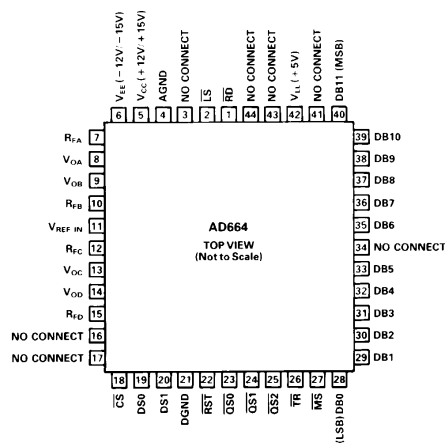
**GLITCH IMPULSE:** Glitch impulse is an undesired output voltage transient caused by asymmetrical switching times in the switches of a DAC. These transients are specified by their net area (in nV-sec) of the voltage vs. time characteristic.

### PIN CONFIGURATIONS

**28-Pin DIP Package**



**44-Pin Package**



# AD664

## ANALOG CIRCUIT CONSIDERATIONS

### Grounding Recommendations

The AD664 has two pins, designated ANALOG and DIGITAL ground. The analog ground pin is the “high quality” ground reference point for the device. A unique internal design has resulted in low analog ground current. This greatly simplifies management of ground current and the associated induced voltage drops. The analog ground pin should be connected to the analog ground point in the system. The external reference and any external loads should also be returned to analog ground.

The digital ground pin should be connected to the digital ground point in the circuit. This pin returns current from the logic portions of the AD664 circuitry to ground.

Analog and digital grounds should be connected at one point in the system. If there is a possibility that this connection be broken or otherwise disconnected, then two diodes should be connected between the analog and digital ground pins of the AD664 to limit the maximum ground voltage difference.

### Power Supplies and Decoupling

The AD664 requires three power supplies for proper operation.  $V_{LL}$  powers the logic portions of the device and requires +5 volts.  $V_{CC}$  and  $V_{EE}$  power the remaining portions of the circuitry and require +12 V to +15 V and -12 V to -15 V, respectively.  $V_{CC}$  and  $V_{EE}$  must also be a minimum of two volts greater than the maximum reference and output voltages anticipated.

Decoupling capacitors should be used on all power supply pins. Good engineering practice dictates that the bypass capacitors be located as near as possible to the package pins.  $V_{LL}$  should be bypassed to digital ground.  $V_{CC}$  and  $V_{EE}$  should be decoupled to analog ground.

### Driving the Reference Input

The reference input of the AD664 can have an impedance as low as 1.3 k $\Omega$ . Therefore, the external reference voltage must be able to source up to 7.7 mA of load current. Suitable choices include the 5 V AD586, the 10 V AD587 and the 8.192 V AD689.

The architecture of the AD664 derives an inverted version of the reference voltage for some portions of the internal circuitry. This means that the power supplies must be at least 2 V

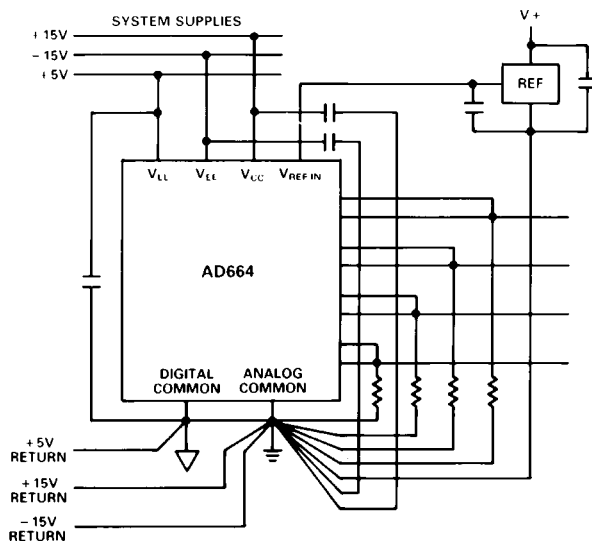


Figure 2. Recommended Circuit Schematic

greater than both the external reference and the inverted external reference.

### Output Considerations

Each DAC output can source or sink 5 mA of current to an external load. Short-circuit protection limits load current to a maximum load current of 40 mA. Load capacitance of up to 500 pF can be accommodated with no effect on stability. Should an application require additional output current, a current boosting element can be inserted into the output loop with no sacrifice in accuracy. Figure 3 details this method.

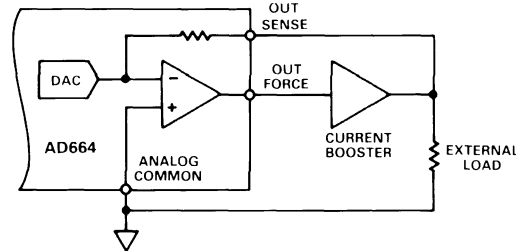


Figure 3. Current-Boosting Scheme

AD664 output voltage settling time is 10  $\mu$ s maximum. Figure 4 shows the output voltage settling time with a fixed 10 V reference, gain = 1 and all bits switched from 1 to 0.

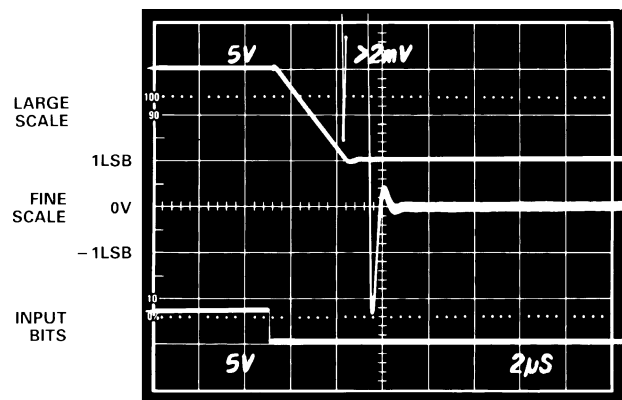


Figure 4. Settling Time; All Bits Switched from On to Off

Alternately, Figure 5 shows the settling characteristics when the reference is switched and the input bits remain fixed. In this case, all bits are “on,” the gain is 1 and the reference is switched from -5 V to +5 V.

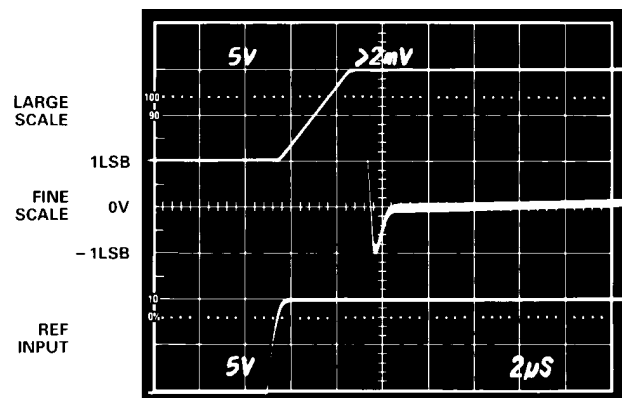


Figure 5. Settling Time; Input Bits Fixed, Reference Switched

### Multiplying Mode Performance

Figure 6 illustrates the typical open-loop gain and phase performance of the output amplifiers of the AD664.

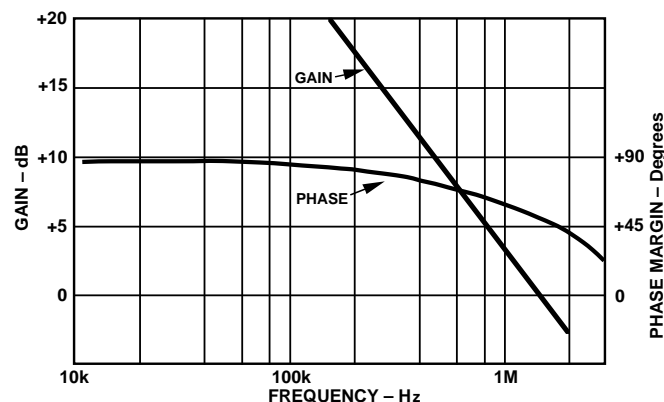


Figure 6. Gain and Phase Performance of AD664 Outputs

### Crosstalk

Crosstalk is a spurious signal on one DAC output caused by a change in the output of one or more of the other DACs. Crosstalk can be induced by capacitive, thermal or load current induced feedthrough. Figure 7 shows typical crosstalk. DAC B is set to output 0 volts. The outputs of DAC A, C and D switch 2 k $\Omega$  loads from 10 V to 0 V. The first disturbance in the output of DAC B is caused by digital feedthrough from the input data lows. The second disturbance is caused by analog feedthrough from the other DAC outputs.

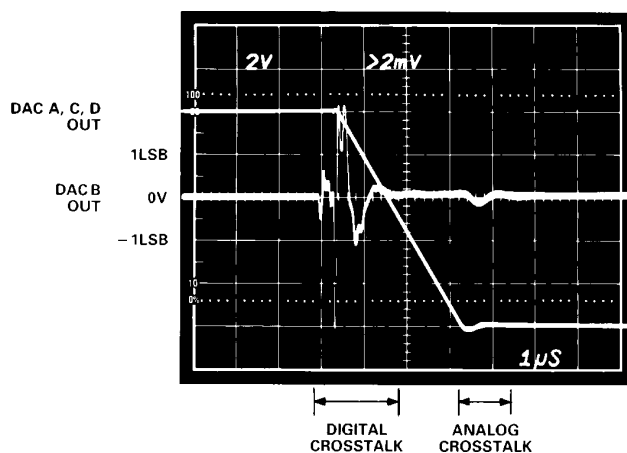


Figure 7. Output Crosstalk

### Output Noise

Wideband output noise is shown in Figure 8. This measurement was made with a 7 MHz noise bandwidth, gain = 1 and all bits on. The total rms noise is approximately one fifth the visual peak-to-peak noise.

### DIGITAL INTERFACE

As Table II shows, the AD664 makes a wide variety of operating modes available to the user. These modes are accessed or programmed through the high speed digital port of the quad DAC. On-board registers program and store the DAC input codes and

the DAC operating mode data. All registers are double-buffered to allow for simultaneous updating of all outputs. Register data may be read back to verify the respective contents. The digital port also allows transparent operation. Data from the input pins can be sent directly through both ranks of latches to the DAC.

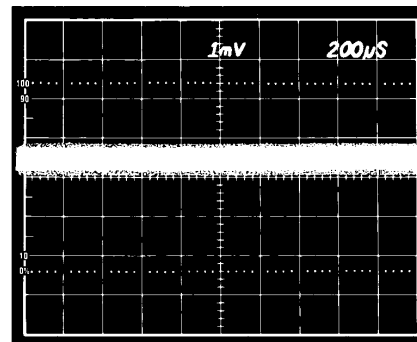


Figure 8. Typical Output Noise

Partial address decoding is performed by the DS0, DS1,  $\overline{QS0}$ ,  $\overline{QS1}$  and  $\overline{QS2}$  address bits.  $\overline{QS0}$ ,  $\overline{QS1}$  and  $\overline{QS2}$  allow the 44-pin versions of the AD664 to be addressed in 4-bit nibble, 8-bit byte or 12-bit parallel words.

The  $\overline{RST}$  pin provides a simple method to reset all output voltages to zero. Its advantages are speed and low software overhead.

### INPUT DATA

In general, two types of data will be input to the registers of the AD664, input code data and mode select data. Input code data sets the DAC inputs while the mode select data sets the gain and range of each DAC.

The versatile I/O port of the AD664 allows many different types of data input schemes. For example, the input code for just one of the DACs may be loaded and the output may or may not be updated. Or, the input codes for all four DACs may be written, and the outputs may or may not be updated.

The same applies for MODE SELECTION. The mode of just one or many of the DACs may be rewritten and the user can choose to immediately update the outputs or wait until a later time to transfer the mode information to the outputs.

A user may also write both input code and mode information into their respective first ranks and then update all second ranks at once.

Finally, transparent operation allows data to be transferred from the inputs to the outputs using a single control line. This feature is useful, for example, in a situation where one of the DACs is used in an A/D converter. The SAR register could be connected directly to a DAC by using the transparent mode of operation. Another use for this feature would be during system calibration where the endpoints of the transfer function of each DAC would be measured. For example, if the full-scale voltages of each DAC were to be measured, then by making all four DACs transparent and putting all "1s" on the input port, all four DACs would be at full-scale. This requires far less software overhead than loading each register individually.

**Table II. AD664 Digital Truth Table**

Function	DS1, DS0	$\overline{LS}$	$\overline{MS}$	$\overline{TR}$	$\overline{QS0}, \overline{1}, \overline{2}^1$	$\overline{RD}$	$\overline{CS}$	$\overline{RST}$
Load 1st Rank (data)								
DACA	00	0	1	1	Select Quad	1	1→0	1
DACB	01	0	1	1	Select Quad	1	1→0	1
DACC	10	0	1	1	Select Quad	1	1→0	1
DACD	11	0	1	1	Select Quad	1	1→0	1
Load 2nd Rank (data)	XX	1	1	1	XXX	1	1→0	1
Readback 2nd Rank (data)	Select D/A	X	1	1	Select Quad	0	1→0	1
Reset	XX	X	X	X	XXX	X	X	0
Transparent <sup>1</sup>								
All DACs	XX	1	1	0	000	1	1→0	1
DACA	00	0	1	0	000	1	1→0	1
DACB	01	0	1	0	000	1	1→0	1
DACC	10	0	1	0	000	1	1→0	1
DACD	11	0	1	0	000	1	1→0	1
Mode Select <sup>1,2</sup>								
1st Rank	XX	0	0	1	00X	1	1→0	1
2nd Rank	XX	1	0	1	XXX	1	1→0	1
Readback Mode <sup>1</sup>	XX	X	0	1	00X	0	1→0	1
Update 2nd Rank and Mode	XX	1	0	0	XXX	1	1→0	1

**NOTES**

X = Don't Care.

<sup>1</sup>For 44-pin versions only. Allow the AD664 to be addressed in 4-bit nibble, 8-bit byte or 12-bit parallel words.

<sup>2</sup>For  $\overline{MS}$ ,  $\overline{TR}$ ,  $\overline{LS} = 0$ , a  $\overline{MS}$  1st write occurs.

The following sections detail the timing requirements for various data loading schemes. All of the timing specifications shown assume  $V_{IH} = 2.4\text{ V}$ ,  $V_{IL} = 0.4\text{ V}$ ,  $V_{CC} = +15\text{ V}$ ,  $V_{EE} = -15\text{ V}$  and  $V_{LL} = +5\text{ V}$ .

**Load and Update One DAC Output**

In this first example, the object is simply to change the output of one of the four DACs on the AD664 chip. The procedure is to select the address bits that indicate the DAC to be programmed, pull LATCH SELECT ( $\overline{LS}$ ) low, pull CHIP SELECT ( $\overline{CS}$ ) low, release  $\overline{LS}$  and then release  $\overline{CS}$ . When  $\overline{CS}$  goes low, data enters the first rank of the input latch. As soon as  $\overline{LS}$  goes high, the data is transferred into the second rank and produces the new output voltage. During this transfer,  $\overline{MS}$ ,  $\overline{TR}$ ,  $\overline{RD}$  and  $\overline{RST}$  should be held high.

**Preloading the First Rank of One DAC**

In this case, the object is to load new data into the first rank of one of the DACs but *not* the output. As in the previous case, the address and data inputs are placed on the appropriate pins.  $\overline{LS}$  is then brought to "0" and then  $\overline{CS}$  is asserted. Note that in this situation, however,  $\overline{CS}$  goes high before  $\overline{LS}$  goes high. The input data is prevented from getting to the second rank and affecting the output voltage.

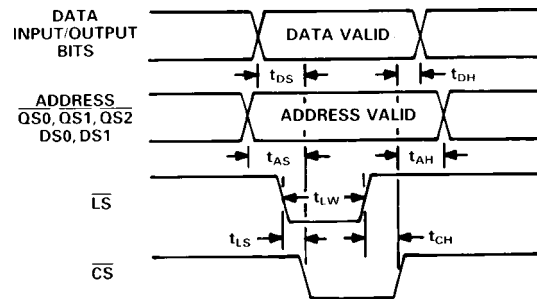


Figure 9a. Update Output of a Single DAC

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
t <sub>LS</sub> *	0	0
t <sub>DS</sub>	0	0
t <sub>DH</sub>	0	0
t <sub>LW</sub>	60	80
t <sub>CH</sub>	30	50
t <sub>AS</sub>	0	0
t <sub>AH</sub>	0	0

\*FOR t<sub>LS</sub> > 0, THE WIDTH OF  $\overline{LS}$  MUST BE INCREASED BY THE SAME AMOUNT THAT t<sub>LS</sub> IS GREATER THAN 0 ns.

Figure 9b. Update Output of a Single DAC Timing



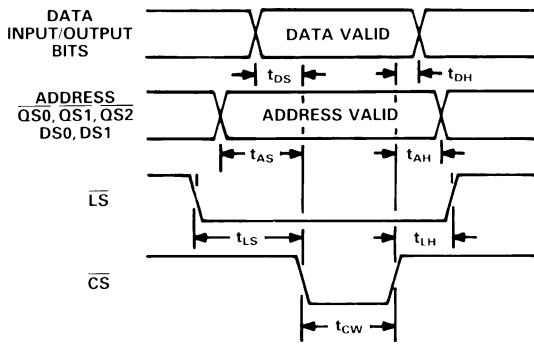


Figure 10a. Preload First Rank of a DAC

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
t <sub>LS</sub>	0	0
t <sub>LH</sub>	15	15
t <sub>cw</sub>	80	100
t <sub>DS</sub>	0	0
t <sub>DH</sub>	15	15
t <sub>AS</sub>	0	0
t <sub>AH</sub>	15	15

Figure 10b. Preload First Rank of a DAC Timing

This allows the user to “preload” the data to a DAC and strobe it into the output latch at some future time. The user could do this by reproducing the sequence of signals illustrated in the next section.

**Update Second Rank of a DAC**

Assuming that a new input code had previously been placed into the first rank of the input latches, the user can update the output of the DAC by simply pulling CS low while keeping LS, MS, TR, RD and RST high. Address data is not needed in this case. In reality, all second ranks are being updated by this procedure, but only those which receive data different from that already there would manifest a change. Updating the second rank does not change the contents of the first rank.

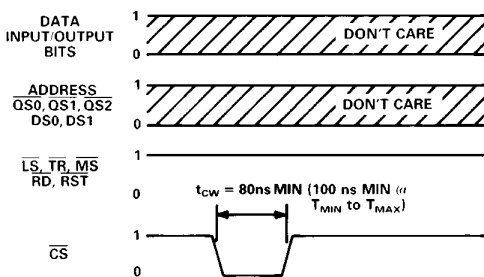


Figure 11. Update Second Rank of a DAC

The same options that exist for individual DAC input loading also exist for multiple DAC input loading. That is, the user can choose to update the first and second ranks of the registers or preload the first ranks and then update them at a future time.

**Preload Multiple First Rank Registers**

The first ranks of the DAC input registers may be preloaded with new input data without disturbing the second rank data. This is done by transferring the data into the first rank by bringing CS low while LS is low. But CS must return high before LS. This prevents the data from the first rank from getting into the second rank. A simple second rank update cycle as shown in Figure 11 would move the “preloaded” information to the DACs.

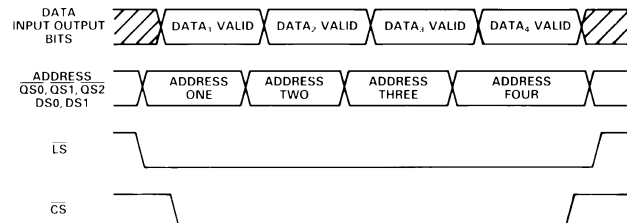


Figure 12. Preload First Rank Registers

**Load and Update Multiple DAC Outputs**

The following examples demonstrate two ways to update all DAC outputs. The first method involves doing all data transfers during one long CS low period. Note that in this case, shown in Figure 13, LS returns high before CS goes high. Data hold time, relative to an address change, is 70 ns. This updates the outputs of all DACs simultaneously.

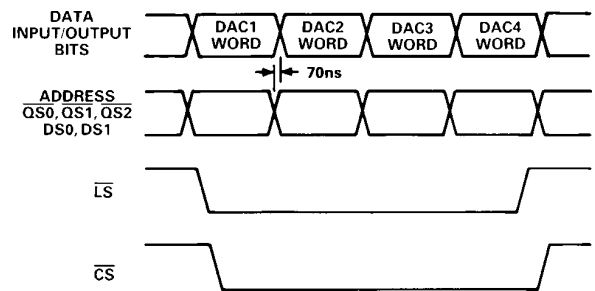


Figure 13. Update All DAC Outputs

The second method involves doing a CS assertion (low) and an LS toggle separately for each DAC. It is basically a series of preload operations (Figure 10). In this case, illustrated in Figure 14, two LS signals are shown. One, labeled LS, goes high before CS returns high. This transfers the “new” input word to the DAC outputs sequentially. The second LS signal, labeled Alternate LS, stays low until CS returns high. Using this sequence loads the first ranks with each “new” input word but doesn’t update the DAC outputs. To then update all DAC outputs simultaneously would require the signals illustrated in Figure 11.

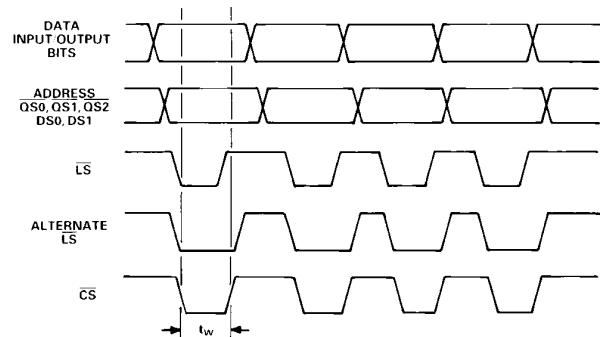


Figure 14. Load and Update Multiple DACs

**SELECTING GAIN RANGE AND MODES (44-PIN VERSIONS)**

The AD664’s mode select feature allows a user to configure the gain ranges and output modes of each of the four DACs. On-board switches take the place of up to eight external relays that would normally be required to accomplish this task. The switches are programmed by the mode select word entered via the data I/O port. The mode select word is eight-bits wide and

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occupies the topmost eight bits of the input word. The last four bits of the input word are “don’t cares.”

Figure 15 shows the format of the MODE SELECT word. The first four bits determine the gain range of the DAC. When set to be a gain of 1, the output of the DAC spans a voltage of 1 times the reference. When set to a gain of 2, the output of the DAC spans a voltage of 2 times the reference.

The next four bits determine the mode of the DAC. When set to UNIPOLAR, the output goes from 0 to REF or 0 to 2 REF. When the BIPOLAR mode is selected, the output goes from -REF/2 to REF/2 or -REF to REF.

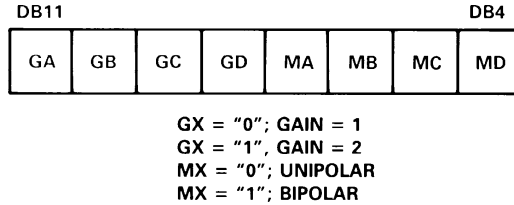


Figure 15. Mode Select Word Format

## Load and Update Mode of One DAC

In this next example, the object is to load new mode information for one of the DACs into the first rank of latches and then immediately update the second rank. This is done by putting the new mode information (8-bit word length) onto the databus. Then  $\overline{MS}$  and  $\overline{LS}$  are pulled low. Following that,  $\overline{CS}$  is pulled low. This loads the mode information into the first rank of latches.  $\overline{LS}$  is then brought high. This action updates the second rank of latches (and, therefore, the DAC outputs). The load cycle ends when  $\overline{CS}$  is brought high.

In reality, this load cycle really updates the modes of all the DACs, but the effect is to only change the modes of those DACs whose mode select information has actually changed.

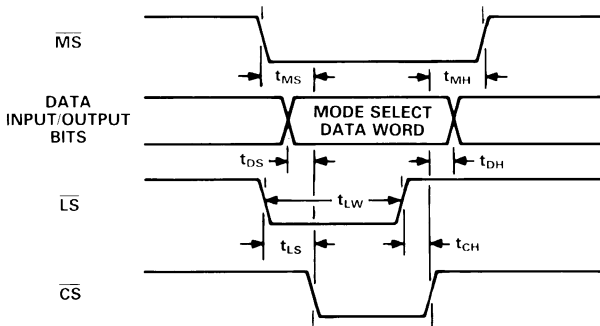


Figure 16a. Load and Update Mode of One DAC

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
t <sub>MS</sub>	0	0
t <sub>LS*</sub>	0	0
t <sub>DS</sub>	0	0
t <sub>LW</sub>	60	70
t <sub>CH</sub>	70	80
t <sub>DH</sub>	0	0
t <sub>MH</sub>	0	0

\*FOR t<sub>LS</sub> > 0, THE WIDTH OF  $\overline{LS}$  MUST BE INCREASED BY THE SAME AMOUNT THAT t<sub>LS</sub> IS GREATER THAN 0 ns.

Figure 16b. Load and Update Mode of One DAC Timing

## Preloading the Mode Select Register

Mode data can be written into the first rank of the mode select latch without changing the modes currently being used. This feature is useful when a user wants to preload new mode information in anticipation of strobing that in at a future time. Figure 17 illustrates the correct sequence and timing of control signals to accomplish this task.

This allows the user to “preload” the data to a DAC and strobe it into the output latch at some future time. The user could do this by reproducing the sequence of signals illustrated in Figures 17c and 17d.

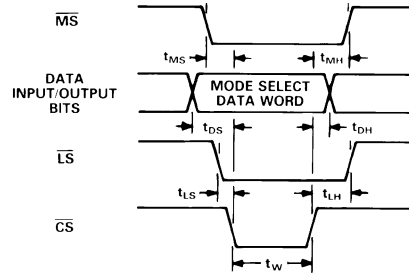


Figure 17a. Preload Mode Select Register

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
t <sub>MH</sub>	15	15
t <sub>MS</sub>	0	0
t <sub>LS</sub>	0	0
t <sub>DS</sub>	0	0
t <sub>W</sub>	80	100
t <sub>LH</sub>	15	15
t <sub>DH</sub>	15	15

Figure 17b. Preload Mode Select Register Timing

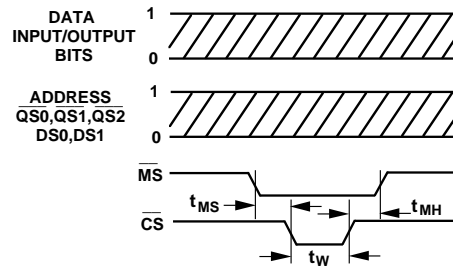


Figure 17c. Update Second Rank of Mode Select Latch

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
t <sub>MS</sub>	0	0
t <sub>MH</sub>	0	0
t <sub>W</sub>	80	100

Figure 17d. Update Second Rank of Mode Select Latch Timing

## Transparent Operation (44-Pin Versions)

Transparent operation allows data from the inputs of the AD664 to be transferred into the DAC registers without the intervening step of being latched into the first rank of latches. Two modes of transparent operation exist, the “partially transparent” mode and a “fully transparent” mode. In the “partially transparent” mode, one of the DACs is transparent while the remaining three continue to use the data latched into their respective input registers. Both modes require a 12-bit wide input word!

Fully transparent operation can be thought of as a simultaneous load of data from Figure 9a where replacing  $\overline{LS}$  with  $\overline{TR}$  causes all 4 DACs to be loaded at once.

The Fully transparent mode is achieved by asserting lows on  $\overline{QS0}$ ,  $\overline{QS1}$ ,  $\overline{QS2}$ ,  $\overline{TR}$  and  $\overline{CS}$  while keeping  $\overline{LS}$  high in addition to  $\overline{MS}$  and  $\overline{RB}$ . Figure 18a illustrates the necessary timing relationships. Fully transparent operation will also work with  $\overline{TR}$  tied low (enabled).

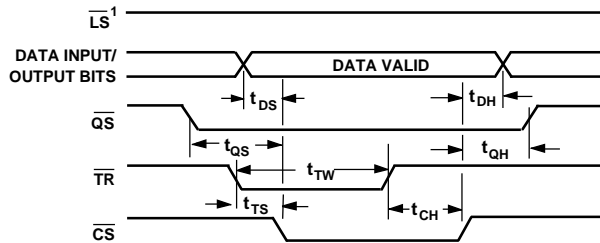


Figure 18a. Fully Transparent Mode

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
t <sub>AS</sub>	0	0
t <sub>OS</sub>	0	0
t <sub>TS</sub> *	0	0
t <sub>TW</sub>	80	90
t <sub>CH</sub>	90	110
t <sub>DH</sub>	0	0
t <sub>QH</sub>	0	0

\*FOR t<sub>TS</sub> > 0, THE WIDTH OF  $\overline{TR}$  MUST BE INCREASED BY THE SAME AMOUNT THAT t<sub>TS</sub> IS GREATER THAN 0 ns.

Figure 18b. Fully Transparent Mode Timing

Partially transparent operation can be thought of as preloading the first rank in Figure 10a without requiring the additional  $\overline{CS}$  pulse from Figure 11.

The partially transparent mode is achieved by setting  $\overline{CS}$ ,  $\overline{QS0}$ ,  $\overline{QS1}$ ,  $\overline{QS2}$ ,  $\overline{LS}$ , and  $\overline{TR}$  low while keeping  $\overline{RD}$  and  $\overline{MS}$  high. The address of the transparent DAC is asserted on  $\overline{DS0}$  and  $\overline{DS1}$ . Figure 19a illustrates the necessary timing relationships. Partially transparent operation will also work with  $\overline{TR}$  tied low (enabled).

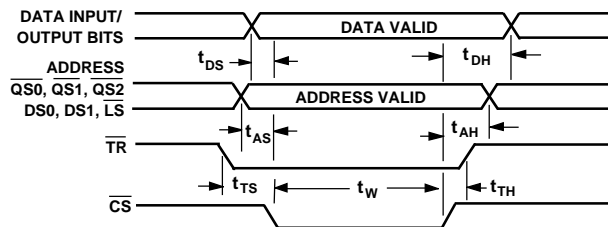


Figure 19a. Partially Transparent

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
t <sub>DS</sub>	0	0
t <sub>AS</sub>	0	0
t <sub>TS</sub>	0	0
t <sub>TW</sub>	90	110
t <sub>DH</sub>	15	15
t <sub>AH</sub>	15	15
t <sub>TH</sub>	15	15

Figure 19b. Partially Transparent Mode Timing

**OUTPUT DATA**

Two types of outputs may be obtained from the internal data registers of the AD664 chip, mode select and DAC input code data. Readback data may be in the same forms in which it can be entered; 4-, 8-, and 12-bit wide words (12 bits only for 28-pin versions).

**DAC Data Readback**

DAC input code readback data is obtained by setting the address of the DAC ( $\overline{DS0}$ ,  $\overline{DS1}$ ) and Quads ( $\overline{QS0}$ ,  $\overline{QS1}$ ,  $\overline{QS2}$ ) on the address pins and bringing the  $\overline{RD}$  and  $\overline{CS}$  pins low. The timing diagram for a DAC code readback operation appears in Figure 20.



Figure 20a. DAC Input Code Readback

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
t <sub>AS</sub>	0	0
t <sub>RS</sub>	0	0
t <sub>DV</sub>	150	180
t <sub>DF</sub>	60	75
t <sub>AH</sub>	0	0
t <sub>RH</sub>	0	0

Figure 20b. DAC Input Code Readback Timing

**Mode Data Readback**

Mode data is read back in a similar fashion. By setting  $\overline{MS}$ ,  $\overline{QS0}$ ,  $\overline{QS1}$ ,  $\overline{RD}$  and  $\overline{CS}$  low while setting  $\overline{TR}$  and  $\overline{RST}$  high, the mode select word is presented to the I/O port pins. Figure 21 shows the timing diagram for a readback of the mode select data register.

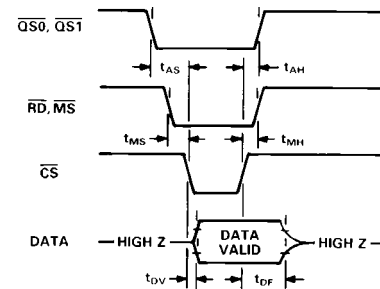


Figure 21a. Mode Data Readback

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
t <sub>AS</sub>	0	0
t <sub>MS</sub>	0	0
t <sub>DV</sub>	150	180
t <sub>DF</sub>	60	75
t <sub>AH</sub>	0	0
t <sub>MH</sub>	0	0

Figure 21b. DAC Mode Readback Timing

# AD664

## Output Loads

Readback timing is tested with the output loads shown in Figure 22.

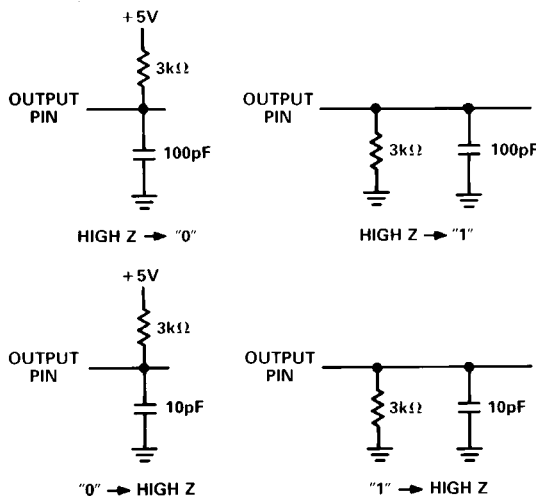


Figure 22. Output Loads

## Asynchronous Reset Operation

The asynchronous reset signal shown in Figure 23 may be asserted at any time. A minimum pulse width ( $t_{RW}$ ) of 90 ns is required. The reset feature is designed to return all DAC outputs to 0 volts regardless of the mode or range selected. In the 44-pin versions, the modes are reset to unipolar 10 V span (gain of 1), and the input codes are rewritten to be “0s.” Previous DAC code and mode information is erased.

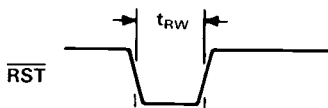


Figure 23a. Asynchronous Reset Operation

SYMBOL	25°C MIN (ns)	T <sub>MIN</sub> to T <sub>MAX</sub> MIN (ns)
$t_{RW}$	80	100

Figure 23b. Asynchronous Reset Operation Timing

In the 28-pin versions of the AD664, the mode remains unchanged, the appropriate input code is rewritten to reset the output voltage to 0 volts. As in the 44-pin versions, the previous input data is erased.

At power-up, an AD664 may be activated in either the read or write modes. While at the device level this will not produce any problems, at the system level it may. Analog Devices recommends the addition of a simple power-on reset scheme to any system where the possibility of an unknown start-up state could be a problem. The simplest version of this scheme is illustrated in Figure 24.

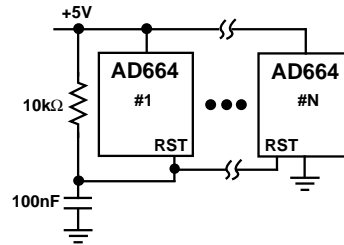


Figure 24. Power-On Reset

It is obvious from inspection that the scheme shown in Figure 24 is only appropriate for systems in which the  $\overline{RST}$  is otherwise not used. Should the user wish to use the  $\overline{RST}$  pin, an additional logic gate may be included to combine the power-on reset with the reset signal.

## INTERFACING THE AD664 TO MICROPROCESSORS

The AD664 is easy to interface with a wide variety of popular microprocessors. Common architectures include processors with dedicated 8-bit data and address buses, an 8-bit bus over which data and address are multiplexed, an 8-bit data and 16-bit address partially muxed, and separate 16-bit data and address buses.

AD664 addressing can be accomplished through either memory-mapped or I/O techniques. In memory-mapped schemes, the AD664 appears to the host microprocessor as RAM memory. Standard memory addressing techniques are used to select the AD664. In the I/O schemes, the AD664 is treated as an external I/O device by the host. Dedicated I/O pins are used to address the AD664.

## MC6801 Interface

In Figures 25a–25d, we illustrate a few of the various methods that can be used to connect an AD664 to the popular MC6801 microprocessor. In each of these cases, the MC6801 is intended to be configured in its expanded, nonmultiplexed mode of operation. In this mode, the MC6801 can address 256 bytes of external memory over 8-bit data (Port 3) and 8-bit address (Port 4) buses. Eight general-purpose I/O lines (Port 1) are also available. On-board RAM and ROM provide program and data storage space.

In Figure 25a, the three least significant address bits (P40, P41 and P42) are employed to select the appropriate on-chip addresses for the various input registers of the AD664. Three I/O lines (P17, P16 and P15) are used to select various operating features of the the AD664. IOS and E(nable) are combined to produce an appropriate  $\overline{CS}$  signal. This addressing scheme leaves the five most significant address bits and five I/O lines free for other tasks in the system.

Figure 25b shows another way to interface an AD664 to the MC6801. Here we’ve used the six least significant address lines to select AD664 features and registers. This is a purely memory-mapped scheme while the one illustrated in Figure 25a uses some memory-mapping as well as some dedicated I/O pins. In Figure 25b, two address lines and all eight I/O lines remain free for other system tasks.

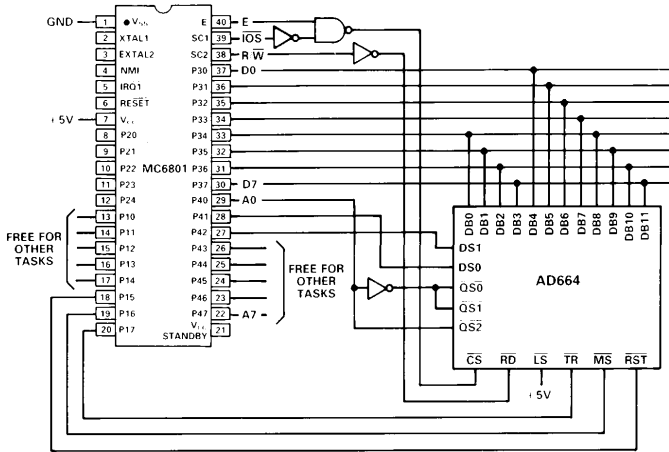


Figure 25a. Simple AD664 to MC6801 Interface

Expansion of the scheme employed in Figure 25a results in that shown in Figure 25c. Here, two AD664s are connected to an MC6801, providing a total of eight 12-bit, software programmable DACs. Again, the three least significant bits of address are used to select the on-chip registers of the AD664. IOS and E, as well as a fourth address bit, are decoded to provide the appropriate CS signals. Four address and five I/O lines remain uncommitted.

A slightly more sophisticated approach to system expansion is illustrated in Figure 25d. Here, a 74LS138 (1-of-8 decoder) is used to address one of the eight AD664s connected to the MC6801. The three least significant address bits are used to select on-chip register and DAC. The next three address bits are used to select the appropriate AD664. IOS and E gate the 74LS138 output.

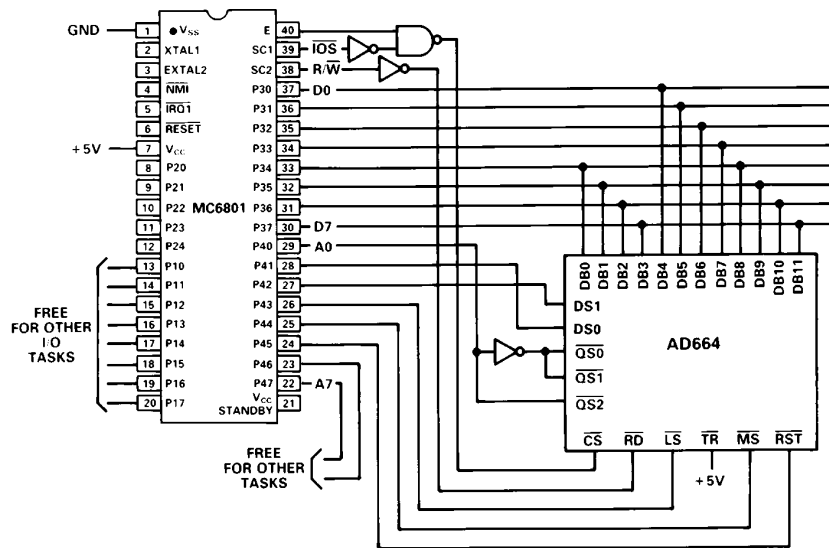


Figure 25b. Alternate AD664 to MC6801 Interface

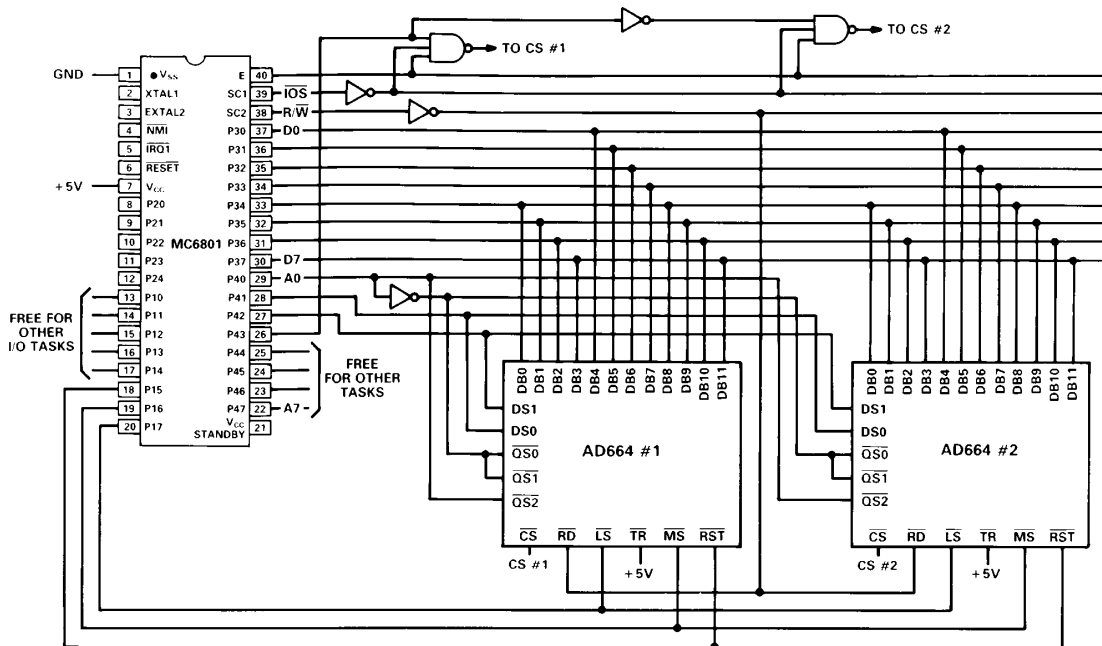


Figure 25c. Interfacing Two AD664s to an MC6801

# AD664

The schemes in Figure 25 illustrate some of the trade-offs which a designer may make when configuring a system. For example, the designer may use I/O lines instead of address bits or vice versa. This decision may be influenced by other I/O tasks or system expansion requirements. He/she can also choose to implement only a subset of the features available. Perhaps the  $\overline{RST}$  pin isn't really needed. Tying that input pin to  $V_{LOGIC}$  frees up another I/O or address bit. The same consideration applies to mode select. In all of these cases  $\overline{TR}$  is shown tied to  $V_{LOGIC}$ , because the MC6801 cannot provide the 12-bit-wide input word required for the transparent mode. In situations where transparent operation isn't required, and mode select is also not needed, the designer may consider specifying the DIP version of the device (either the UNI or BIP version).

Each of the schemes illustrated in Figure 25 operates with an MC6801 at clock rates up to and including 1.5 MHz. Similar schemes can be derived for other 8-bit microprocessors and microcontrollers such as the 8051/8086/8088/6502, etc. One such scheme developed for the 8051/AD664 is illustrated in Figure 26.

### 8051 Interface

Figure 26 shows the AD664 combined with an 8051  $\mu$ controller chip. Three LSBs of address provide the quad and DAC select signals. Control signals from Port 1 select various operating modes such as readback, mode select and reset as well as providing the  $\overline{LS}$  signal. Read and write signals from the 8051 are decoded to provide the  $\overline{CS}$  signal.

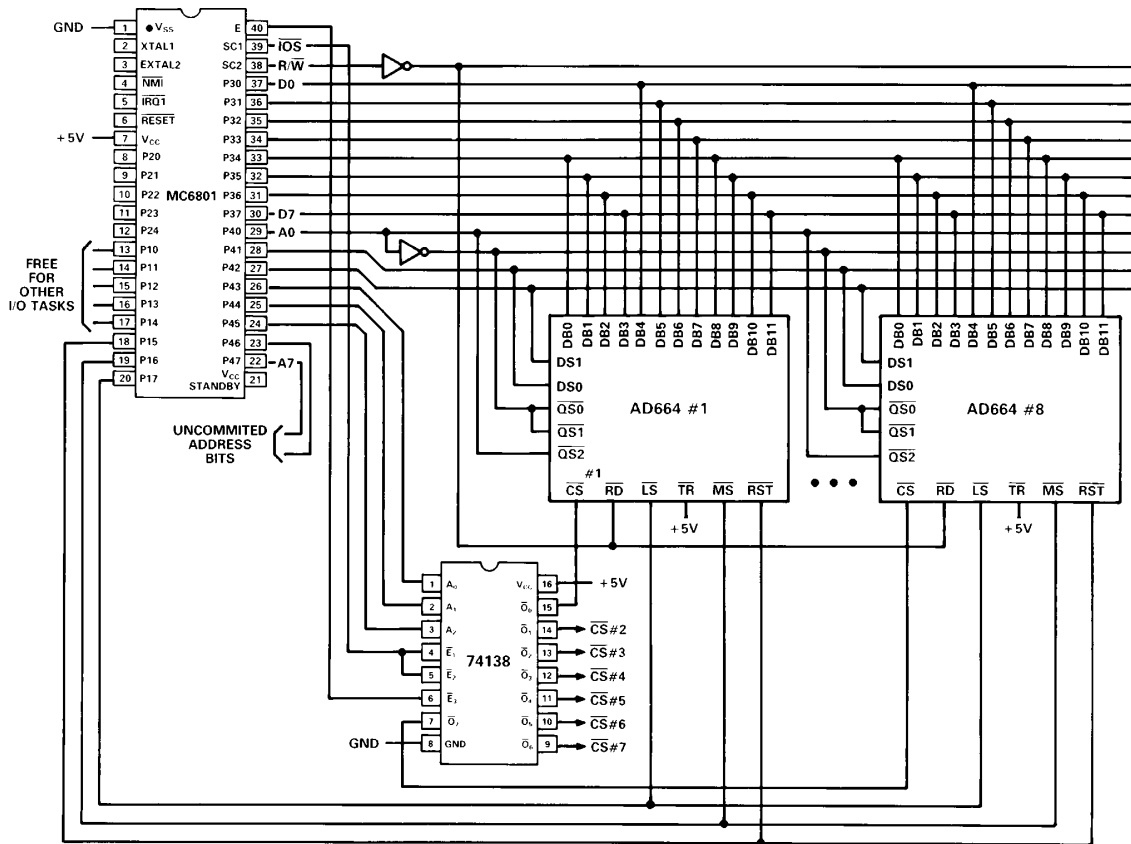


Figure 25d. Interfacing Eight AD664s to an MC6801

## IBM PC\* Interface

Figure 27 illustrates a simple interface between an IBM PC and an AD664. The three least significant address bits are used to select the Quad and DAC. The next two address bits are used for  $\overline{LS}$  and  $\overline{MS}$ . In this scheme, a 12-bit input word requires two load cycles, an 8-bit word and a 4-bit word.

is required to transfer the word or words previously written to the second rank. A 12-bit-wide word again requires at least two read cycles; one for the 8 MSBs and four for the LSBs. The page select signal produces a  $\overline{CS}$  strobe for any address from 300H to 31FH.

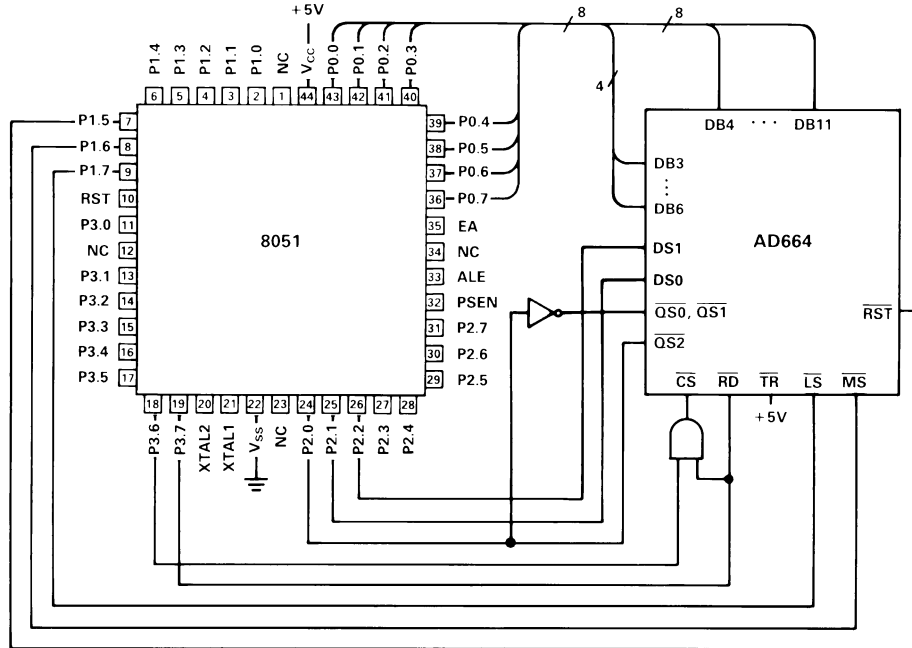


Figure 26. AD664 to 8051 Interface

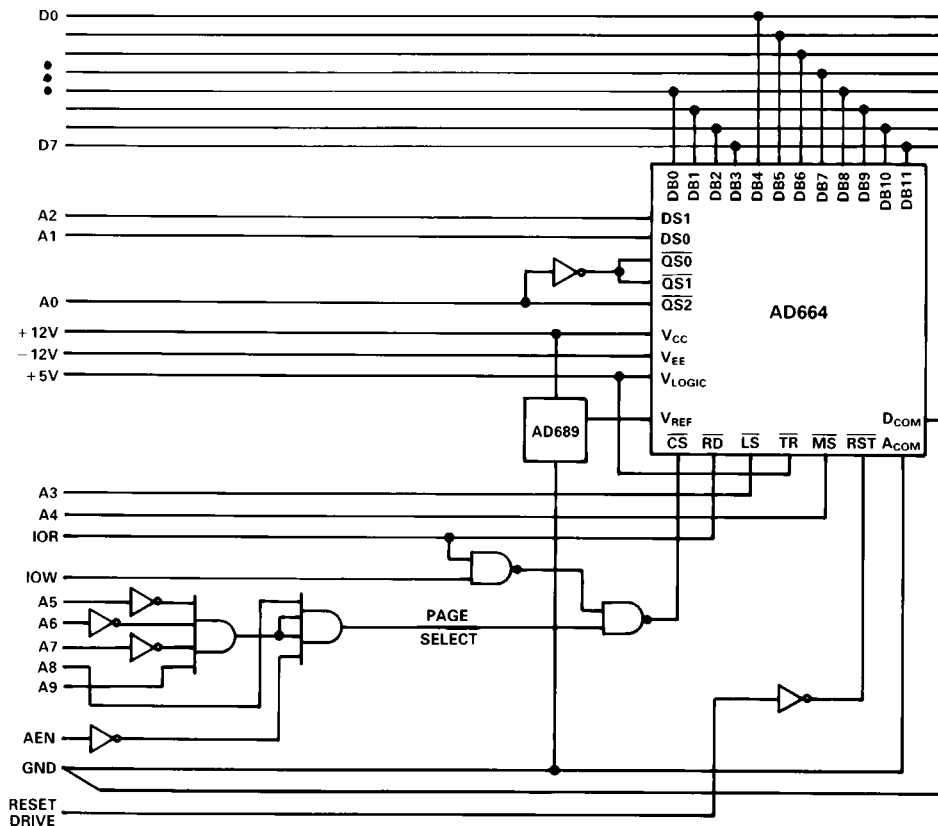


Figure 27. AD664 to IBM PC Interface

\*IBM PC is a trademark of International Business Machines Corp.

# AD664

Table III details the memory locations and addresses used by this interface.

**Table III. IBM PC Memory Map**

HEX	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	REGISTER SELECTED
300	1	1	0	0	0	0	0	0	0	0	Illegal Address
301	↓	↓	↓	↓	↓	↓	↓	0	0	1	Mode Select, 1st Rank
302	↓	↓	↓	↓	↓	↓	↓	0	1	0	Illegal Address
303	↓	↓	↓	↓	↓	↓	↓	0	1	1	Mode Select, 1st Rank
304	↓	↓	↓	↓	↓	↓	↓	1	0	0	Illegal Address
305	↓	↓	↓	↓	↓	↓	↓	1	0	1	Mode Select, 1st Rank
306	↓	↓	↓	↓	↓	↓	↓	1	1	0	Illegal Address
307	↓	↓	↓	↓	↓	↓	▼	1	1	1	Mode Select, 1st Rank
308	↓	↓	↓	↓	↓	↓	1	0	0	0	Mode Select, 2nd Rank
309	↓	↓	↓	↓	↓	↓	↓	0	0	1	
30A	↓	↓	↓	↓	↓	↓	↓	0	1	0	
30B	↓	↓	↓	↓	↓	↓	↓	0	1	1	
30C	↓	↓	↓	↓	↓	↓	↓	1	0	0	
30D	↓	↓	↓	↓	↓	↓	↓	1	0	1	
30E	↓	↓	↓	↓	↓	↓	↓	1	1	0	
30F	↓	↓	↓	↓	↓	▼	▼	1	1	1	▼
310	↓	↓	↓	↓	↓	1	0	0	0	0	DAC A, 4 LSBs, 1st Rank
311	↓	↓	↓	↓	↓	↓	↓	0	0	1	DAC A, 8 MSBs, 1st Rank
312	↓	↓	↓	↓	↓	↓	↓	0	1	0	DAC B, 4 LSBs, 1st Rank
313	↓	↓	↓	↓	↓	↓	↓	0	1	1	DAC B, 8 MSBs, 1st Rank
314	↓	↓	↓	↓	↓	↓	↓	1	0	0	DAC C, 4 LSBs, 1st Rank
315	↓	↓	↓	↓	↓	↓	↓	1	0	1	DAC C, 8 MSBs, 1st Rank
316	↓	↓	↓	↓	↓	↓	↓	1	1	0	DAC D, 4 LSBs, 1st Rank
317	↓	↓	↓	↓	↓	↓	▼	1	1	1	DAC D, 8 MSBs, 1st Rank
318	↓	↓	↓	↓	↓	↓	1	0	0	0	2nd Rank
319	↓	↓	↓	↓	↓	↓	↓	0	0	1	↓
31A	↓	↓	↓	↓	↓	↓	↓	0	1	0	
31B	↓	↓	↓	↓	↓	↓	↓	0	1	1	
31C	↓	↓	↓	↓	↓	↓	↓	1	0	0	
31D	↓	↓	↓	↓	↓	↓	↓	1	0	1	
31E	↓	↓	↓	↓	↓	↓	↓	1	1	0	
31F	▼	▼	▼	▼	▼	▼	▼	1	1	1	▼

Note: Shaded registers are readable.



The following IBM PC Basic routine produces four output voltage ramps from one AD664. Line numbers 10 through 70 define the hardware addresses for the first and second ranks of DAC registers as well as the first and second ranks of the mode select register. Program variables are initialized in line numbers 110 through 130. Line number 170 writes "0s" out to the first rank and, then, the second rank of the mode select register.

Line numbers 200 through 320 calculate output voltages. Finally line numbers 410 through 450 update the first, then the second ranks of the DAC input registers. Hardware registers may be read with the "INP" instruction. For example, the contents of the DAC A register may be accessed with the following command: Line# A = INP(DACA).

```

5          REM----AD664 LISSAJOUS PATTERNS----
10         REM ---ASSIGN HARDWARE ADDRESSES---
20         DACA = 785
30         DACB = 787
40         DACC = 789
50         DACD = 791
60         DAC2ND = 792
70         MODE1 = 769: MODE2 = 776
80         REM
90         REM
100        REM ---INITIALIZE VARIABLES---
110        X = 0: Y1 = 128: Y2 = 64: Y3 = 32
120        CX = 1: CY1 = 1: CY2 = -1: CY3 = 1
130        FX = 9: FY1 = 5: FY2 = 13: FY3 = 15
140        REM
150        REM
160        REM ---INITIALIZE MODES AND GAINS---
170        OUT MODE1,0: OUT MODE2,0
180        REM
190        REM
200        REM ---CALCULATE VARIABLES---
210        X = X + FX*CX
220        Y1 = Y1 + FY1*CY1
230        Y2 = Y2 + FY2*CY2
240        Y3 = Y3 + FY3*CY3
250        IF X > 255 THEN X = 255: CX = -1: GOTO 270
260        IF X < 0 THEN X = 0: CX = 1
270        IF Y1 > 255 THEN Y1 = 255: CY1 = -1: GOTO 290
280        IF Y1 < 0 THEN Y1 = 0: CY1 = 1
290        IF Y2 > 255 THEN Y2 = 255: CY2 = -1 GOTO 310
300        IF Y2 < 0 THEN Y2 = 0: CY2 = -1
310        IF Y3 > 255 THEN Y3 = 255: CY3 = -1: GOTO 400
320        IF Y3 < 0 THEN Y3 = 0: CY3 = 1
330        REM
340        REM
400        REM ---SEND DAC DATA---
410        OUT DACA,X
420        OUT DACB,Y1
430        OUT DACC,Y2
440        OUT DACD,Y3
450        OUT DAC2ND,0
500        REM
510        REM
520        REM ---LOOP BACK---
530        GOTO 210

```





Figure 29. AD664 in "Tester-per-Pin" Architecture

**APPLICATIONS OF THE AD664**  
**"Tester-Per-Pin" ATE Architecture**

Figure 29 shows the AD664 used in a single channel of a digital test system. In this scheme, the AD664 supplies four individual output voltages. Two are provided to the  $V_{HIGH}$  and  $V_{LOW}$  inputs of the AD345 pin driver I.C. to set the digital output levels. Two others are routed to the inputs of the AD96687 dual comparator to supply reference levels of the readback features. This approach can be replicated to give as many channels of stimulus/readback as the tester has pins. The AD664 is a particularly appropriate choice for a large-scale system because the low power requirements (under 500 mW) ease power supply and cooling requirements. Analog ground currents of 600  $\mu A$  or less make the ground current management task simpler. All DACs can be driven from the same system reference and will track over time and temperature. Finally, the small board area required by the AD664 (and AD345 and AD96687) allows a high functional density.

**X-Y Plotters**

Figure 30 is a block diagram of the control section of a microprocessor-controlled X-Y pen plotter. In this conceptual exercise, two of the DACs are used for the X-channel drive and two are used for the Y-channel drive. Each provides either the coarse or fine movement control for its respective channel. This approach offers increased resolution over some other approaches.

A designer can take advantage of the reset feature of the AD664 in the following manner. If the system is designed such that the "HOME" position of the pen (or galvanometer, beam, head or similar mechanism) results when the outputs of all of the DACs are at zero, then no system software is required to home the pen. A simple reset signal is sufficient.

Similarly, the transparent feature could be used to the same end. One code can be sent to all DACs at the same time to send the pen to the home position. Of course, this would require

some software where the previous example would require only a single reset strobe signal!

Drawing scaling can be achieved by taking advantage of the AD664's software programmable gain settings. If, for example, an "A" size drawing is created with gain settings of 1, then a "C" size drawing can be created by simply resetting all DAC gains to 2 and redrawing the object. Conversely, a "C" size drawing created with gains of 2 can be reduced to "A" size simply by changing the gains to 1 and redrawing. The same principle applies for conversion from "B" size to "D" size or "D" size to "B" size. The multiplying capability of the AD664 provides another scaling option. Changing the reference voltage provides a proportional change in drawing size. Inverting the reference voltage would invert the drawing.

Swapping digital input data from the X channel to the Y channel would rotate the drawing 90 degrees.

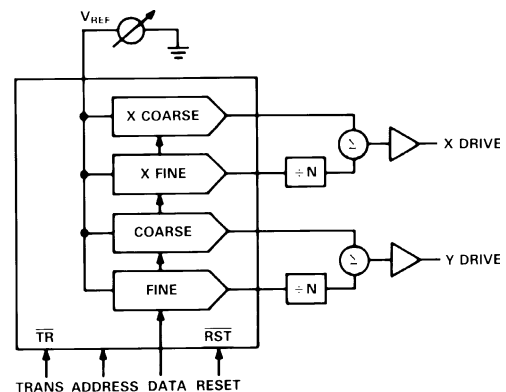


Figure 30. X-Y Plotter Block Diagram

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Output Range	Gain Error	Linearity Error	Package Options <sup>2</sup>
AD664JN-UNI	0°C to +70°C	0 to +V <sub>REF</sub>	±7 LSB	±0.75 LSB	N-28
AD664JN-BIP	0°C to +70°C	-V <sub>REF</sub> to +V <sub>REF</sub>	±7 LSB	±0.75 LSB	N-28
AD664JP	0°C to +70°C	Programmable	±7 LSB	±0.75 LSB	P-44A
AD664KN-UNI	0°C to +70°C	0 to +V <sub>REF</sub>	±5 LSB	±0.5 LSB	N-28
AD664KN-BIP	0°C to +70°C	-V <sub>REF</sub> to +V <sub>REF</sub>	±5 LSB	±0.5 LSB	N-28
AD664KP	0°C to +70°C	Programmable	±5 LSB	±0.5 LSB	P-44A
AD664AD-UNI	-40°C to +85°C	0 to +V <sub>REF</sub>	±7 LSB	±0.75 LSB	D-28
AD664AD-BIP	-40°C to +85°C	-V <sub>REF</sub> to +V <sub>REF</sub>	±7 LSB	±0.75 LSB	D-28
AD664AJ	-40°C to +85°C	Programmable	±7 LSB	±0.75 LSB	J-44
AD664BD-UNI	-40°C to +85°C	0 to +V <sub>REF</sub>	±5 LSB	±0.5 LSB	D-28
AD664BD-BIP	-40°C to +85°C	-V <sub>REF</sub> to +V <sub>REF</sub>	±5 LSB	±0.5 LSB	D-28
AD664BJ	-40°C to +85°C	Programmable	±5 LSB	±0.5 LSB	J-44
AD664BE	-40°C to +85°C	Programmable	±5 LSB	±0.5 LSB	E-44A
AD664SD-UNI	-55°C to +125°C	0 to +V <sub>REF</sub>	±7 LSB	±0.75 LSB	D-28
AD664SD-BIP	-55°C to +125°C	-V <sub>REF</sub> to +V <sub>REF</sub>	±7 LSB	±0.75 LSB	D-28
AD664TD-UNI	-55°C to +125°C	0 to +V <sub>REF</sub>	±5 LSB	±0.5 LSB	D-28
AD664TD-BIP	-55°C to +125°C	-V <sub>REF</sub> to +V <sub>REF</sub>	±5 LSB	±0.5 LSB	D-28

### NOTES

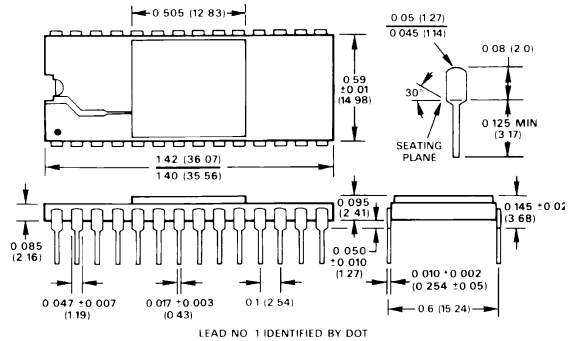
<sup>1</sup>For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD664/883B data sheet.

<sup>2</sup>D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; J = Leaded Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier.

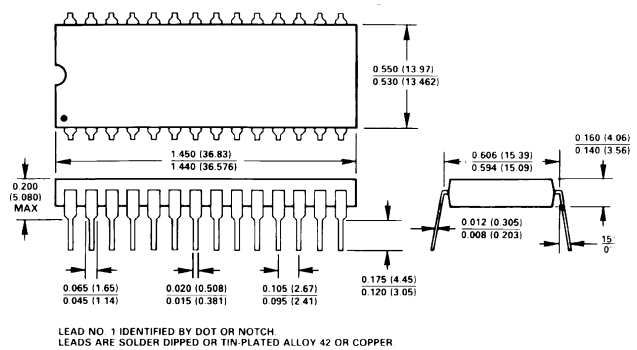
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

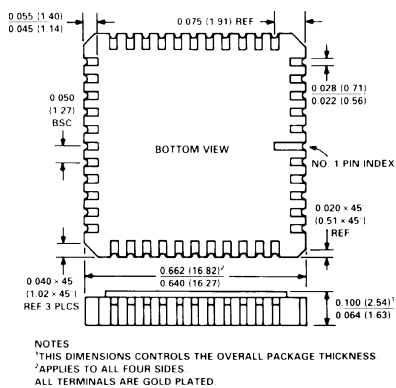
**D-28**  
28-Pin Ceramic DIP Package



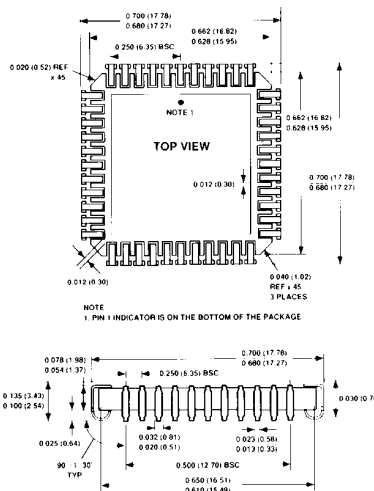
**N-28**  
28-Lead Plastic DIP



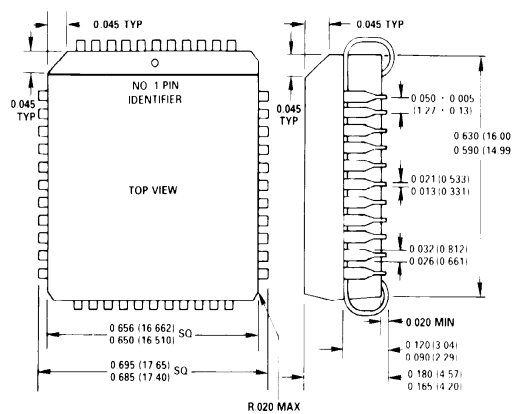
**E-44A**  
44-Pin LCC Package



**J-44**  
J-Leaded Chip Carrier



**P-44A**  
44-Lead Plastic Leaded Chip Carrier (PLCC)



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11. ECP NO. No registered users			
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13. DESCRIPTION OF REVISION			
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d. TITLE  Chief, Microelectronics Branch	e. SIGNATURE  Michael A. Frye		f. DATE SIGNED (YYMMDD) 96-03-08
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4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)	5. CAGE CODE	6. NOR NO.	
a. TYPED NAME (First, Middle Initial, Last)	Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5270	67268	5962-R032-95	
		7. CAGE CODE	8. DOCUMENT NO.	
		67268	5962-88719	
9. TITLE OF DOCUMENT MICROCIRCUIT, LINEAR, 12-BIT, QUAD D/A CONVERTER, MONOLITHIC SILICON		10. REVISION LETTER		11. ECP NO.
		a. CURRENT	b. NEW	No registered users
		Basic	A	
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13. DESCRIPTION OF REVISION				
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Sheet 1 of 2				
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Chief, Microelectronics Branch	Michael A. Frye		94-11-08	
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DESC-ELDS	Dan Wonnell		94-11-08	

Update second rank of a DAC

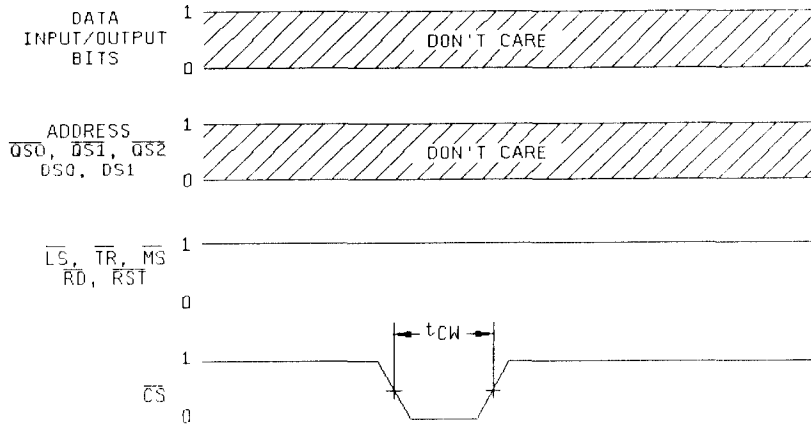


Diagram I

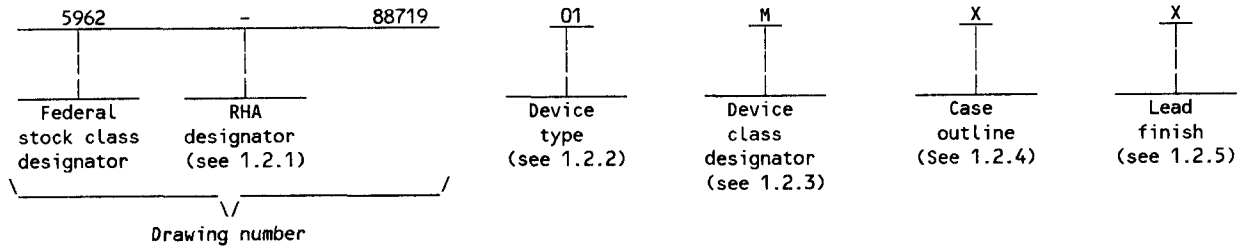




1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	AD664TD-UNI	D/A converter, 12-bit, unipolar
02	AD664TD-BIP	D/A converter, 12-bit, bipolar
03	AD664TE	D/A converter, 12-bit, unipolar/bipolar

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N44	44	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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1.3 Absolute maximum ratings. 1/

$V_{LL}$ to DGND	-----	0 V dc to +7 V dc
$V_{CC}$ to DGND	-----	0 V dc to +18 V dc
$V_{EE}$ to DGND	-----	-18 V dc to 0 V dc
Power dissipation ( $P_D$ )	-----	1000 mW
AGND to DGND	-----	-1 V dc to +1 V dc
Reference input	-----	$V_{ref} \leq \pm 10$ V dc and $V_{ref} \leq (V_{CC} - 2$ V, $V_{EE} + 2$ V)
$V_{CC}$ to $V_{EE}$	-----	0 V dc to +36 V dc
Digital inputs	-----	-0.3 V dc to +7 V dc
Analog inputs	-----	Indefinite shorts to $V_{CC}$ , $V_{LL}$ , $V_{EE}$ and GND
Lead temperature (soldering, 10 seconds)	-----	+300°C

1.4 Recommended operating conditions.

Input voltage requirements:

$V_{LL}$ max	-----	+5.0 V dc
$V_{CC}/V_{EE}$	-----	$\pm 15$ V dc
Ambient temperature range ( $T_A$ )	-----	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

- MIL-M-38510 - Microcircuits, General Specification for.
- MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

- MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
- MIL-STD-883 - Test Methods and Procedures for Microelectronics.
- MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

- MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

- MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 92 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified 1/	Group A sub- groups	Device type	Limits		Unit
					Min	Max	
Resolution	RES		1,2,3	ALL		12	Bits
Relative accuracy	RA		1	01,02		±3/4	LSB
				03		±1/2	
			2,3	01,02		±1	
				03		±3/4	
12	01,02		±1/2				
Differential nonlinearity	DNL	Major carry errors	2,3	ALL		±1	LSB
				1	01,02		
			12	01,02		±1/2	
Gain error	A <sub>E</sub>	All bits on	1	01,02		±7	LSB
				03		±5	
12	01,02		±5				
Gain temperature coefficient	TCA <sub>E</sub>	All bits on	1,2,3	ALL		±10	ppm/°C
Unipolar offset error	V <sub>OS</sub>	All bits off	1	01		±2	LSB
				03		±1	
12	01		±1				
Unipolar offset temperature coefficient	TCV <sub>OS</sub>	All bits off	1,2,3	01 03		±2	ppm/°C
Bipolar zero error 2/	B <sub>PZE</sub>	MSB on, all others off	1	02		±3	LSB
				03		±2	
12	02		±2				
Bipolar zero temperature coefficient	TCPZE	MSB on, all others off	1,2,3	02 03		±10	ppm/°C
Reference input resistance	R <sub>IN</sub>	3/	1	ALL	1.3	2.6	kΩ
Reference voltage range 4/	V <sub>REF</sub>	3/	1	ALL	V <sub>EE</sub> +2	V <sub>CC</sub> -2	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified 1/	Group A sub- groups	Device type	Limits		Unit
					Min	Max	
Voltage output, UNI 5/	V <sub>OU</sub>	3/	1	01 03	0	V <sub>CC</sub> -2	V
Voltage output, BPI	V <sub>OB</sub>		1	02 03	V <sub>CC</sub> -2	V <sub>EE</sub> +2	V
Output current	I <sub>O</sub>		1	ALL	5		mA
Current, short circuit	I <sub>SC</sub>		1	ALL		40	mA
Power supply current	I <sub>LL</sub>	V <sub>CC</sub> = +16.5 V, V <sub>EE</sub> = -16.5 V, V <sub>IH</sub> = +2 V, V <sub>IL</sub> = +0.8 V	1	ALL		6	mA
		V <sub>CC</sub> = +16.5 V, V <sub>EE</sub> = -16.5 V, V <sub>IH</sub> = V <sub>LL</sub> , V <sub>IL</sub> = 0 V				1	
	I <sub>CC</sub>	I <sub>CC</sub> : All bits on				15	
	I <sub>EE</sub>	I <sub>EE</sub> : All bits on				19	
Gain matching error 6/	mA <sub>E</sub>		1	01,02		±6	LSB
				03		±4	
			12	01,02		±4	
Bipolar zero matching error 7/	mB <sub>PZE</sub>		1	02		±3	LSB
				03		±2	
			12	02		±2	
Offset matching error 8/	mV <sub>OS</sub>		1	01		±2	LSB
				03		±1	
			12	01		±1	
Digital input high voltage	V <sub>IH</sub>		1,2,3	ALL	2.0		V
Digital input low voltage	V <sub>IL</sub>		1,2,3	ALL		0.8	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified 1/	Group A sub- groups	Device type	Limits		Unit
					Min	Max	
Digital inputs high current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>LL</sub> Data inputs	1,2,3	ALL		±10	μA
		V <sub>IN</sub> = V <sub>LL</sub> : $\overline{\text{CS}}/\overline{\text{DSO}}/\overline{\text{DS1}}/\overline{\text{RST}}/\overline{\text{RD}}/\overline{\text{LS}}$				±10	
		V <sub>IN</sub> = V <sub>LL</sub> $\overline{\text{MS}}/\overline{\text{TR}} \text{ 9/}$			±10		
		V <sub>IN</sub> = V <sub>LL</sub> $\overline{\text{QSO}}/\overline{\text{QS1}}/\overline{\text{QS2}} \text{ 9/}$				+10	
Digital inputs low current	I <sub>IL</sub>	V <sub>IN</sub> = DGND: Data inputs	1,2,3	ALL		±10	μA
		V <sub>IN</sub> = DGND: $\overline{\text{CS}}/\overline{\text{DSO}}/\overline{\text{DS1}}/\overline{\text{RST}}/\overline{\text{RD}}/\overline{\text{LS}}$				±10	
		V <sub>IN</sub> = DGND $\overline{\text{MS}}/\overline{\text{TR}} \text{ 9/}$				-10	
		V <sub>IN</sub> = DGND $\overline{\text{QSO}}/\overline{\text{QS1}}/\overline{\text{QS2}} \text{ 9/}$				±10	
Digital out low voltage	V <sub>OL</sub>		1,2,3	ALL		+0.4	V
Digital out high voltage	V <sub>OH</sub>		1,2,3	ALL	+2.4		V
Power supply gain sensitivity	PSGS	11.4 V ≤ V <sub>CC</sub> ≤ 16.5 V	1	ALL	±5		ppm/%
		-16.5 V ≤ V <sub>EE</sub> ≤ -11.4 V					
		4.5 V ≤ V <sub>LL</sub> ≤ 5.5 V					
$\overline{\text{CS}}$ pulse width	t <sub>w</sub>	Data input mode (figure 4 diagram A) 10/	9	ALL	80		ns
Data setup	t <sub>DS</sub>		10,11		100		
Data hold	t <sub>DH</sub>		9,10,11		0		
			9,10,11		15		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified 1/	Group A sub- groups	Device type	Limits		Unit
					Min	Max	
Adress setup	t <sub>AS</sub>	Data input mode <sup>10/</sup> (figure 4 diagram A)	9,10,11	ALL	0		ns
Adress hold	t <sub>AH</sub>		9,10,11		15		
$\overline{\text{LS}}$ setup	t <sub>LS</sub>		9,10,11		0		
$\overline{\text{LS}}$ hold	t <sub>LH</sub>		9,10,11		15		
Data setup	t <sub>DS</sub>	Data input mode <sup>10/</sup> (figure 4 diagram B)	9,10,11	ALL	0		
Data hold	t <sub>DH</sub>		9,10,11		0		
$\overline{\text{LS}}$ width	t <sub>LW</sub>		9		60		
			10,11		80		
$\overline{\text{LS}}$ setup	t <sub>LS</sub>		9,10,11		0		
$\overline{\text{CS}}$ hold	t <sub>CH</sub>		9		30		
			10,11		50		
Address setup	t <sub>AS</sub>		9,10,11		0		
Address hold	t <sub>AH</sub>		9,10,11		0		
$\overline{\text{MS}}$ setup	t <sub>MS</sub>		Mode select <sup>10/</sup> (figure 4 diagram C)		9,10,11	ALL	
Address setup	t <sub>AS</sub>	9,10,11		0			
Data setup	t <sub>DS</sub>	9,10,11		0			
$\overline{\text{LS}}$ width	t <sub>LW</sub>	9		60			
		10,11	70				

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified 1/	Group A sub- groups	Device type	Limits		Unit			
					Min	Max				
$\overline{CS}$ hold	t <sub>CH</sub>	Mode select <sup>10/</sup> (figure 4 diagram C)	9	ALL	70		ns			
			10,11		80					
Data hold	t <sub>DH</sub>		9,10,11		0					
$\overline{MS}$ hold	t <sub>MH</sub>		9,10,11		0					
Mode select	t <sub>MS</sub>	Mode select <sup>10/</sup> (figure 4 diagram D)	9,10,11	ALL	0					
$\overline{MS}$ hold	t <sub>MH</sub>		9,10,11		15					
$\overline{LS}$ setup	t <sub>LS</sub>		9,10,11		0					
Data setup	t <sub>DS</sub>		9,10,11		0					
$\overline{CS}$ hold	t <sub>w</sub>		9		80					
			10,11		100					
$\overline{LS}$ hold	t <sub>LH</sub>		9,10,11		15					
Data hold	t <sub>DH</sub>		9,10,11		15					
Address setup	t <sub>AS</sub>		Readback mode <sup>10/</sup> (figure diagram E and F)		9,10,11	ALL		0		
Address hold	t <sub>AH</sub>				9,10,11			0		
$\overline{RD}$ setup	t <sub>RS</sub>	9,10,11		0						
$\overline{RD}$ hold	t <sub>RH</sub>	9,10,11		0						

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified 1/	Group A sub- groups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{MS}}$ setup	t <sub>MS</sub>	Readback mode 10/ (figure 4 diagram E and F)	9,10,11	ALL	0		ns
$\overline{\text{MS}}$ hold	t <sub>MH</sub>	10/	9,10,11		0		
Data access	t <sub>DV</sub>		9		150		
			10,11		180		
Data release	t <sub>DF</sub>		9		60		
			10,11	75			
Reset width	t <sub>RW</sub>	Asynchronous reset 10/ (figure 4 diagram G)	9	ALL	80		
			10,11		100		
Address setup	t <sub>AS</sub>	Transparent mode 10/ (figure 4 diagram H)	9,10,11	03	0		
Quad select setup	t <sub>QS</sub>		9,10,11		0		
Transparent setup	t <sub>TS</sub>		9,10,11		0		
Transparent width	t <sub>TW</sub>		9		80		
			10,11		90		
Chip select hold	t <sub>CH</sub>		9		90		
			10,11		110		
Data hold	t <sub>DH</sub>		9,10,11		0		
Quad select setup	t <sub>QS</sub>		9,10,11	0			
Functional tests	FT	See paragraph 4.4.1 b	7,8				

- 1/ V<sub>CC</sub> = +15 V, V<sub>EE</sub> = -15 V, 50Ω resistor pin 6 to pin 7, A0, A1, A2, A3,  $\overline{\text{CS}}$  = Logic "0", V<sub>IH</sub> = 2.0 V, V<sub>IL</sub> = 0.8 V, unipolar configuration.
- 2/ Bipolar zero error is the difference from the ideal output (0 volts) and the actual output voltage with code 100 000 000 000 applied to the inputs.
- 3/ Parameter is guaranteed by design, not tested.
- 4/ A minimum power supply of ±12.0 V is required for a 10 V reference voltage.
- 5/ A minimum power supply of ±12.0 V is required for 0 to +10 V and ±10 V operation. A minimum power supply of ±11.4 V is required for -5 V to +5 V operation.
- 6/ Gain error matching is the largest difference in gain error between any two DACs in one package.
- 7/ Bipolar zero matching is the largest difference in bipolar zero error between any two DACs in one package.
- 8/ Offset error matching is the largest difference in offset error between any two DACs in one package.
- 9/ Device type 03 only.
- 10/ Timing specifications are relative to  $\overline{\text{CS}}$ , V<sub>CC</sub> = +15 V, V<sub>EE</sub> = -15 V, V<sub>REF</sub> = +10 V, T<sub>A</sub> = +25°C. Specifications are guaranteed but not tested. Refer to figure 4.

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Device types	01 and 02	03
Case outlines	X	Y
Terminal number	Terminal symbol	
1	V <sub>REF</sub>	<u>RD</u>
2	V <sub>OUTC</sub>	LS
3	V <sub>OUTD</sub>	NC
4	<u>CS</u>	AGND
5	DS0	V <sub>CC</sub>
6	DS1	V <sub>EE</sub>
7	<u>DGND</u>	R <sub>FA</sub>
8	RST	V <sub>OUTA</sub>
9	DB0(LSB)	V <sub>OUTB</sub>
10	DB1	R <sub>FB</sub>
11	DB2	V <sub>REF</sub>
12	DB3	R <sub>FC</sub>
13	DB4	V <sub>OUTC</sub>
14	DB5	V <sub>OUTD</sub>
15	DB6	R <sub>FD</sub>
16	DB7	NC
17	DB8	NC
18	DB9	CS
19	DB10	DS0
20	DB11(MSB)	DS1
21	V <sub>LL</sub>	DGND
22	<u>RD</u>	<u>RST</u>
23	LS	QSD
24	AGND	QS1
25	V <sub>CC</sub>	QS2
26	V <sub>EE</sub>	TR
27	V <sub>OUTA</sub>	MS
28	V <sub>OUTB</sub>	DB0(LSB)
29	---	DB1
30	---	DB2
31	---	DB3
32	---	DB4
33	---	DB5
34	---	NC
35	---	DB6
36	---	DB7
37	---	DB8
38	---	DB9
39	---	DB10
40	---	DB11
41	---	NC
42	---	V <sub>LL</sub>
43	---	NC
44	---	NC

FIGURE 1. Terminal connections.

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Function	DS1, DSO	$\overline{LS}$	$\overline{MS}$	$\overline{TR}$	$\overline{QS0}, \overline{1}, \overline{2}$ (see note 1)	$\overline{RD}$	$\overline{CS}$	$\overline{RST}$
Load 1 <sup>st</sup> rank								
DACA	00	0	1	1	Select quad	1	1→0	1
DACB	01	0	1	1	Select quad	1	1→0	1
DACC	10	0	1	1	Select quad	1	1→0	1
DACD	11	0	1	1	Select quad	1	1→0	1
Load 2 <sup>nd</sup> rank	XX	1	1	1	XXX	1	1→0	1
Read 2 <sup>nd</sup> rank	Select D/A	X	1	1	Select quad	0	1→0	1
Reset	XX	X	X	X	XXX	X	X	0
(see note 1) Transparent all DACs	XX	1	1	0	000	1	1→0	1
DACA	00	0	1	0	000	1	1→0	1
DACB	01	0	1	0	000	1	1→0	1
DACC	10	0	1	0	000	1	1→0	1
DACD	11	0	1	0	000	1	1→0	1
(see notes 1 and 2) Mode select								
1st rank	XX	0	0	1	00X	1	1→0	1
2nd rank	XX	1	0	1	XXX	1	1→0	1
Readback mode (see note 1)	XX	X	0	1	00X	0	1→0	1

NOTES:

1. For device type 03 only.
2. For MS, TR, LS = 0, a MS 1st write occurs.
3. X = Don't care.

FIGURE 2. Truth table.

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28-Terminal

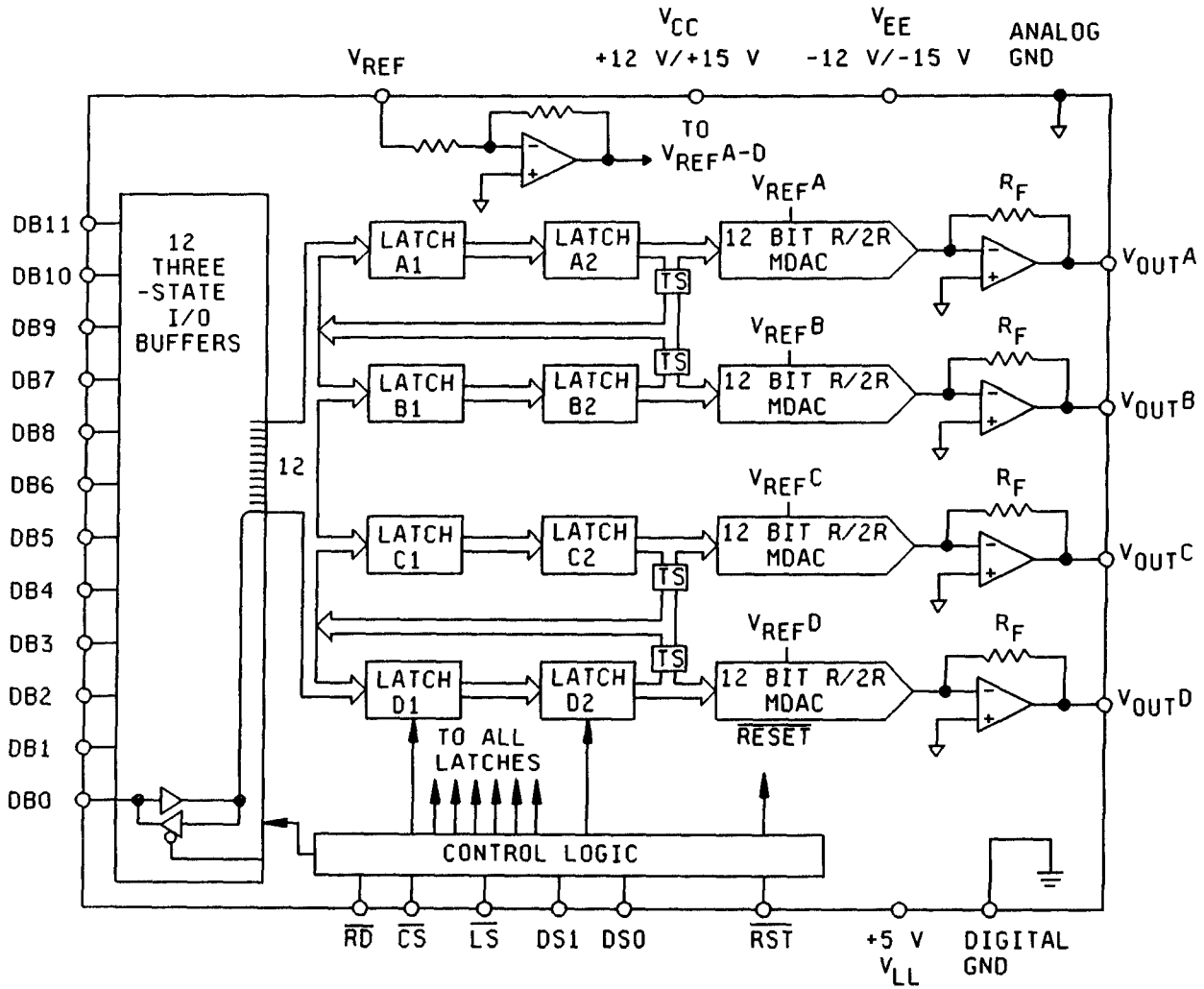


FIGURE 3. Block diagram.

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44-Terminal

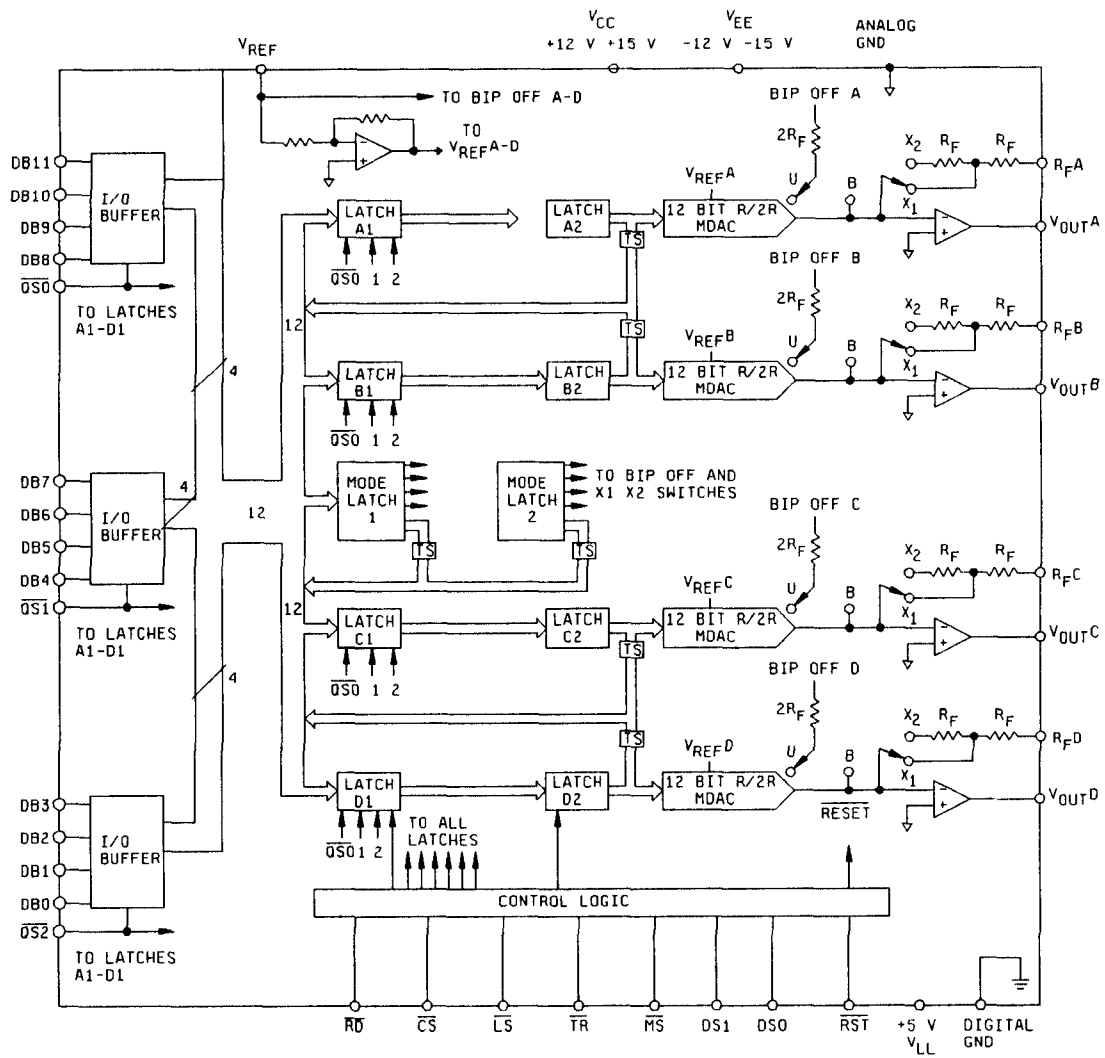


FIGURE 3. Block diagram - Continued.

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Preload first rank of DAC

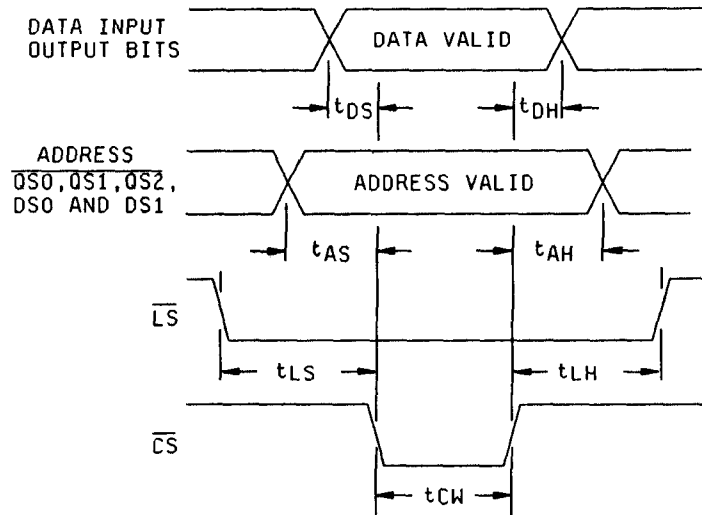


Diagram A

Update output of a single DAC

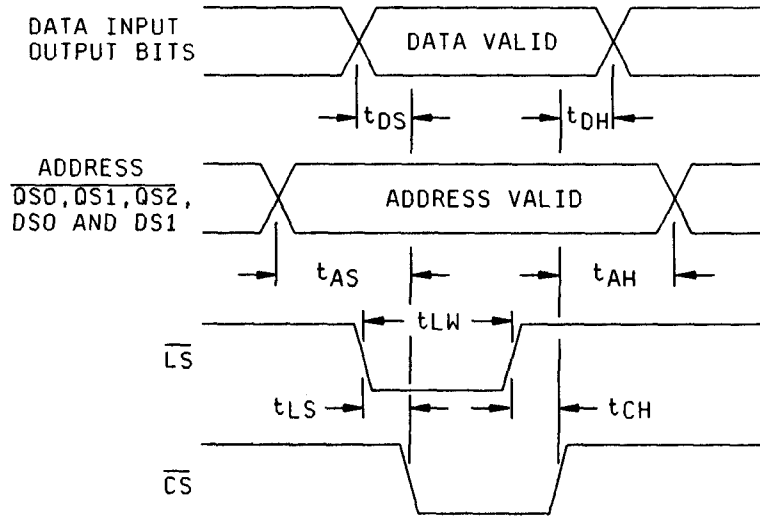


Diagram B

FIGURE 4. Timing diagram.

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Load and update mode of one DAC

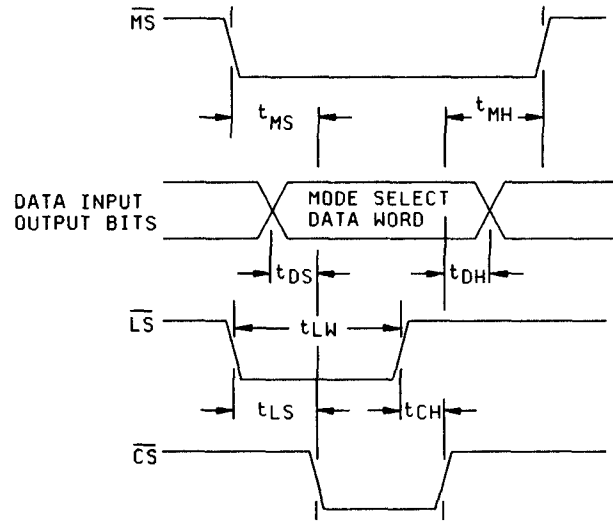


Diagram C

Preload mode select register

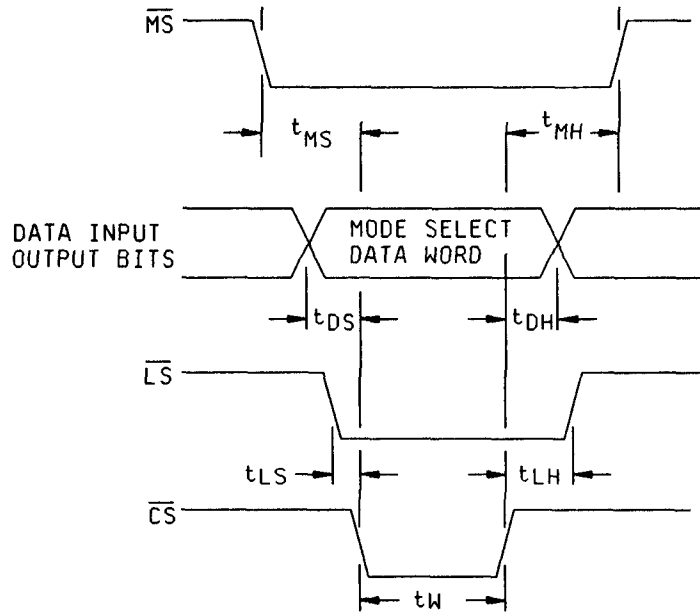


Diagram D

FIGURE 4. Timing diagram - Continued.

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DAC input code readback

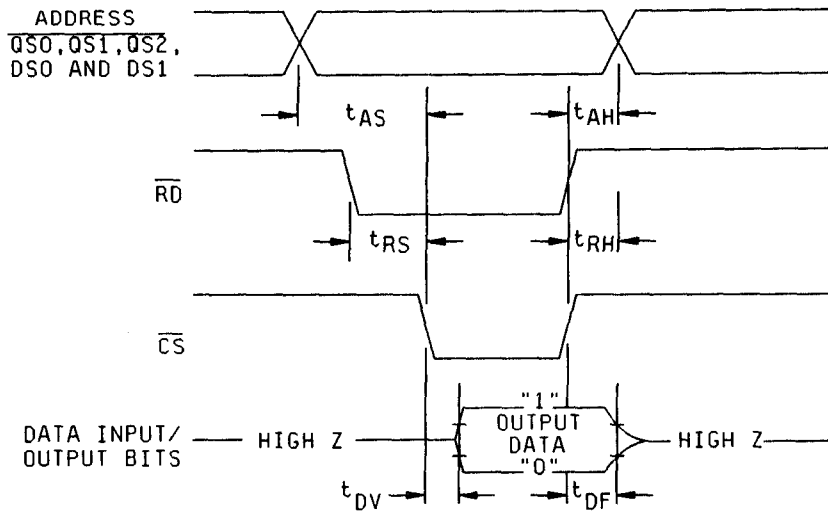


Diagram E

Mode select readback

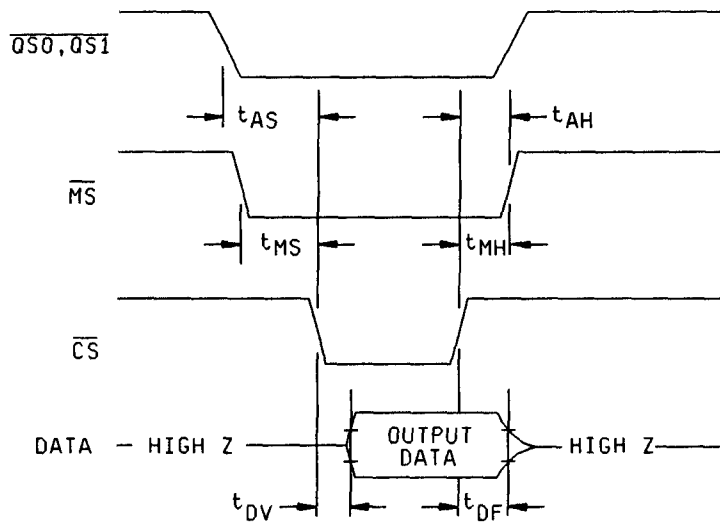


Diagram F

FIGURE 4. Timing diagram - Continued.

STANDARDIZED  
MILITARY DRAWING  
DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
A

5962-88719

REVISION LEVEL

SHEET

17



Asynchronous reset operation

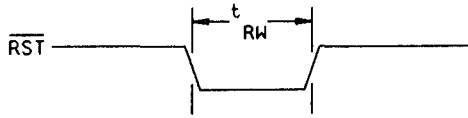


Diagram G

Fully transparent mode

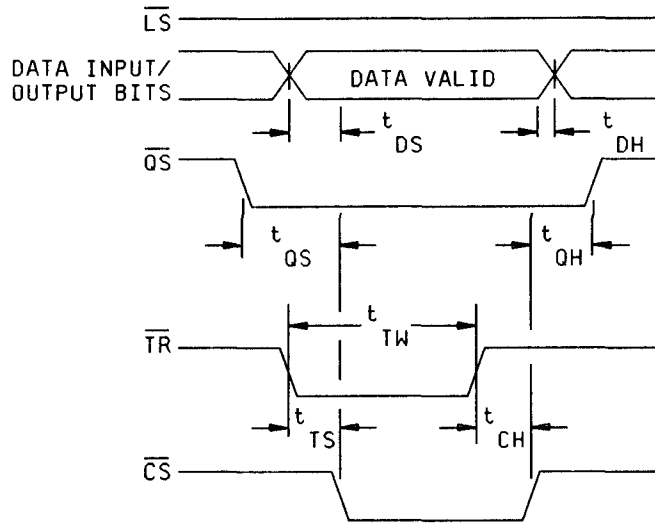


Diagram H

FIGURE 4. Timing diagram - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or B. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1	1	1
Final electrical parameters (see 4.2)	1/ 1,2,3,9, 10,11	1/ 1,2,3,9, 10,11	1/ 1,2,3,9, 10,11	1/ 1,2,3,9, 10,11	1/ 1,2,3,9, 10,11
Group A test requirements (see 4.4)	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11
Group B end-point electrical parameters (see 4.4)	---	---	1,2,3,9, 10,11	---	---
Group C end-point electrical parameters (see 4.4)	1	1	---	1	1,2,3,9, 10,11
Group D end-point electrical parameters (see 4.4)	1	1	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---	---	---

1/ PDA applies to subgroup 1.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- c. Special subgroup 12 (as referenced in table I) added for grading and selection tests at +25°C.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

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4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A or B. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b.  $T_A = +125^{\circ}\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA environment and level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

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6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-01-14

Approved sources of supply for SMD 5962-88719 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-8871901MXX	51640	AD664TD-UNI/883B
5962-8871902MXX	51640	AD664TD-BIP/883B
5962-8871903MYX	51640	AD664TE/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

51640

Vendor name and address

Analog Devices  
804 Woburn Street  
Wilmington, MA 01887

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.

## Package/Price Information

For detailed packaging information, please select the Datasheets button.

Monolithic 12-Bit Quad DAC

Model	Status	Package Description	Pin Count	Temperature Range	Price* (100-499)
5962-8871901MXA	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$342.61
5962-8871902MXA	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$342.61
5962-8871903MYA	PRODUCTION	CER. LEADLESS CHIP CARRIER	44	MILITARY	\$411.07
AD664AD-BIP	PRODUCTION	S/B OR B/B CERAMIC DIP	28	INDUSTRIAL	\$71.81
AD664AD-UNI	PRODUCTION	S/B OR B/B CERAMIC DIP	28	INDUSTRIAL	\$71.81
AD664AJ	PRODUCTION	CER. J-LEAD CHIP CARRIER	44	INDUSTRIAL	\$78.20
AD664BD-BIP	PRODUCTION	S/B OR B/B CERAMIC DIP	28	INDUSTRIAL	\$91.21
AD664BD-UNI	PRODUCTION	S/B OR B/B CERAMIC DIP	28	INDUSTRIAL	\$91.21
AD664BE	PRODUCTION	CER. LEADLESS CHIP CARRIER	44	INDUSTRIAL	\$96.18
AD664BJ	PRODUCTION	CER. J-LEAD CHIP CARRIER	44	INDUSTRIAL	\$96.18
AD664JN-BIP	PRODUCTION	PLASTIC/EPOXY DIP	28	COMMERCIAL	\$52.53
AD664JN-UNI	PRODUCTION	PLASTIC/EPOXY DIP	28	COMMERCIAL	\$52.53
AD664JP	PRODUCTION	PLASTIC LEAD CHIP CARRIER	44	COMMERCIAL	\$60.85
AD664KN-BIP	PRODUCTION	PLASTIC/EPOXY DIP	28	COMMERCIAL	\$71.25
AD664KN-UNI	PRODUCTION	PLASTIC/EPOXY DIP	28	COMMERCIAL	\$71.25
AD664KP	PRODUCTION	PLASTIC LEAD CHIP CARRIER	44	COMMERCIAL	\$82.92
AD664SD-BIP	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$245.60
AD664SD-BIP/883B	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$304.47
AD664SD-UNI	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$245.60
AD664SD-UNI/883B	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$304.47
AD664TD-BIP	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$292.35

AD664TD-BIP/883B	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$342.61
AD664TD-UNI	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$292.35
AD664TD-UNI/883B	PRODUCTION	S/B OR B/B CERAMIC DIP	28	MILITARY	\$342.61
AD664TE/883B	PRODUCTION	CER. LEADLESS CHIP CARRIER	44	MILITARY	\$411.07
AD664TJ/883B	PRODUCTION	CER. J-LEAD CHIP CARRIER	44	MILITARY	\$411.07

\* This price is provided for budgetary purposes as recommended list price in U.S. Dollars per unit the stated volume. Pricing displayed for Evaluation Boards and Kits is based on 1-piece pricing. View [Pricing and Availability](#) (currently available to North American customers) for further information.