MOTOROLA

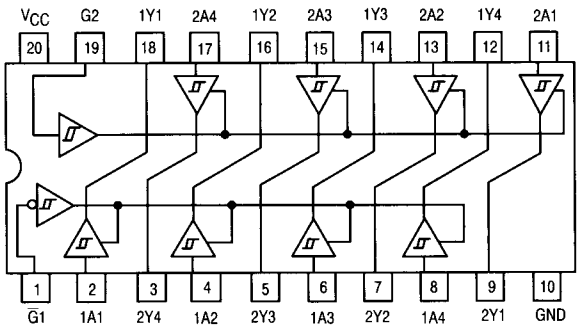
Octal Buffer/Line Driver With 3-State Outputs (Non-Inverting)

ELECTRICALLY TESTED PER:
MIL-M-38510/32402

The 54LS241 is an Octal Buffer and Line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which will provide improved PC board density.

- Hysteresis at Inputs to Improve Noise Margins
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC DIAGRAM



TRUTH TABLE		
Inputs		Output
$\overline{G1}$	D	
L	L	L
L	H	H
H	X	(Z)

TRUTH TABLE		
Inputs		Output
G2	D	
H	L	L
H	H	H
L	X	(Z)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

Military 54LS241

AVAILABLE AS:

1) JAN: JM38510/32402BXA
2) SMD: N/A
3) 883: 54LS241/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$\overline{G1}$	1	1	1	GND
1A1	2	2	2	V_{CC}
2Y4	3	3	3	V_{CC}
1A2	4	4	4	V_{CC}
2Y3	5	5	5	V_{CC}
1A3	6	6	6	V_{CC}
2Y2	7	7	7	V_{CC}
1A4	8	8	8	V_{CC}
2Y1	9	9	9	V_{CC}
GND	10	10	10	GND
2A1	11	11	11	V_{CC}
1Y4	12	12	12	V_{CC}
2A2	13	13	13	V_{CC}
1Y3	14	14	14	V_{CC}
2A3	15	15	15	V_{CC}
1Y2	16	16	16	V_{CC}
2A4	17	17	17	V_{CC}
1Y1	18	18	18	V_{CC}
G2	19	19	19	V_{CC}
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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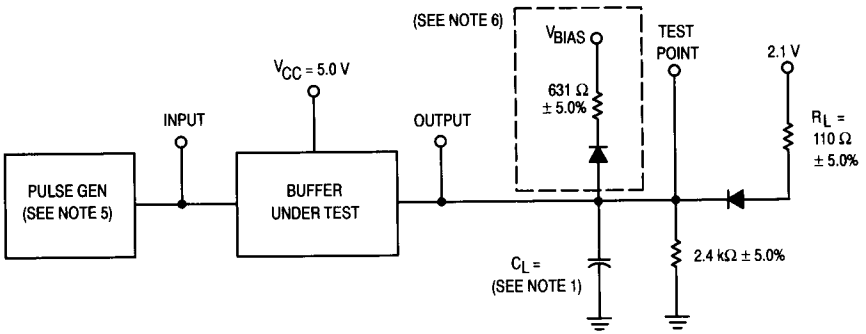
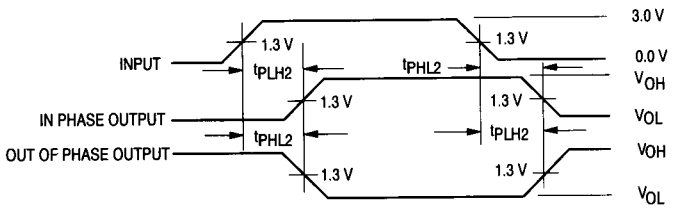
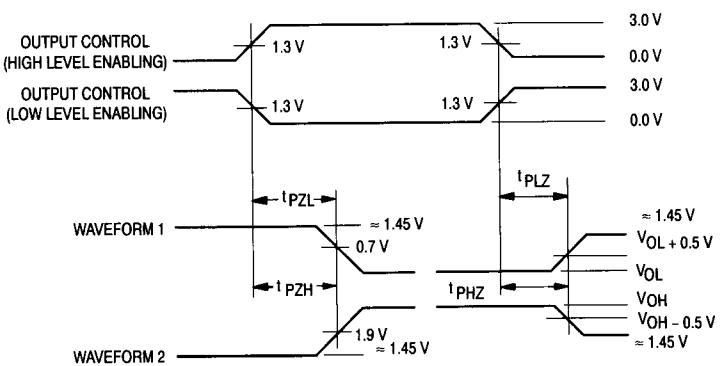
AC TEST CIRCUIT



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



REFERENCE NOTES ON PAGE 5-301

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OHH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = − 3.0 mA, V_{IN} = 2.0 V (other inputs are open), $\overline{G}1/G2$ = 0.7 V/2.0 V or open per truth table.
V_{OHL}	Logical "1" Output Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V, I_{OH} = − 12 mA, V_{IN} = 2.0 V (other inputs are open), $\overline{G}1/G2$ = 0.5 V/2.0 V or open per truth table.
V_{OL1}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IN} = 0.7 V (other inputs are open), $\overline{G}1/G2$ = 0.7 V/ 2.0 V or open per truth table.
V_{OL2}	Logical "0" Output Voltage		0.45		0.45		0.45	V	V_{CC} = 4.5 V, I_{OL} = 18 mA, V_{IN} = 0.7 V (other inputs an open), $\overline{G}1/G2$ = 0.7 V/ 2.0 V or open per truth table.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, all other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current	− 5.0	− 200	− 5.0	− 200	− 5.0	− 200	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{OS}	Output Short Circuit Current	− 40	− 225	− 40	− 225	− 40	− 225	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (other inputs are open), V_{OUT} = GND, $\overline{G}1/G2$ = GND/5.5 V or open per truth table.
I_{IOZH}	Output Off Current High		20		20		20	µA	V_{CC} = 5.5 V, all inputs are open, V_{OUT} = 2.7 V, $\overline{G}1/G2$ = 2.0 V/0.7 V or open per truth table.
I_{IOZL}	Output Off Current Low		− 20		− 20		− 20	µA	V_{CC} = 5.5 V, all inputs are open, V_{OUT} = 0.4 V, $\overline{G}1/G2$ = 2.0 V/0.7 V or open per truth table.
I_{CCH}	Power Supply Current		27		27		27	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{G}1$ = GND, G2 = 5.5 V.
I_{CCL}	Power Supply Current		46		46		46	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), $\overline{G}1/G2$ = 5.5 V.
I_{CCZ}	Power Supply Current Off		54		54		54	mA	V_{CC} = 5.5 V, all inputs are open, $\overline{G}1/G2$ = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Switching Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Output High-Low	2.0 —	18 18	2.0 —	23 23	2.0 —	23 23	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Output Low-High	2.0 —	18 18	2.0 —	23 23	2.0 —	23 23	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLZ1} t_{PLZ1}	Propagation Delay /Data-Output Output Low-High	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHZ1} t_{PHZ1}	Propagation Delay /Data-Output Output High-Low	2.0 —	35 18	2.0 —	45 40	2.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZL1} t_{PZL1}	Propagation Delay /Data-Output Output Low-High	2.0 —	30 30	2.0 —	39 34	2.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZH1} t_{PZH1}	Propagation Delay /Data-Output Output High-Low	2.0 —	30 23	2.0 —	39 34	2.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.

NOTES:

1. C_L = 50 pF ± 10%. C_L includes scope probe and jig capacitance.
2. All diodes are 1N3064 or equivalent.
3. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. In the test circuit example, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics:
   PRR ≤ 1.0 MHz, t_p = 500 ns, Z_{OUT} ≈ 50 Ω, V_{gen} = 3.0 V, t_r ≤ 15 ns and t_f ≤ 6.0 ns between 0.7 V and 2.7 V.
6. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all tests except for t_{PHZ}, for t_{PHZ} tests, V_{BIAS} shall be − 0.6 V.

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