REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct typing errors in truth table and table I. Reword paragraph 4.3.1c. Update vendors part numbers.	1987 July 13	M. A. Frye
B	Add one vendor, CAGE 18324 and their part numbers. Add programming procedure and waveforms for circuit B.	1988 May 17	M. A. Frye
C	Change vendor similar part numbers from 82523B/BEA and 82523B/BFA to 82S123B/BEA and 82S123B/BFA respectively. Table I changed V_{OL} max limit from 0.45 volt to 0.5 volt and I_{OS} max limit from -90 mA to -100 mA. Editorial changes throughout.	1989 Jan 12	M. A. Frye
D	Updated boilerplate. Removed programming specifics from drawing, including table III. Separated source bulletin from body of drawing. - glg	00-08-09	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D					
	SHEET	1	2	3	4	5	6	7	8	9	10					

PMIC N/A	PREPARED BY Steve Duncan	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Ray Monnin	
	APPROVED BY Michael. A. Frye	MICROCIRCUITS, MEMORY, DIGITAL, 32 x 8-BIT PROM, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 1986 July 17	
	REVISION LEVEL D	SIZE A CAGE CODE **67268** **5962-86703** SHEET 1 OF 10

DSCC FORM 2233
APR 97

5962-E476-00

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-86703	01	E	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	1/	32 x 8-bit PROM, T.S.	50 ns
02	1/	32 x 8-bit PROM, T.S.	35 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	dual-in-line package
F	GDFP2-F16 or CDFP3-F16	16	flat package
2	CQCC1-N20	20	square leadless chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D): 2/	633 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
DC voltage applied to outputs during programming	21 V dc
DC voltage applied to outputs (except during programming)	-0.5 V dc to +V_{CC} maximum
Output current into outputs during programming (maximum duration of one second)	250 mA
DC input current	-30 mA to +5 mA

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Maximum low level input low voltage (V_{IL})	0.8 V dc
Minimum high level input high voltage (V_{IH})	2.0 V dc
Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.
2/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3. When testing is required per 4.3 herein, the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be specified by an altered item drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH} 1/	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -2.0$ mA, V_{CC} = min.	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL} 1/	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 16$ mA, V_{CC} = min.	1, 2, 3	All		0.5	V
Input high level voltage	V_{IH} 1/	Guaranteed input logical high voltage for all inputs.	1, 2, 3	All	2.0		V
Input low level voltage	V_{IL} 1/	Guaranteed input logical low voltage for all inputs.	1, 2, 3	All		0.8	V
High level input current	I_{IH}	V_{CC} = max., $V_{IN} = 2.7$ V	1, 2, 3	All		25	µA
Low level input current	I_{IL}	V_{CC} = max., $V_{IN} = 0.45$ V	1, 2, 3	All		-250	µA
Output short-circuit current	I_{OS}	$V_{CC} = 5.5$ V, $V_O = 0$ V 2/	1, 2, 3	All	-20	-100	mA
Power supply current	I_{CC}	V_{CC} = max. All inputs = GND	1, 2, 3	All		115	mA
Input clamp voltage	V_I 1/	V_{CC} = min., $I_{IN} = -18$ mA	1, 2, 3	All		-1.2	V
Output leakage current	I_{CEX}	V_{CC} = max.; $V_{CS} = 2.4$ V; $V_O = 4.5$ V	1, 2, 3	All		40	µA
		V_{CC} = max.; $V_{CS} = 2.4$ V; $V_O = 2.4$ V				40	
		V_{CC} = max.; $V_{CS} = 2.4$ V; $V_O = 0.4$ V				-40	
Address access time	t_{AA}	See figures 3 and 4 3/	9, 10, 11	01		50	ns
				02		35	
Enable access time	t_{EA}	See figures 3 and 4 4/	9, 10, 11	01		30	ns
				02		25	
Enable recovery time	t_{ER}	See figures 3 and 4 4/	9, 10, 11	01		30	ns
				02		25	

1/ These are absolute voltages with respect to device ground pin and include all overshoots due to system or tester noise or both. Do not attempt to test these values without suitable equipment.
2/ Not more than one output should be shorted at a time. Duration of the short circuit should not be more than 1 second.
3/ Parameter t_{AA} is tested with switch S1 closed and $C_L = 30$ pF.
4/ Parameter t_{EA} is tested with $C_L = 30$ pF to the 1.5 V; S1 is open for high impedance to high tests and closed for high impedance to low tests. Parameter t_{ER} is tested with $C_L = 5$ pF. High to high impedance tests are made with S1 open to an output voltage of V_{OH} -0.5 V. Low to high impedance tests are made with S1 closed to the V_{OL} +0.5 V level.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, Appendix A.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for the selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices processed to an altered item drawing may be programmed either before or after burn-in at the discretion of the manufacturer. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II.

All device types			
Case Outlines	E, F		2
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	O0	1	NC
2	O1	2	O0
3	O2	3	O1
4	O3	4	O2
5	O4	5	O3
6	O5	6	NC
7	O6	7	O4
8	GND	8	O5
9	O7	9	O6
10	A0	10	GND
11	A1	11	NC
12	A2	12	O7
13	A3	13	A0
14	A4	14	A1
15	$\overline{CS}$	15	A2
16	VCC	16	NC
17	- - -	17	A3
18	- - -	18	A4
19	- - -	19	$\overline{CS}$
20	- - -	20	VCC

FIGURE 1. Terminal connections.

Word number	$\overline{CS}$	Address					Data							
		A4	A3	A2	A1	A0	O7	O6	O5	O4	O3	O2	O1	O0
N/A	L H	X X	X X	X X	X X	X X	5/ OC	5/ OC	5/ OC	5/ OC	5/ OC	5/ OC	5/ OC	5/ OC

Notes:
1. NA = not applicable.
2. X = Input may be high level, low level, or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with enable input at low level.
5. The outputs for an unprogrammed device shall be low.

FIGURE 2. Truth table.

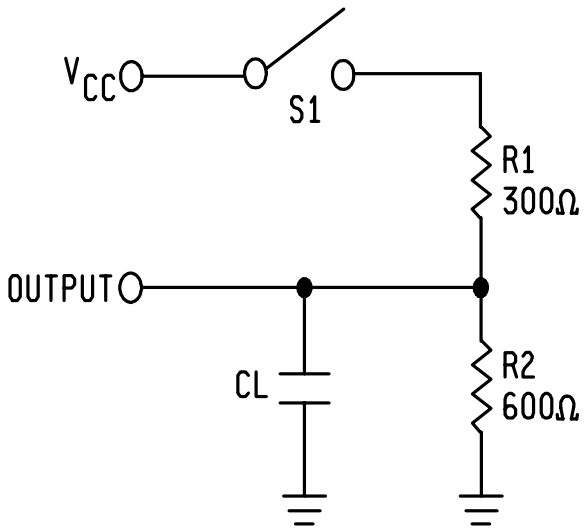

FIGURE 3. Switching test circuit.

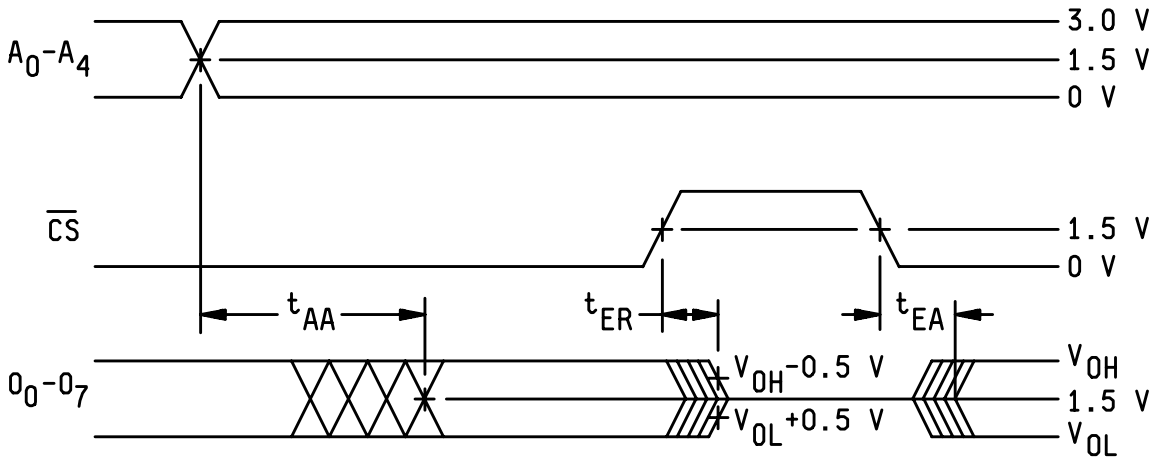

FIGURE 4. Switching waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9,10**,11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroups 1 and 7.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9. 10, and 11. Either of two techniques is acceptable.

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883

c. The group C, subgroup 1 sample shall include devices tested in accordance with 4.3.1c.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone 614-692-0674.

6.6 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-08-09

Approved sources of supply for SMD 5962-86703 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-8670301EA	0C7V7	82S123A/BEA
	3/	82S123A/BEA
	58625	SL82S123A/BEA
	3/	AM27S19/BEA
5962-8670301FA	0C7V7	82S123A/BFA
	3/	82S123A/BFA
	58625	SL82S123A/BFA
	3/	AM27S19/BFA
5962-86703012A	3/	AM27S19/B2A
5962-8670302EA	0C7V7	82S123B/BEA
	3/	82S123B/BEA
	58625	SL82S123B/BEA
	3/	AM27S19A/BEA
5962-8670302FA	0C7V7	82S123B/BFA
	3/	82S123B/BFA
	58625	SL82S123B/BFA
	3/	AM27S19A/BFA
5962-86703022A	3/	AM27S19A/B2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP LABS 3605 Kifer Road Santa Clara, CA 95051
58625	Lansdale Semiconductor Inc. 2412 W. Huntington Drive Tempe, AZ 85282-3134