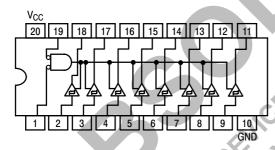
# **Octal Buffer/Line Driver** with 3-State Outputs

The SN74LS541 is an octal buffer and line driver with the same functions as the LS241, but with pinouts on the opposite side of the package.

This device type is designed to be used as a memory address driver, clock driver and bus-oriented transmitter/receiver. This device is especially useful as output ports for the microprocessors, allowing ease of layout and greater PC board density.

- Hysteresis at Inputs to Improve Noise Margin
- PNP Inputs Reduce Loading
- 3-State Outputs Drive Bus Lines
- Inputs and Outputs Opposite Side of Package, Allowing Easier Interface to Microprocessors
- Input Clamp Diodes Limit High-Speed Termination Effects

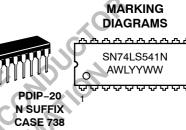
# LOGIC AND CONNECTION DIAGRAM DIP (TOP VIEW)



# **GUARANTEED OPERATING RANGES**

			· / /		w.
Symbol	Parameter	Min	Тур	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High		ζ.	-15	mA
I <sub>OL</sub>	Output Current – Low			24	mA
		÷			





 SOIC-20
 LS541

 DW SUFFIX
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 CASE 751D
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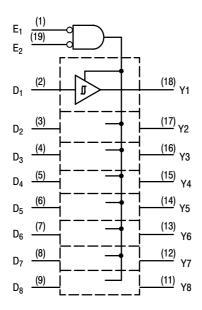
A = Assembly Location WL = Wafer Lot Y, YY = Year WW = Work Week

#### **ORDERING INFORMATION**

Device	Package	Shipping	
SN74LS541N	I74LS541N PDIP-20		
SN74LS541DW	SOIC-WIDE	38 Units/Rail	
SN74LS541DWR2	SOIC-WIDE	2500/Tape & Reel	
SN74LS541M	SOEIAJ-20	See Note 1	
SN74LS541MEL	SOEIAJ-20	See Note 1	

 For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

## **BLOCK DIAGRAM**



IN	PUTS	3	OUTPUTS		
E <sub>1</sub>	E <sub>2</sub>	D	LS540	LS541	
L	L	Н	L	Н	
Н	Х	X	Z	Z	
Х	Н	X	Z	Z	
L	L	L	Н	L	

L = LOW Voltage Level H = HIGH Voltage Level X = Immaterial

Z = High Impedance

D <sub>7</sub> (8) D <sub>8</sub> (9)	(12) (12) (11) (11) (11) (12) (12) (12)		OUCTOR
DC CHARACTERISTICS	OVER OPERATING TEMPE	ERATURE RANGE (unless otherwise s	specified)

		Limits					
Symbol	Parameter	Min	Тур	Max	Unit	Tes	t Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			v	Guaranteed Input HIGH Voltage for All Inputs	
VIL	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> =	–18 mA
Maria	Output HIGH Voltage	2.4	3.4	2	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> =	–3.0 mA
V <sub>OH</sub>	Output High Voltage	2.0	1		V	$V_{CC}$ = MIN, $I_{OH}$ =	MAX, $V_{IL} = 0.5 V$
		2	0.25	0.4	V	I <sub>OL</sub> = 12 mA	$V_{CC} = V_{CC} MIN,$
V <sub>OL</sub>	Output LOW Voltage		0.35	0.5	V	I <sub>OL</sub> = 24 mA	· V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
$V_{T+}-V_{T-}$	Hysteresis	0.2	0.4		V	V <sub>CC</sub> = MIN	
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	$V_{CC} = MAX, V_{OUT} = 2.7 V$	
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	$V_{CC} = MAX, V_{OUT} = 0.4 V$	
l	Input HIGH Current	Ċ		20	μA	$V_{CC} = MAX, V_{IN} =$	= 2.7 V
IIH				0.1	mA	$V_{CC} = MAX, V_{IN} = 7.0 V$	
IIL	Input LOW Current			-0.2	mA	$V_{CC} = MAX, V_{IN} = 0.4 V$	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-40		-225	mA	V <sub>CC</sub> = MAX	
	Power Supply Current Total, Output HIGH			32	mA		
ICC	Total, Output LOW			52	mA	$V_{CC} = MAX$	
1 Not more	Total Output 3-State			55	mA		

1. Not more than one output should be shorted at a time, nor for more than 1 second.

### AC CHARACTERISTICS ( $T_A = 25^{\circ}C$ )

			Limits				
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions	
t <sub>PLH</sub>	Propagation Delay,		12	15			
t <sub>PHL</sub>	Data to Output		12	18	ns		
t <sub>PZH</sub>	Output Enable Time to HIGH Level		15	32	ns ns	$V_{CC} = 5.0 \text{ V}$ $C_{L} = 45 \text{ pF}$ $R_{I} = 667 \Omega$	
t <sub>PZL</sub>	Output Enable Time to LOW Level		20	38			
t <sub>PHZ</sub>	Output Disable Time to HIGH Level		10	18	ns	0.5075	
t <sub>PLZ</sub>	Output Disable Time to LOW Level		15	29	ns	C <sub>L</sub> = 5.0 pF	

## AC WAVEFORMS

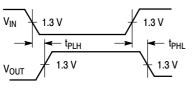
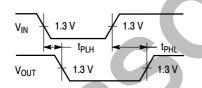


Figure 1.



1.5 V

0.5 V

1.5 V

t<sub>PHZ</sub> ≥V<sub>OH</sub>

≈[].5 V 0.5 V

Figure 2.

t<sub>PZL</sub>

1.5 V ډډ

Figure 3.

1.5 V

1.5 V

t<sub>PZH</sub>

1.5 V

 $V_{\mathsf{E}}$ 

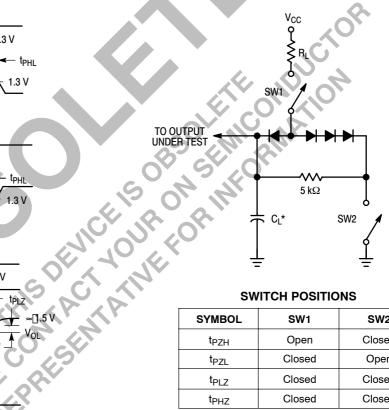
 $V_{\mathsf{E}}$ 

V<sub>OUT</sub>

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 $V_{\mathsf{E}}$ 

V<sub>OUT</sub>



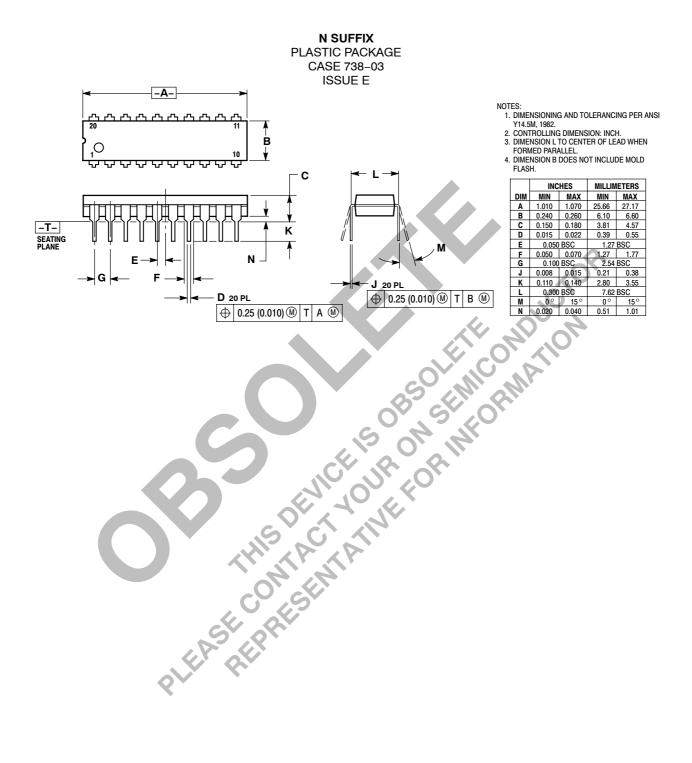
# SWITCH POSITIONS

SYMBOL	SW1	SW2		
t <sub>PZH</sub>	Open	Closed		
t <sub>PZL</sub>	Closed	Open		
t <sub>PLZ</sub>	Closed	Closed		
t <sub>PHZ</sub>	Closed	Closed		

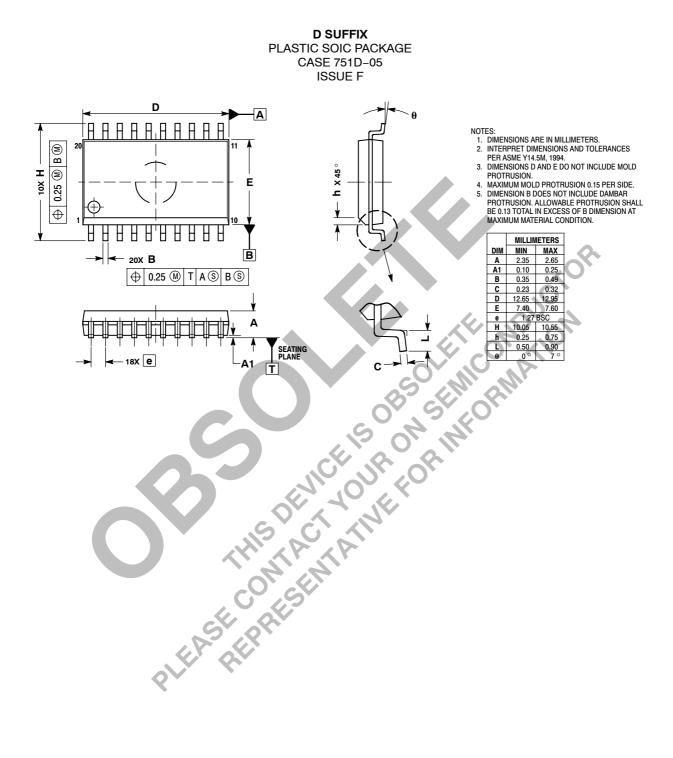
Figure 4.

Figure 5.

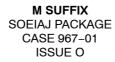
### PACKAGE DIMENSIONS



### PACKAGE DIMENSIONS



#### PACKAGE DIMENSIONS





NOTES DIMENSIONING AND TOLERANCING PER ANSI

- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006)
- TERMINAL NUMBERS ARE SHOWN FOR
- INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD

	MILLIÑ	IETERS	INCHES			
DIM	MIN	MAX	MIN	MAX		
Α	đ	2.05		0.081		
A <sub>1</sub>	0.05	0.20	0.002	0.008		
b	0.35	0.50	0.014	0.020		
C	0.18	0.27	0.007	0.011		
D	12.35	12.80	0.486	0.504		
Е	5.10	5.45	0.201	0.215		
e	1.27 BSC		0.050 BSC			
HE	7.40	8.20	0.291	0.323		
1	0.50	0.85	0.020	0.033		
LE	1.10	1.50	0.043	0.059		
M	0 °	10 °	0 °	10 °		
Q <sub>1</sub>	0.70	0.90	0.028	0.035		
Z		0.81		0.032		

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