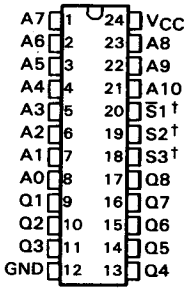
SEPTEMBER 1986—REVISED APRIL 1988

- **Organization . . . 2K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 2K × 8 Bipolar/High-Speed CMOS EPROMs and PROMs**
- **All Inputs/Outputs TTL Compatible**
- **High Speed**
- **Max Access/Min Cycle Time**

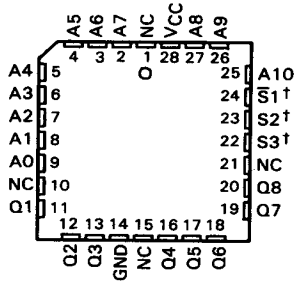
V_{CC} ± 5%		
'27C/PC291-3	'27C292-3	35 ns
'27C/PC291	'27C292	45 ns
'27C/PC291-5	'27C292-5	50 ns
V_{CC} ± 10%		
'27C/PC291-35	'27C292-35	35 ns
'27C/PC291-45	'27C292-45	45 ns
'27C/PC291-50	'27C292-50	50 ns

- **Low-Power CMOS Technology**
- **3-State Output Buffers**
- **Low Power Dissipation (V_{CC} = 5.25 V) — Active . . . 394 mW Max**
- **Erasable**
- **100% Pretestable**

J AND N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



†These pins have different pin assignments and functions in the program mode (see page 3).

description

The TMS27C291 and TMS27C292 series are 16,384-bit, ultraviolet-light erasable, electrically programmable read-only memories. The TMS27PC291 series are 16,384-bit, one-time, electrically programmable read-only memories. These devices are fabricated using CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external resistors. Each output can drive eight Series 74 TTL circuits without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The J and N dual-in-line packages are pin compatible with existing 24-pin bipolar PROMs and high speed EPROMs.

READ MODE

PIN NOMENCLATURE	
A0-A10	Address Inputs
GND	Ground
NC	No Connection
Q1-Q8	Outputs
$\overline{S}1$, S2, S3	Chip Selects
V_{CC}	5-V Power Supply

The TMS27C291 and TMS27C292 are offered in dual-in-line ceramic packages (J suffix). The TMS27C291 ceramic package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers. The TMS27C292 ceramic package is designed for insertion in mounting-hole rows on 15,24-mm (600-mil) centers.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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The TMS27PC291 PROM is offered in dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers. This version of the device is still in development, and the ADVANCE INFORMATION notices in this data sheet pertain to the N package devices. The TMS27PC291 PROM is also offered in a 28-lead plastic-leaded chip carrier (FN suffix) for surface mounting applications on solder lands on 1,27-mm (50-mil) centers.

All devices are guaranteed for operation from 0°C to 70°C.

operation

There are eight modes of operation for the TMS27C291, TMS27C292 and the TMS27PC291 as listed in the following table. The read mode requires a single 5-V supply. All inputs are TTL or CMOS levels except for V_{PP} during programming (13.5 V).

FUNCTION	MODE										
	Read	Output Disable#	Output Disable#	Output Disable#	Program Verify	Program Inhibit	Fast Program	Blank Check Ones	Blank Check Zeros	Signature	
$\overline{S1}/V_{PP}$†	V_{IL}	V_{IH}	X‡	X	V_{PP}	V_{PP}	V_{PP}	$V_{IL(P)}$¶	$V_{IL(P)}$	V_{IL}	
S2/$\overline{VFY}$†	V_{IH}	X	V_{IL}	X	$V_{IL(P)}$	$V_{IH(P)}$	$V_{IH(P)}$	$V_{IL(P)}$	$V_{IH(P)}$	V_{IH}	
S3/$\overline{PGM}$†	V_{IH}	X	X	V_{IL}	$V_{IH(P)}$	$V_{IH(P)}$	$V_{IL(P)}$	V_H§	V_H	V_H	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	X	X	X	V_{PP}	V_{PP}
A0	X	X	X	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8	D_{OUT}	HI-Z	HI-Z	HI-Z	D_{OUT}	HI-Z	D_{IN}	Ones	Zeros	CODE	
										MFG	DEV
										97	02

†Pin assignment for program mode.
‡X can be V_{IL} or V_{IH}.
§V_H = 12 V ± 0.5 V.
¶(P) = Programming mode.
#Output can be disabled using any of these three methods.

read/output disable

When the outputs of two or more of these devices are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a '27C291, '27PC291, or '27C292, a low-level signal is applied to $\overline{S1}$ and a high-level signal is applied to S2 and S3. Any other combination of logic states on these three inputs will disable the outputs. Output data is accessed at pins Q1 through Q8.

latchup immunity

Latchup immunity is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

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erasure (TMS27C291-_ _JL and TMS27C292-_ _JL)

Before programming, the '27C291 or '27C292 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is 25 watt-seconds per square centimeter. A typical 12 milliwatt-per-square-centimeter, filterless UV lamp will erase the device in 45 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the '27C291 or '27C292, the window should be covered with an opaque label.

programming mode pin functions

In the programming mode pins 18-20 on the dual-in-line packages or pins 22-24 on the plastic-leaded chip carrier no longer act as chip selects. Pin $\overline{S1}$ becomes the V_{PP} power supply, pin S2 becomes the $\overline{VFY}$ (verify) input, and pin S3 becomes the $\overline{PGM}$ (program) input in the programming mode. Programming mode pin assignments and nomenclature are given in the figures to the right.

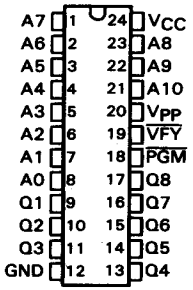
blank check mode

The '27C291 and '27C292 use a differential memory cell. This means that an unprogrammed device has ambiguous states in all address locations. Prior to programming, the blank check mode is used to verify that both sides of the differential cell are erased. The blank check mode is defined as S3 to V_H and $\overline{S1}$ to V_{IL}. In this mode, S2 selects between blank check 0s and 1s.

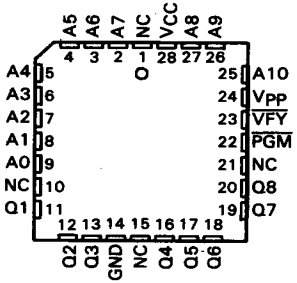
fast programming

Data is presented in parallel (eight bits) on pins Q1 through Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 13.5 V, V_{CC} = 5.0 V, $\overline{VFY}$ = V_{IH}, $\overline{PGM}$ = pulsed V_{IL}. More than one '27C291, '27C292, or '27PC291 can be programmed when the devices are connected in parallel. Locations can be programmed in any order, but it is recommended that all locations be programmed.

PROGRAMMING AND BLANK CHECK MODE PIN ASSIGNMENTS
J AND N PACKAGES
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



PROGRAM MODE

PIN NOMENCLATURE	
A0-A10	Address Inputs
GND	Ground
NC	No Connection
$\overline{PGM}$	Program Input
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
$\overline{VFY}$	Verify Input
V_{PP}	13.5-V Power Supply

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Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 0.1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied. If correct data is not read, an additional 0.1-millisecond pulse is applied up to a maximum X of 4. The Final programming pulse is 24X long. This sequence of programming and verification is performed at V_{CC} = 5.0 V and V_{PP} = 13.5 V. When the full Fast programming routine is complete, all bits are verified with V_{CC} = 5 V ± 10% (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high-level input on the $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 13.5 V when $\overline{VFY}$ = V_{IL} and $\overline{PGM}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0, i.e., A0 = V_{IL} accesses the manufacturer code; A0 = V_{IH} accesses device code. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for these devices is 97, and the device code is 02.

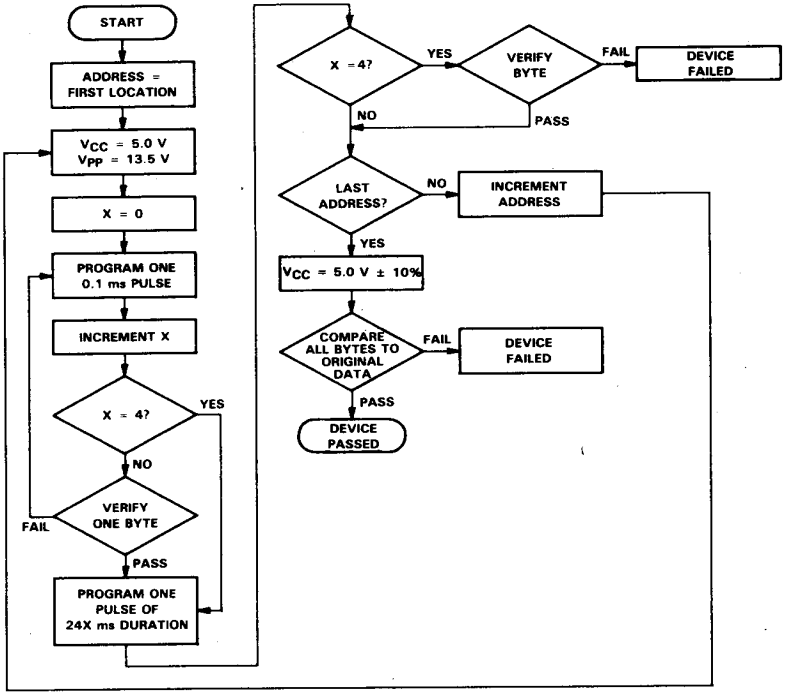

FIGURE 1. FAST PROGRAMMING FLOWCHART

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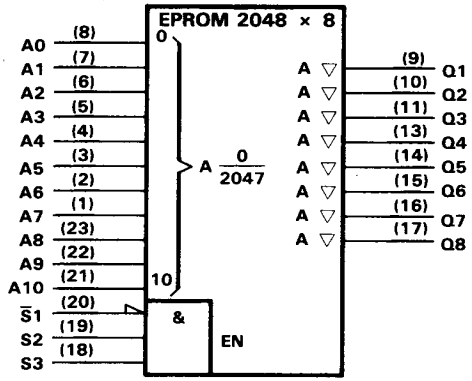
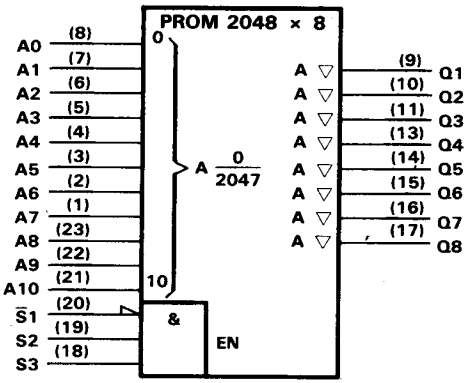
logic symbols†





†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} (programming mode) . . . . . −0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 and S3 . . . . . −0.6 V to 6.5 V
A9 and S3 . . . . . −0.6 V to 14 V
Output voltage range (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

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recommended operating conditions

			'27C291, '27PC291 '27C292 '27C291-3, '27PC291-3 '27C292-3 '27C291-5, '27PC291-5 '27C292-5			'27C291-35, '27PC291-35 '27C292-35 '27C291-45, '27PC291-45 '27C292-45 '27C291-50, '27PC291-50 '27C292-50			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+1$	$V_{CC}-0.2$		$V_{CC}+1$	
$V_{IH(P)}$	High-level input voltage (see Note 2)	Programming	3		$V_{CC}+1$	3		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	−0.5		GND+0.2	−0.5		GND+0.2	
$V_{IL(P)}$	Low-level input voltage (see Note 2)	Programming	−0.5		0.4	−0.5		0.4	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only. These are absolute voltages with respect to device ground pin and include all overshoot due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −4 mA		2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 16 mA				0.4	V
I_I	Input current (leakage)	All inputs except $\overline{S1}$	V_I = 0 V to 5.5 V			1	±10	μA
		$\overline{S1}$	$\overline{S1}$ = 0 V to 5.5 V				±10	
I_O	Output current (leakage)		V_O = 0 V to V_{CC}			1	±10	μA
I_{PP}	V_{PP} programming current		V_{PP} = 13.5 V				50	mA
I_{CC}	Supply current (see Note 3)	'27C291-3, '27PC291-3	V_{CC} = 5.25 V	t_c = dc		15	35	mA
		'27C292-3		t_c = min		40	75	
		'27C291-35, '27PC291-35	V_{CC} = 5.5 V	t_c = dc		15	35	mA
		'27C292-35		t_c = min		40	75	
		'27C291, '27PC291	V_{CC} = 5.25 V	t_c = dc		15	35	mA
		'27C292		t_c = min		35	60	
		'27C291-45, '27PC291-45	V_{CC} = 5.5 V	t_c = dc		15	35	mA
		'27C292-45		t_c = min		35	60	
		'27C291-5, '27PC291-5	V_{CC} = 5.25 V	t_c = dc		15	35	mA
		'27C292-5		t_c = min		30	55	
		'27C291-50, '27PC291-50	V_{CC} = 5.5 V	t_c = dc		15	35	mA
		'27C292-50		t_c = min		30	55	

†Typical I_{CC} is measured at V_{CC} = 5 V, T_A = 25°C and CMOS input levels.
NOTE 3: Assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, and addresses toggling between 0 V and 3 V

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	All inputs except $\overline{S1}$	V_I = 0 V, f = 1 MHz		8	10	pF
		$\overline{S1}$	V_I = 0 V, f = 1 MHz		16	20	pF
C_o	Output capacitance		V_O = 0 V, f = 1 MHz		12	15	pF

†Capacitance measurements are made on a sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Notes 3 and 4 and Figure 2)

PARAMETER		'27C291-3, '27PC291-3 '27C292-3 '27C291-35, '27PC291-35 '27C292-35		'27C291, '27PC291 '27C292 '27C291-45, '27PC291-45 '27C292-45		'27C291-5, '27PC291-5 '27C292-5 '27C291-50, '27PC291-50 '27C292-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		35		45		50	ns
$t_{en(S1)}$	Enable time from $\overline{S1}$		25		35		35	ns
$t_{en(S2)}$	Enable time from S2		25		35		35	ns
$t_{en(S3)}$	Enable time from S3		25		35		35	ns
t_{dis}	Disable time from $\overline{S1}$, S2, S3	0	25	0	35	0	35	ns
$t_{v(A)}$	Output valid time	0		0		0		ns

NOTES: 3. Assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, and addresses toggling between 0 V to 3 V.
4. Minimum cycle time is equal to maximum access time.

recommended timing requirements for programming

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.1		0.4	ms
$t_{w(FPGM)}$	Final program pulse duration	2.4		9.6	ms
$t_{su(A)}$	Address setup time	1			μs
$t_{su(VPP)}$	V_{PP} setup time	1			μs
$t_{su(VFY)}$	$\overline{VFY}$ setup time	1			μs
$t_{dis(VFY)}$	Output disable time from $\overline{VFY}$	0		35	ns
$t_{en(VFY)}$	Output enable time from $\overline{VFY}$			35	ns
$t_{su(D)}$	Data setup time	1			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	1			μs

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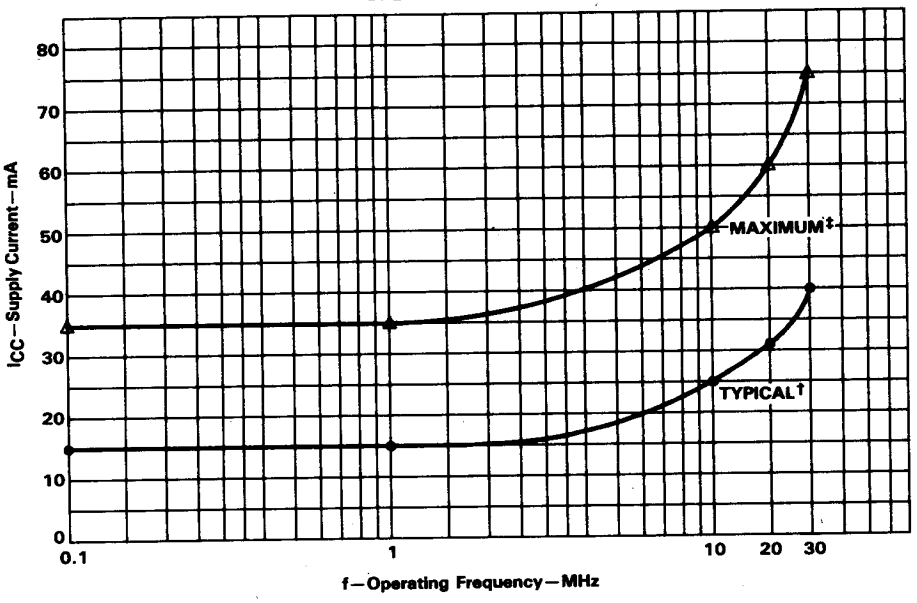
supply current vs operating frequency

PARAMETER		TEST CONDITIONS	TYP†	MAX‡	UNIT
I_{CC}	Supply current	0 Hz ≤ f ≤ 1 MHz	15	35	mA
		f = 10 MHz	25	50	mA
		f = 20 MHz	32	60	mA
		f = 30 MHz	40	75	mA

SUPPLY CURRENT
vs
OPERATING FREQUENCY



†Typical I_{CC} is measured at V_{CC} = 5 V, T_A = 25°C and CMOS inputs levels.
‡Maximum I_{CC} is measured at V_{CC} = 5.5 V, T_A = 0°C and CMOS input levels.

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PARAMETER MEASUREMENT INFORMATION

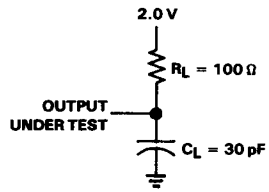
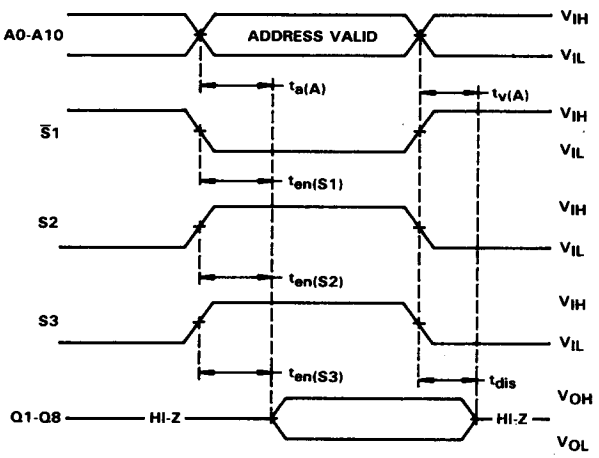


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



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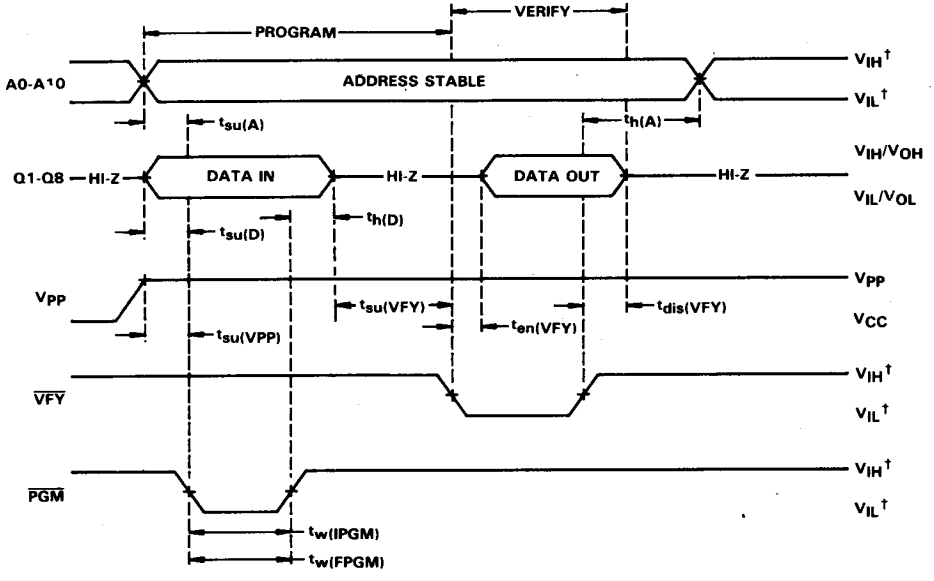
program cycle timing



†Programming levels for V_{IH} and V_{IL}.

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