SCAN926260 Six 1 to 10 Bus LVDS Deserializers with IEEE 1149.1 and At-Speed BIST

Check for Samples: SCAN926260

FEATURES

- **Deserializes One to Six Bus LVDS Input Serial Data Streams with Embedded Clocks**
- **IEEE 1149.1 (JTAG) Compliant and At-Speed BIST Test Modes**
- **Parallel Clock Rate 16-66MHz**
- **On Chip Filtering for PLL**
- **High Impedance Inputs Upon Power Off (V_{cc} = 0V)**
- **Single Power Supply at +3.3V**
- **196-Pin NFBGA Package (Low-Profile Ball Grid Array) Package**
- **Industrial Temperature Range Operation: −40°C to +85°C**
- **ROUTn[0:9] and RCLKn Default High when Channel is Not Locked**
- **Powerdown Per Channel to Conserve Power on Unused Channels**

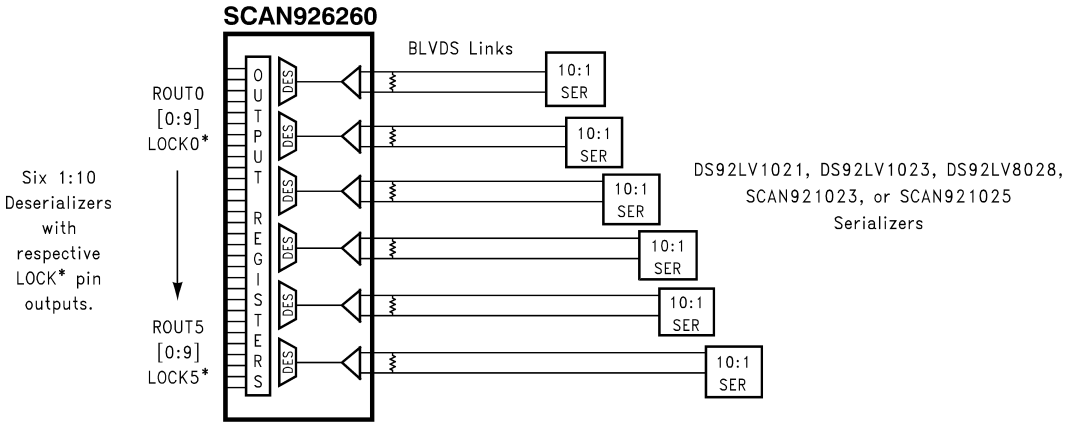
DESCRIPTION

The SCAN926260 integrates six 10-bit deserializer devices into a single chip. The SCAN926260 can simultaneously deserialize up to six data streams that have been serialized by TI's 10-bit Bus LVDS serializers. In addition, the SCAN926260 is compliant with IEEE standard 1149.1 and also features an At-Speed Built-In Self Test (BIST). For more details, please see the sections titled IEEE 1149.1 Test Modes and BIST Alone Test Modes.

Each deserializer block in the SCAN926260 has it's own powerdown pin ($\overline{\text{PWRDWN[n]}}$)and operates independently with its own clock recovery circuitry and lock-detect signaling. In addition, a master powerdown pin ($\overline{\text{MS\_PWRDWN}}$) which puts all the entire device into sleep mode is provided.

The SCAN926260 uses a single +3.3V power supply and consumes 1.2W at 3.3V with a PRBS-15 pattern on all channels at 660Mbps.

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{DD})		-0.3 to 3.8V
BLVDS Input Voltage (Rin ±)		-0.3V to +3.9V
Maximum Package Power Dissipation Capacity @ 25°C		3.7W
Package Thermal Resistance	θ_{JA} 196 NFBGA:	34°C/W
	θ_{JC} 196 NFBGA:	8°C/W
Storage Temp. Range		-65°C to +150°C
Junction Temperature		+125°C
Lead Temperature (Soldering 10 Seconds)		+225°C
ESD Ratings	Human Body Model	>2KV
	Machine Model	>250V

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

Supply Voltage (V_{DD})	3.0V to 3.6V
Operating Free Air Temperature (T_A)	-40°C to +85°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVCMOS/LVTTL DC Specifications							
V_{IH}	High Level Input Voltage		REN, REFCLK, $\overline{\text{PWRDWNn}}$, MS_PWRDWN	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage				-0.87	-1.5	V
I_{IN}	Input Current	V_{in} = 0 or 3.6V		-10		+10	uA
I_{IN}	Input Current	V_{in} = 0 or 3.6V	$\overline{\text{TRST}}$, TMS, TDI, BIST_SEL[0:2]	-20		+20	uA
V_{OH}	High Level Output Voltage	I_{OH} = −6mA	ROUT, $\overline{\text{RCLK}}$, $\overline{\text{LOCKn}}$	2	3	V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 6mA		GND	0.18	0.5	V
I_{OS}	Output short Circuit Current	V_{out} = 0V		-15	-46	-85	mA
I_{OZ}	Tri-state Output Current	$\overline{\text{MS\_PWRDWN}}$ or REN = 0.8V V_{out} = 0V or V_{CC}		-10	±0.2	+10	µA
V_{OH}	High Level Output Voltage	I_{OH} = −12mA	TDO	2		V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 12mA		GND		0.5	V
I_{OS}	Tri-state Output Current	V_{out} = 0V		-15		-120	mA

(1) Typical values are given for VDD = 3.3V and TA =25°C

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
Bus LVDS DC specifications							
V_{TH}	Differential Threshold High Voltage	VCM = 0.025, 1.250, 2.375V (V_{RI+}-V_{RI-})	RI+, RI-		+3	+50	mV
V_{TL}	Differential Threshold Low Voltage			-50mV	-2		mV
I_{IN}	Input Current	V_{in} = +2.4V, V_{cc} = 3.6 or 0V		-10	±1	+10	µA
		V_{in} =0V, V_{cc} = 3.6 or 0V		-10	±1	+10	µA
Supply Current							
I_{CCR}	Total Supply Current	Checker Board Pattern, C_L=15pF	66 MHz		500	600	mA
		PRBS-15 Pattern, C_L=15pF	66 MHz		385		mA
ΔI_{CCR}	Reduction in Supply Current per Channel	Checker Board Pattern	66 MHz	55	77	100	mA
I_{CCXR}	Total Supply Current when Powered Down	$\overline{MS\_PWRDN}$= 0.8V(2)			1.5	2.2	mA
Timing Requirements for REFCLK							
t_{RFCP}	REFCLK Period			15.15		62.5	ns
t_{RFDC}	REFCLK Duty Cycle			30	50	70	%
t_{RFCP}/t_{TCP}	Ratio of REFCLK to TCLK			0.95		1.05	
t_{RFTT}	REFCLK Transition Time					8	ns
Deserializer Switching Characteristics							
t_{RCP}	RCLK Period		RCLK	15.15		62.5	ns
t_{RDC}	RCLK Duty Cycle	See(3)		41	50	55	%
t_{CLH}	LVCMOS/LVTTL Low-to-High Transition Time	C_L = 15pF, Figure 3(4)	$\overline{LOCK}$, RCLK, ROUT	1.3	1.8	2.2	ns
t_{CHL}	LVCMOS/LVTTL High-to-Low Transition Time			1.0	1.5	2.0	ns
t_{ROS}	Rout Data Valid before RCLK	See Figure 2		0.4*t_{RCP}			ns
t_{ROH}	Rout Data Valid after RCLK	See Figure 2		-0.4*t_{RCP}			ns
t_{HZR}	High to Tri-state Delay	See Figure 7				10	ns
t_{LZR}	Low to Tri-state Delay					10	ns
t_{ZHR}	Tri-state to High Delay					12	ns
t_{ZLR}	Tri-state to Low Delay					12	ns
t_{DD}	Deserializer Delay	See Figure 1 (All Cases)	RCLK	1.75*t_{RCP}+5	1.75*t_{RCP}+7	1.75*t_{RCP}+10	ns
		66 MHz Only		1.75*t_{RCP}+6	1.75*t_{RCP}+7	1.75*t_{RCP}+9	ns

(2) Total Supply Current when Powered Down (I_{CCXR}) is higher than previous six channel devices because previous devices asserted ROUTn and RCLKn into tri-state upon loss-of-lock, whereas the SCAN926260 now asserts ROUTn and RCLKn HIGH upon loss-of-lock.
(3) t_{RDC} was specified by measuring the positive pulse on the RCLK and dividing this number by the ideal pulse width.
(4) t_{CLH} and t_{CHL} are Ensured by Statistical Analysis (EBSA). Please see Figure 3 for a graphical representation.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{DSR1}	Deserializer PLL LOCK Time from PWRDNn (with SYNCPAT)	See Figure 4(5)	66MHz			2.5	µs
			16MHz			7.0	µs
t_{DSR2}	Deserializer PLL Lock Time from SYNCPAT	See Figure 5(5)	66MHz			1.1	µs
			16MHz			4.5	µs
$t_{RNMI-RIGHT}$	Deserializer Right Noise Margin	See Figure 8(6)	66MHz	400	500		ps
			16MHz	1.3	2.51		ns
$t_{RNMI-LEFT}$	Deserializer Left Noise Margin		66MHz	440	600		ps
			16MHz	1.4	2.59		ns

(5) For the purpose of specifying deserializer PLL performance, t_{DSR1} and t_{DSR2} are specified with the REFCLK running and stable, and specific conditions of the incoming data stream (SYNCPATs). t_{DSR1} is the time required for the deserializer to indicate lock upon power-up or when leaving the power-down mode. t_{DSR2} is the time required to indicate lock for the powered-up and enabled deserializer when the input (RI+ and RI−) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs). The time to lock to random data is dependent upon the incoming data and is not specified.

(6) $t_{RNMI-LEFT}$ and $t_{RNMI-RIGHT}$ are a measure of how much phase noise (jitter) the deserializer can tolerate in the incoming data stream before bit errors occur. The Deserializer noise margin specification does not include transmitter jitter and is Ensured By Statistical Analysis (EBSA). Please see Figure 8 for a graphical representation.

SCAN Circuitry Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Maximum TCK Clock Frequency	R_L = 500Ω, C_L = 35 pF	25.0	50.0		MHz
t_S	TDI to TCK, H or L		2.0			ns
t_H	TDI to TCK, H or L		1.0			ns
t_S	TMS to TCK, H or L		2.5			ns
t_H	TMS to TCK, H or L		1.0			ns
t_W	TCK Pulse Width, H or L		10.0			ns
t_W	$\overline{TRST}$ Pulse Width, L		2.5			ns
t_{REC}	Recovery Time, $\overline{TRST}$ to TCK		2.0			ns

Timing Diagrams

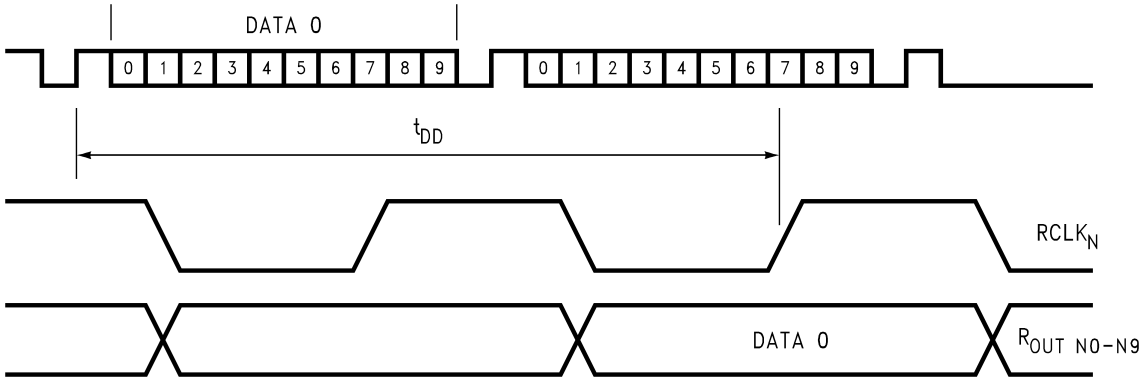


Figure 1. Deserializer Delay t_{DD}

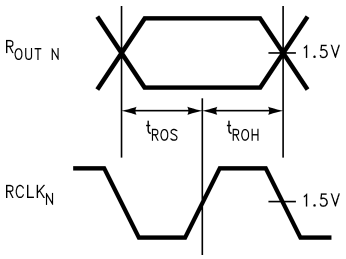


Figure 2. Output Timing t_{ROS} and t_{ROH} (Data Valid)

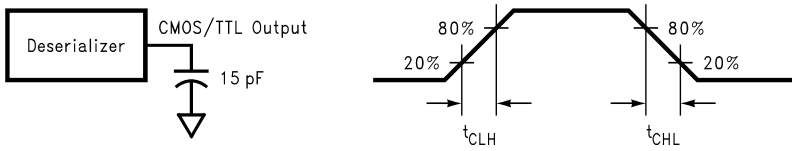


Figure 3. Deserializer CMOS/LVTTL Output Load and Transition Times

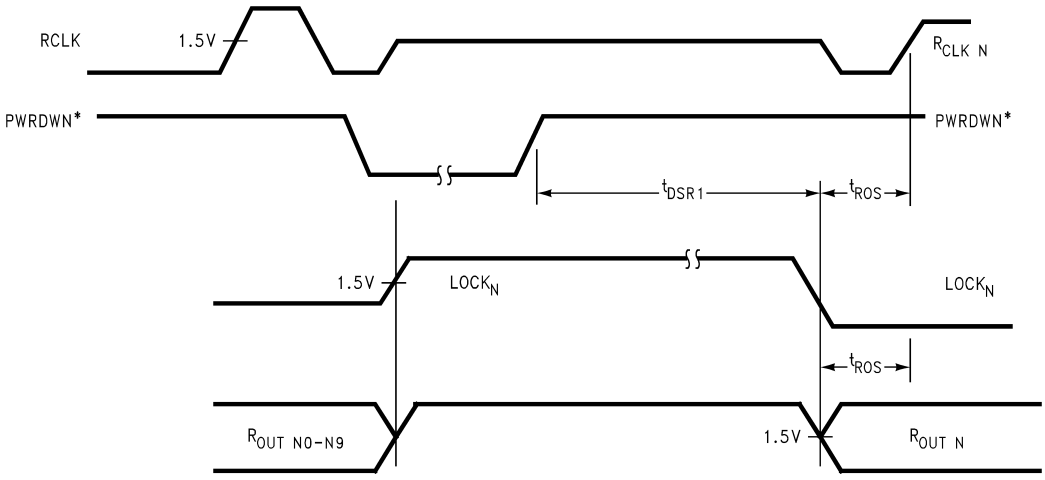


Figure 4. Locktime from $\overline{\text{PWRDN}}$n t_{DSR1}

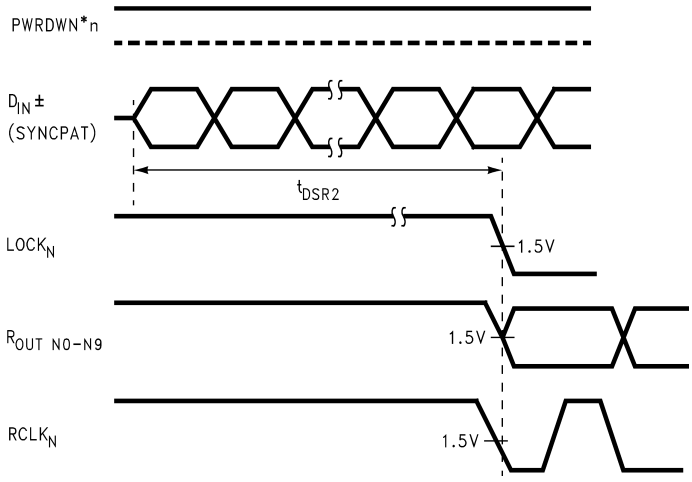


Figure 5. Locktime to SYNCPAT t_{DSR2}

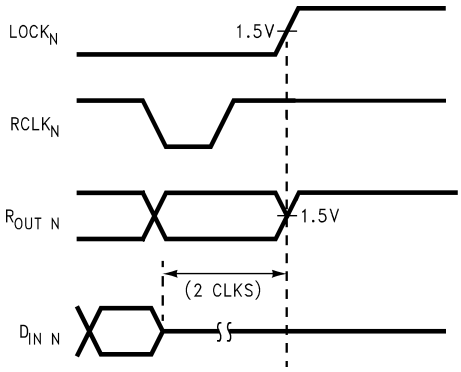


Figure 6. Loss of Lock

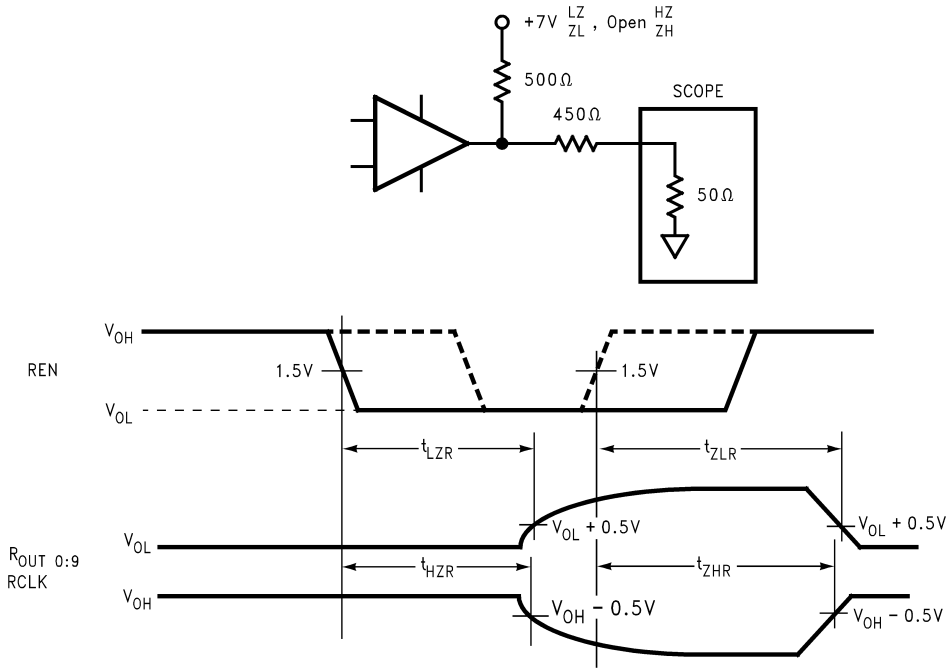
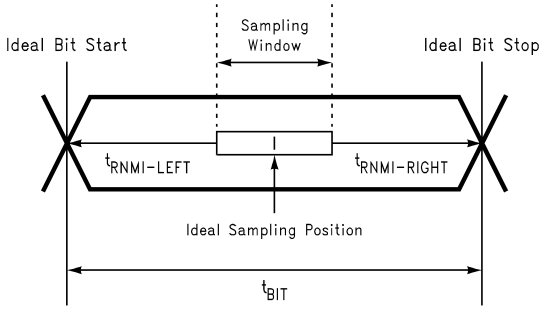


Figure 7. Deserializer Tri-state Test Circuit and Timing

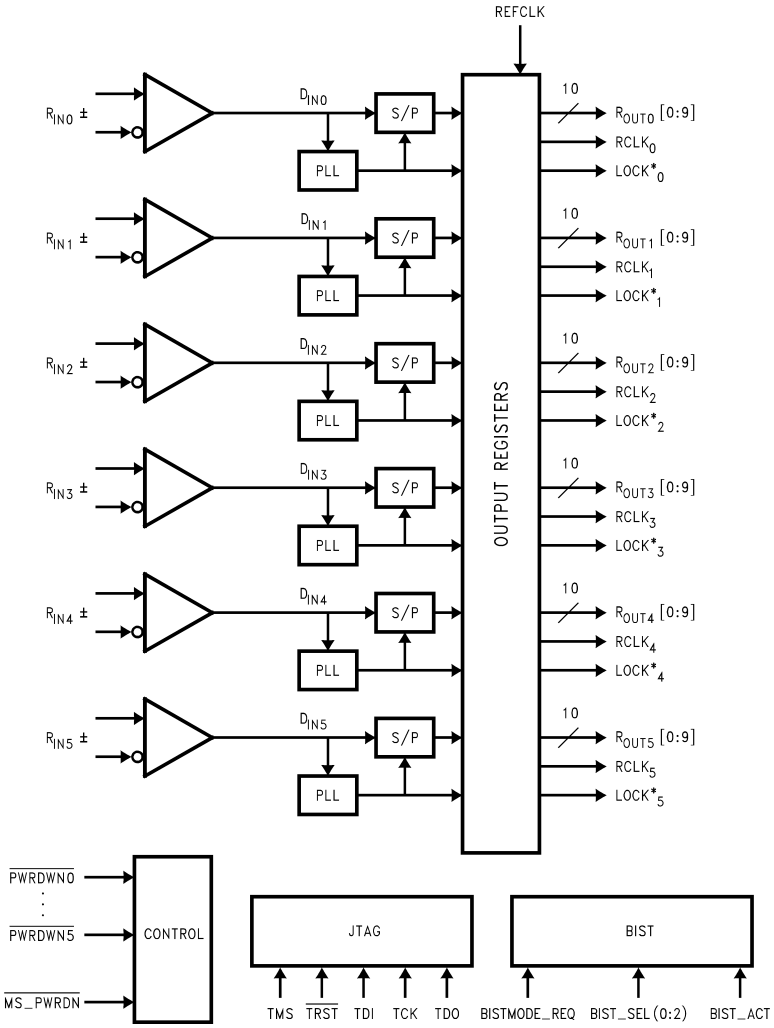


$$\text{Ideal Sampling Position} = \frac{(t_{BIT})}{2}$$

Note: For an explanation of Ideal Crossing Point and Noise Margin, please see the Application Information section.

Figure 8. Deserializer Noise Margin and Sampling Window

Block Diagram



Functional Description

The SCAN926260 combines six 1:10 deserializers into a single chip. Each of the six deserializers accepts a Bus LVDS data stream from TI's DS92LV1021, DS92LV1023, DS92LV8028, SCAN921023, or SCAN921025 Serializer. The deserializers then recover the clock and data to deliver the resulting 10-bit wide words to the outputs.

Each of the six channels acts completely independent of each other. Each independent channel has outputs for a 10-bit wide data word, a recovered clock output, and a lock-detect output.

The SCAN926260 has three operating states: Initialization, Data Transfer, and Resynchronization. In addition, there are two passive states: Powerdown and Tri-state. During normal operation, the SCAN6260 also has the capability of utilizing the IEEE 1149.1 test modes (JTAG) or the Built-In Self Test mode (BIST).

The following sections describe each operating mode, passive states, and the JTAG and BIST modes.

Initialization

Before the SCAN926260 receives and deserializes data, it and the transmitting Serializer must initialize the link. Initialization refers to synchronizing the Serializer's and the Deserializer's PLL's to local clocks. The local clocks must be within ±5% of the incoming transmitter clock frequency. After all devices synchronize to local clocks, the Deserializer synchronizes to the Serializer as the second and final initialization step.

Step 1: After applying power to the Deserializer, the outputs are held high and the on-chip Power-on Reset (POR) circuitry disables the internal circuits. When V_{cc} reaches V_{cc}OK (2.1V), the PLL in each deserializer begins locking to the local clock (REFCLK). A local on-board oscillator or other source that provides the specified clock input to the REFCLK pin.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete the initialization. Refer to the Serializer data sheet for proper operation during the Initialization State. The Deserializer identifies the rising clock edge in a synchronization pattern or pseudo-random data and after 80 clock cycles will synchronize to the data stream from the Serializer. At the point where the Deserializer's PLL locks to the embedded clock, the LOCKn pin goes low and valid data appears at the outputs.

Data Transfer

After initialization, the Serializer transfers data to the Deserializer. The serial data stream includes a start and stop bit appended by the serializer, which frames the ten data bits. The start bit is always high and the stop bit is always low. The start and stop bits also function as clock bits embedded in the serial stream.

The Serializer transmits the data and clock bits (10+2 bits) at 12 times the TCLK frequency. For example, if TCLK is 40 MHz, the serial rate is 40 X 12 = 480 Mbps. Since only 10 bits are from input data, the serial 'payload' rate is 10 times the TCLK frequency. For instance, if TCLK = 40 MHz, the payload data is 40 X 10 = 400 Mbps. TCLK is provided by the data source and must be in the range of 16MHz to 66MHz.

When one of six Deserializer channels synchronizes to the input from a Serializer, it drives its $\overline{\text{LOCKn}}$ pin low and synchronously delivers valid data at its outputs. The Deserializer locks to the embedded clock, uses it to generate multiple internal data strobes, and drives the embedded clock to the RCLKn pin. The RCLKn pin is synchronous to the data on the ROUTn[0:9] pins. While $\overline{\text{LOCKn}}$ is low, data on ROUTn[0:9] is valid. Otherwise, ROUTn[0:9] and RCLKn are high.

All ROUT, $\overline{\text{LOCK}}$, and RCLK signals will drive a minimum of three CMOS input gates (15pF load) with a 66 MHz clock. This amount of drive allows bussing outputs of two Deserializers and a destination ASIC. REN controls tri-state of all the outputs.

The Deserializer input pins are high impedance during Powerdown ($\overline{\text{PWRDNn}}$ or $\overline{\text{MS\_PWRDN}}$ low) and power-off (V_{cc} = 0V).

Resynchronization

Whenever one of the six Deserializers loses lock, it will automatically try to resynchronize. For example, if the embedded clock edge is not detected two times in succession, the PLL loses lock and the $\overline{\text{LOCKn}}$ pin is driven high. The system must monitor the $\overline{\text{LOCKn}}$ pin to determine when data is valid.

The user has the choice of allowing the deserializer to re-sync to the data stream or to force synchronization by asserting the Serializer SYNC1 or SYNC2 pin high. This scheme is left up to user discretion. One recommendation is to provide a feedback loop using the LOCKn pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are provided for local or remote control..

Powerdown

The Powerdown state is a low power sleep mode that the Deserializer typically occupies while waiting for initialization or to reduce power consumption when no data is transferred. While in Powerdown Mode, the PLL stops and RCLK and ROUTn[0:9] are high, which reduces the supply current for each channel by approximately 80mA. Each channel has a powerdown (PWRDWNn) pin that puts the respective channel into sleep mode when asserted low. In addition, the SCAN926260 has a master powerdown (MS_PWRDWN) pin that overrides each individual powerdown pin and puts the entire device into sleep mode when asserted low (This same condition can be replicated by asserting all six individual powerdown pins low.). The powerdown pins are internally pulled low which defaults the device into sleep mode. Active operation requires asserting a high on MS_PWRDWN and the selected channel's PWRDWNn pin.

Upon exiting Powerdown, the Deserializer enters the Initialization state. The system must then allow time to Initialize before data transfer can begin.

Tri-state

When the system drives the REN pin low, the Deserializer enters tri-state. This will tri-state the receiver output pins (ROUTn[0:9]) and RCLK[0:5]. When the system drives REN high, the Deserializer will return to the previous state as long as all other control pins remain static (PWRDWNn, MS_PWRDWN). The LOCKn pin is not affected by REN and continues to be active, signalling LOCK status. This allows the system to be sure the channel is locked before enabling the data outputs.

SCAN926260 Control Signal Truth Table(1)

	SCAN Mode Internal Signals		INPUTS			OUTPUTS		
STATE	**SCAN_HIZB**	**SCAN_BIST**	**MS_PWRDWN**	**PWRDWN[n]**	**REN**	**LOCK[n]**	**ROUTn[0:9]**	**RCLK[n]**
SCAN(2)	0	X	X	X	X	Z	10 @ Z	Z
SCAN(2)	1	1	X	X	X	Z	10 @ Z	Z
Powerdown(3)	1	0	0	X	X	1	10 @ 1	1
Powerdown(4)	1	0	1	All 6 @ 0	X	1	10 @ 1	1
Normal, Not Locked(5)	1	0	1	1	1	1	10 @ 1	1
Normal, Locked(5)	1	0	1	1	1	0	data	clock
REN = Low, Not Locked (6)(7)	1	0	1	1	0	1	10 @ Z	Z

(1) **Key:**
Z = High Impedance
X = Don't Care
10 @ Z = All 10 ROUT for the respective Channel are High Impedance
1 = High Voltage Level
0 = Low Voltage Level
SCAN_HIZB = the internal control signal from the HighZ command at the TAP Controller
SCAN_BIST = the internal control signal from the BIST command at the TAP Controller

(2) JTAG/SCAN has the highest priority. SCAN_HIZB is active low and SCAN_BIST is active high. If either control is active, the outputs will be in tri-state.

(3) MS_PWRDWN has the second highest priority. When MS_PWRDWN is low, the entire chip enters sleep mode and all outputs (ROUTn[0:9], RCLK[n], and LOCK[n]) are high.

(4) PWRDWN[n] are the six individual power-down pins. Each will power down the respective channel. A special case occurs when all six PWRDWN[n] pins are low-the common bias circuits will also be powered down. This state is equivalent to the case when MS_PWRDWN is low.

(5) During normal operation mode (no SCAN, no Power-down, and REN high), LOCK[n] controls the ROUTn[0:9] and RCLK[n] outputs. When LOCK[n] is high (unlocked), all outputs will be 1, and when LOCK[n] is low (locked), both data and clock will be valid at the outputs. BIST-ALONE mode is considered part of normal operation and can be overriden by any of the above priorities.

(6) REN has a lower priority than PWRDWN[n]. When REN is low, the output data (ROUTn[0:9] and RCLK[n]) will be in tri-state. The LOCK[n] signal's output is not affected by REN.

(7) There are internal pull-downs on the REN, PWRDWNn and MS_PWRDWN pins. Active operation requires asserting these pins high.

SCAN926260 Control Signal Truth Table[1] (continued)

	SCAN Mode Internal Signals		INPUTS			OUTPUTS		
STATE	$\overline{\text{SCAN\_HIZB}}$	SCAN_BIST	$\overline{\text{MS\_PWRDWN}}$	$\overline{\text{PWRDWN[n]}}$	REN	$\overline{\text{LOCK[n]}}$	ROUTn[0:9]	RCLK[n]
REN = Low, Locked[6][7]	1	0	1	1	0	0	10 @ Z	Z
Default State[7]			0	0	0	1	10 @ 1	1

IEEE 1149.1 Test Modes

The SCAN926260 features interconnect test access that is compliant to the IEEE 1149.1 Standard for Boundary Scan Test (JTAG). All digital TTL I/O's on the device are accessible using IEEE 1149.1, and entering this test mode will override all input control cases including power down and REN. In addition to the four required Test Access Port (TAP) signals of TMS, TCK, TDI, and TDO, $\overline{\text{TRST}}$ is provided for test reset.

To supplement the test coverage provided by the IEEE 1149.1 test access to the digital TTL pins, the SCAN926260 has two instructions to test the LVDS interconnects. The first is EXTEST. This is implemented at LVDS levels and is only intended as a go no-go test (e.g. missing cables). The second method is the RUNBIST instruction. It is an "at-system-speed" interconnect test. It is executed in approximately 33ms with a system clock speed of 66MHz. There are 12 bits in the RX BIST data register for notification of PASS/FAIL and TEST_COMPLETE, with two bits for each of the six channels. The RX BIST register is defined as (from MSB to LSB):

Table 1. RX BIST Register

Bit Number	Description
11 (MSB)	BIST COMPLETE for Channel 6
10	BIST PASS/FAIL for Channel 6
9	BIST COMPLETE for Channel 5
8	BIST PASS/FAIL for Channel 5
7	BIST COMPLETE for Channel 4
6	BIST PASS/FAIL for Channel 4
5	BIST COMPLETE for Channel 3
4	BIST PASS/FAIL for Channel 3
3	BIST COMPLETE for Channel 2
2	BIST PASS/FAIL for Channel 2
1	BIST COMPLETE for Channel 1
0 (LSB)	BIST PASS/FAIL for Channel 1

A "pass" indicates that the BER (Bit-Error-Rate) is better than 10^{-7}. This is a minimum test, so a "fail" indication means that the BER is higher than 10^{-7}.

The BIST features of the SCAN926260 six channel deserializer are compatible with the BIST features on the DS92LV8028, the SCAN921023 and the SCAN921025 Serializers.

An important detail is that once both devices have the RUNBIST instruction loaded into their respective instruction registers, both devices must move into the RTI state within 4K system clocks (At a system CLK of 66MHz and TCK of 1MHz this allows for 66 TCK cycles). This is not a concern when both devices are on the same scan chain or LSP. However, it can be a problem with some multi-drop devices. This test mode has been simulated and verified using TI's Enhanced SCAN Bridge (SCANSTA111).

BIST Alone Test Modes

The SCAN926260 also supports a BIST Alone feature which can be run without enabling the JTAG TAP controller. This feature provides the ability to run continuous BER testing on all channels, or on individual channels without affecting live traffic on other channels. The ability to run the BERT (Bit-Error-Rate-Test) while adjacent channels are carrying normal traffic is a useful tool to determine how normal traffic will affect the BER on any given channel.

The BIST Alone features can be accessed using the 5 pins defined as BIST_SEL0, BIST_SEL1, BIST_SEL2, BIST_ACT, and BISTMODE_REQ.

BIST_ACT activates the BIST Alone mode. The BIST Alone mode will continue until deactivated by the BIST_ACT pin. The BIST_ACT input must be high or low for four or more clock cycles in order to activate or deactivate the BIST Alone mode. The BIST_ACT input is pulled low internally.

BISTMODE_REQ is used to select either gross error reporting or a specific output error report. When the BIST Alone mode is active, the $\overline{\text{LOCK}}$n output for all channels running BIST Alone will go low and the respective ROUTn(0:9) output will report any errors. When BISTMODE_REQ is low, the error reporting is set to Gross Mode, and whenever a bit contains one or more errors, ROUT(0:9) for that channel goes high and stays high until deactivation by the BIST_ACT input. When BISTMODE_REQ is high, the output error reporting is set to Bit Error mode. Whenever any data bit contains an error, the data output for that corresponding bit goes high. The default setting is Gross Error mode.

The three BIST_SELn inputs determine which channel is in BIST Alone mode according to the following table:

Table 2. BIST Alone Mode Selection

BIST_ACT	BIST_SEL2	BIST_SEL1	BIST_SEL0	BIST for Channel
1	0	0	0	0
1	0	0	1	1
1	0	1	0	2
1	0	1	1	3
1	1	0	0	4
1	1	0	1	5
1	1	1	0	All Channels
1	1	1	1	IDLE
0	X	X	X	IDLE

APPLICATION INFORMATION

USING THE SCAN926260

The SCAN926260 combines six 1:10 deserializers into a single chip. Each of the six deserializers accepts a BusLVDS data stream up to 660 Mbps from one of TI's 10-Bit Serializers. The Deserializers then recover the embedded two clock bits and data to deliver the resulting 10-bit wide words to the output. The Deserializer uses a separate reference clock (REFCLK) and an on-board PLL to extract the clock information from the incoming data stream and then deserialize the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the $\overline{\text{LOCK}}$n output high when loss of lock occurs.

POWER CONSIDERATIONS

An all CMOS design of the Deserializer makes it an inherently low power device.

POWERING UP THE DESERIALIZER

The SCAN926260 can be powered up at any time. The REFCLK input can be running before the Deserializer powers up, and it must be running in order for the Deserializer to lock to incoming data. The Deserializer outputs (ROUTn[0:9]), the recovered clock (RCLKn), and $\overline{\text{LOCK}}$n are high until the Deserializer detects data transmission at its inputs and locks to the incoming data stream.

DATA TRANSFER

Once the Deserializer powers up, it must be phase locked to the transmitter to transfer data. Phase locking occurs when the Deserializer locks to incoming data or when the Serializer sends sync patterns. The Serializer sends SYNC patterns whenever the SYNC1 or SYNC2 inputs are high. The $\overline{\text{LOCK}}$n output of the Deserializer remains high until it has locked to the incoming data stream. Connecting the $\overline{\text{LOCK}}$n output of the Deserializer to one of the SYNC inputs of the Serializer will ensure that enough SYNC patterns are sent to achieve Deserializer lock.

The Deserializer can also lock to incoming data by simply powering up the device and allowing the “lock to pseudo random data” circuitry to find and lock to the data stream.

While the Deserializer $\overline{\text{LOCKn}}$ output is low, data at the respective channel’s Deserializer outputs (ROUTn[0:9]) is valid, except for the specific case when loss of lock occurs during transmission which is further discussed in the RECOVERING FROM LOCK LOSS section below.

NOISE MARGIN

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably receive data. Various environmental and systematic factors include:

Serializer: TCLK jitter, V_{DD} noise (noise bandwidth and out-of-band noise)

Media: ISI, Large V_{CM} shifts

Deserializer: V_{DD} noise

Please see the section on USING NOISE MARGIN TO VALIDATE SIGNAL QUALITY for more information.

RECOVERING FROM LOCK LOSS

In the case where the Deserializer loses lock during data transmission, up to 1 cycle of data that was previously received can be invalid. This is due to the delay in the lock detection circuit. The lock detect circuit requires that invalid clock information be received two times in a row to indicate loss of lock. Since clock information has been lost, it is possible that data was also lost during these cycles. Therefore, after the Deserializer relocks to the incoming data stream and the Deserializer $\overline{\text{LOCKn}}$ pin goes low, at least one previous data cycle should be suspect for bit errors.

The Deserializer can relock to the incoming data stream by making the Serializer resend SYNC patterns, as described above, or by locking to pseudo random data, which can take more time, depending on the data patterns being received.

HOT INSERTION

All Bus LVDS Deserializers are hot pluggable if you follow a few rules. When inserting, ensure the Ground pin(s) makes contact first, then the VCC pin(s), and then the I/O pins. When removing, the I/O pins should be unplugged first, then the VCC, then the Ground. Random lock hot insertion is illustrated in Figure 9.

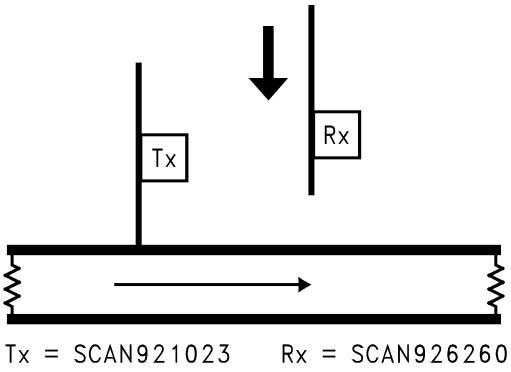


Figure 9. Hot Insertion Lock to Pseudo-Random Data

TRANSMISSION MEDIA

The Serializer and Deserializer can also be used in point-to-point configurations, through PCB trace, through twisted pair cable, or twinax cables. In point-to-point configurations, the transmission media need only be terminated at the receiver end. Please note that in point-to-point configurations, the potential of offsetting the ground levels of the Serializer vs. the Deserializer must be considered. In some applications, multidrop configurations may be possible. Bus LVDS provides a ±1.0V common mode range at the receiver inputs.

FAILSAFE BIASING FOR THE SCAN926260

The SCAN926260 has internal failsafe biasing and an improved input threshold sensitivity of ±50mV versus ±100mV for the DS92LV1210.. This allows for a greater differential noise margin. However, in cases where the receiver input is not being actively driven, the increased sensitivity of the SCAN926260 can pickup noise as a signal and cause unintentional locking. For example, this can occur when an input cable is disconnected.

External resistors can be added to the receiver circuit board to boost the level of failsafe biasing. Typically, the non-inverting receiver input is pulled up and the inverting receiver input is pulled down by high value resistors. The pull-up and pull-down resistors (R_1 and R_2) provide a current path through the termination resistor (R_L) which biases the receiver inputs when they are not connected to an active driver. The value of the pull-up and pull-down resistors should be chosen so that enough current is drawn to provide a +15mV minimum drop across the termination resistor in the presence of anticipated input noise. Also, in systems where use of the individual channel is well known or controlled, using the respective channel's PWRDWNn pin(s) may eliminate the need for external Failsafe Biasing. Please see Figure 11 for the Failsafe Biasing Setup.

DIFFERENCES BETWEEN the DS92LV1260, the SCAN921260, and the SCAN926260

The DS92LV1260 is a six channel, ten bit, Bus LVDS Deserializer with random lock capability and a parallel clock rate up to 40MHz. Each channel contains a recovered clock (RCLKn) and lock (LOCKn) output. The DS92LV1260 also contains a seventh serial input channel that serves as a redundant input. Also, unlike previous deserializers, the LOCKn signal is synchronous to valid data appearing on the outputs. Please see the DS92LV1260 datasheet for more specific details about the seventh redundant channel and further details.

The SCAN921260 contains the same basic functions as the DS92LV1260. However, the SCAN921260 has an increased parallel clock rate up to 66MHz, is IEEE 1149.1 (JTAG) compliant and also contains at-speed Built-In-Self-Test (BIST).

The SCAN926260 contains the same basic functions as the SCAN921260. However, in addition to a master powerdown, the SCAN926260 has individual powerdown pins per channel, has eliminated the seventh redundant channel, and now asserts all outputs ROUTn[0:9] and RCLKn high during powerdown and during loss of lock. Please also note that the LOCKn pin output is no longer affected by REN. Also, the SCAN926260 is footprint compatible and may be used interchangibly with the SCAN921260.

USING NOISE MARGIN TO VALIDATE SIGNAL QUALITY

The parameters $t_{RNMI-LEFT}$ and $t_{RNMI-RIGHT}$ are calculated by first measuring how much of the ideal bit the receiver needs to ensure correct sampling. After determining this amount, what remains of the ideal bit that is available for external sources of noise is called noise margin. Noise margin does not include transmitter jitter. Please see Figure 8 for a graphical explanation. Also, for a more detailed explanation of noise margin, please see Application Note 1217 (SNLA053) titled "How to Validate BLVDS SER/DES Signal Integrity Using an Eye Mask."

The vertical limits of the mask are determined by the SCAN926260 receiver input threshold of ±50mV.

BYPASS

Circuit board layout and stack-up for the BLVDS devices should be designed to provide noise-free power to the device. Good layout practice will also separate high-frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power / ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 3X the power supply voltage being used.

It is a recommended practice to use two vias at each power pin as well as at all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components. Locate RF capacitors as close as possible to the supply pins, and use wide low impedance traces (not 50 Ohm traces). Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLL circuitry.

Use at least a four layer board with a power and ground plane. Locate CMOS (TTL) signals away from the LVDS lines to prevent coupling. Closely-coupled differential lines of 100 Ohms Z_{DIFF} are typically recommended for LVDS interconnects. The closely-coupled lines help to ensure that coupled noise will appear as common-mode and is rejected by the receivers. Also, the tight coupled lines will radiate less.

Termination of the LVDS interconnect is required. For point-to-point applications, termination should be located at the load end. Nominal value is 100 Ohms to match the line's differential impedance. Place the resistor as close to the receiver inputs as possible to minimize the resulting stub between the termination resistor and receiver.

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI web site at: http://www.ti.com/ww/en/analog/interface/lvds.shtml. For packaging information on NFBGA's, please see AN-1126 (SNOA021).

Guidance for the SCAN926260 is provided next:

SCAN926260: SIX 1 TO 10 DESERIALIZERS

General guidance is provided below. Exact guidance can not be given as it is dictated by other board level /system level criteria. This includes the density of the board, power rails, power supply, and other integrated circuit power supply needs.

DVDD = DIGITAL SECTION POWER SUPPLY

These pins supply the digital portion and receiver output buffers of the device. Receiver DVDD pins require more bypass to power outputs under synchronous switching conditions. An estimate of local capacitance requires a minimum of 20nF. This is calculated by taking 66 (60 LVTTL Outputs + 6 RCLK Outputs) times the maximum output short circuit current (IOS) of 85mA. Multiplying this number by the maximum rise time (t_{CLH}) of 4ns and dividing by the maximum allowed droop in VDD (assume 50mV) yields 448.8nF. Dividing this number by the number of DVDD pins (25) yields 18nF. Rounding up to a standard value, 0.1uF is selected for each DVDD pin. The capacitative bandwidth for this capacitor may be extended by placing a 0.01uF capacitor in parallel. The 0.01uF capacitor should be placed closer to the DVDD pin than the 0.1uF capacitor.

PVDD = PLL SECTION POWER SUPPLY

The PVDD pin supplies the PLL circuit. PLL circuits require clean power for the minimization of jitter. A supply noise frequency in the 300kHZ to 1MHz range can cause increased output jitter. Certain power supplies may have switching frequencies or high harmonic content in this range. If this is the case, filtering of this noise spectrum may be required. A notch filter response is best to provide a stable VDD, suppression of the noise band, and good high-frequency response (clock fundamental). This may be accomplished with a pie filter (CRC or CLC). If employed, a separate pie filter is recommended for each PLL to minimize drop in potential due to the series resistance. Separate power planes for the PVDD pins is typically not required.

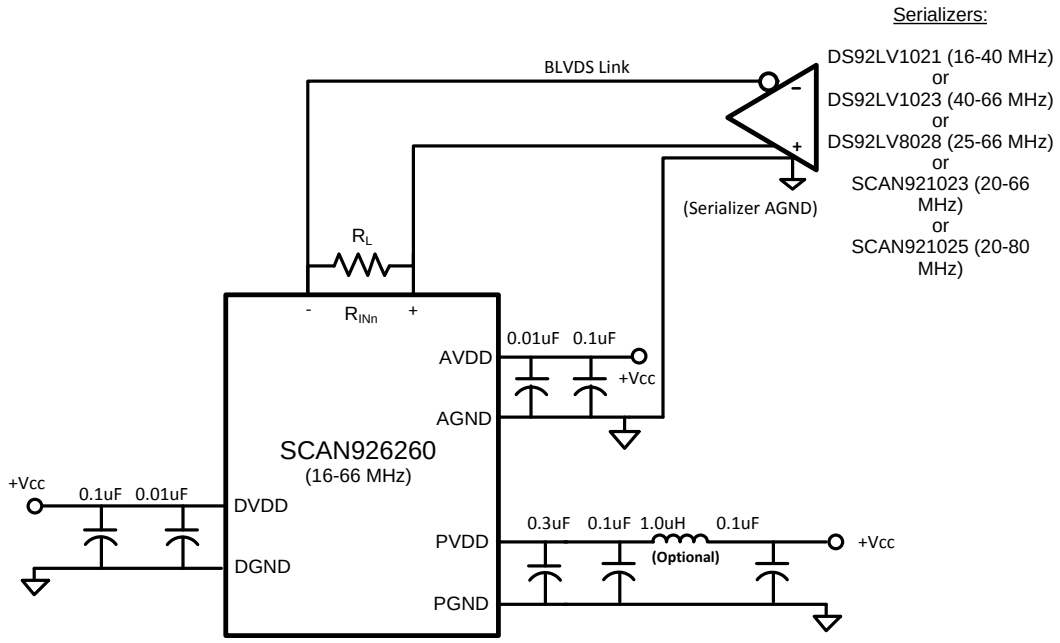
AVDD = LVDS SECTION POWER SUPPLY

The AVDD pin supplies the LVDS portion of the circuit. The SCAN926260 has four AVDD pins. Due to the nature of the design, current draw is not excessive on these pins. A 0.1uF capacitor is sufficient for these pins. If space is available, the 0.01uF capacitor may be used in parallel with the 0.1uF capacitor for additional high frequency filtering.

GROUNDs

The AGND pin should be connected to the signal common in the cable for the return path of any common-mode current. Most of the LVDS current will be odd-mode and return within the interconnect pair. A small amount of current may be even-mode due to coupled noise and driver imbalances. This current should return via a low impedance known path.

For a typical application circuit, please see Figure 10.



(Only one power/ground for each supply type shown for clarity-bypass networks should be repeated for all power/ground pairs.)

Figure 10. Typical Application Circuit

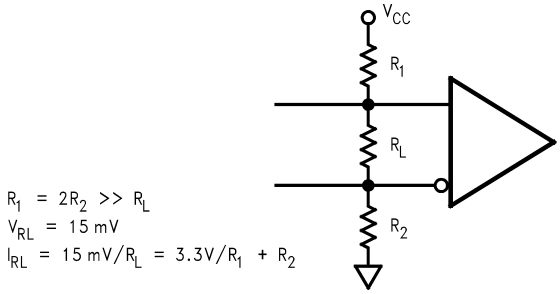


Figure 11. Optional Additional External Failsafe Biasing

Pin Diagram

Figure 12. Top View of SCAN926260TUF (196 pin NFBGA)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DGND	REN	$R_{IN0}-$	$R_{IN0}+$	AGND	$R_{IN2}-$	$R_{IN2}+$	AGND	$R_{IN4}-$	$R_{IN4}+$	AV_{DD}	PWRDWN*1	PWRDWN*0	PGND
B	DV_{DD}	GND	DV_{DD}	REFCLK	MS_PWRDWN*	AV_{DD}	AGND	AGND	AV_{DD}	BISTMODE_REQ	AGND	PGND	N/C	GND
C	TMS	TRST*	PWRDWN*2	DV_{DD}	$R_{IN1}-$	$R_{IN1}+$	AV_{DD}	$R_{IN3}-$	$R_{IN3}+$	$R_{IN5}-$	$R_{IN5}+$	PWRDWN*5	N/C	BIST_SEL2
D	TDI	TCK	TDO	DGND	DGND	DV_{DD}	DGND	BIST_SEL0	DGND	PGND	DGND	DV_{DD}	$LOCK_5$*	BIST_SEL1
E	PV_{DD}	R_{OUT09}	N/C	R_{OUT08}	DGND	DV_{DD}	DV_{DD}	DGND	DV_{DD}	DV_{DD}	PWRDWN*3	R_{OUT57}	R_{OUT58}	R_{OUT59}
F	PV_{DD}	$RCLK_0$	$LOCK_0$*	R_{OUT07}	DGND	DGND	DV_{DD}	DGND	DGND	DV_{DD}	PWRDWN*4	DV_{DD}	$RCLK_5$	PV_{DD}
G	PGND	PGND	R_{OUT06}	R_{OUT05}	DGND	DV_{DD}	DGND	DGND	DGND	DV_{DD}	R_{OUT55}	R_{OUT56}	PGND	PV_{DD}
H	PGND	R_{OUT04}	R_{OUT02}	R_{OUT03}	DGND	DV_{DD}	DGND	DGND	DGND	DV_{DD}	R_{OUT54}	R_{OUT53}	PGND	PGND
J	PV_{DD}	R_{OUT12}	R_{OUT10}	PGND	DV_{DD}	DGND	DGND	DV_{DD}	DV_{DD}	DV_{DD}	R_{OUT52}	R_{OUT51}	PGND	PV_{DD}
K	PV_{DD}	R_{OUT14}	R_{OUT00}	R_{OUT01}	DV_{DD}	DV_{DD}	DV_{DD}	DGND	DGND	DV_{DD}	BIST_ACT	R_{OUT50}	R_{OUT40}	PV_{DD}
L	R_{OUT13}	$RCLK_1$	R_{OUT11}	GND	GND	R_{OUT21}	DGND	R_{OUT31}	R_{OUT34}	DV_{DD}	R_{OUT45}	R_{OUT41}	R_{OUT44}	R_{OUT42}
M	R_{OUT15}	R_{OUT18}	R_{OUT19}	R_{OUT29}	R_{OUT25}	R_{OUT23}	R_{OUT20}	R_{OUT30}	R_{OUT33}	R_{OUT35}	R_{OUT36}	R_{OUT46}	$RCLK_4$	R_{OUT43}
N	R_{OUT16}	R_{OUT17}	$LOCK_2$*	R_{OUT27}	$RCLK_2$	R_{OUT22}	PGND	PGND	R_{OUT32}	$RCLK_3$	R_{OUT37}	R_{OUT39}	R_{OUT47}	R_{OUT48}
P	$LOCK_1$*	R_{OUT28}	R_{OUT26}	R_{OUT24}	PV_{DD}	PV_{DD}	PGND	PGND	PV_{DD}	PV_{DD}	R_{OUT38}	$LOCK_3$*	$LOCK_4$*	R_{OUT49}

Note: * = $\overline{\text{OVERBAR}}$

Pin Descriptions

Pin Name	Type	Pins	Description
GND	GND	B2, B14, L4, L5	Ground pins for ESD structures.
$R_{INn}\pm$	Bus LVDS Input	A3-A4, A6-A7, A9-10, C5-C6, C8-C9, C10-C11	Bus LVDS differential input pins. Failsafe described in Application Information section.
N/C		E3	This pin is not bonded out. Therefore, you may tie this pin High, Low, or as a N/C. However, for board layout compatibility with the SCAN921260 or the DS92LV1260, tie this pin LOW.
DVdd		B1, B3, C4, D6, D12, E6, E7, E9, E10, F7, F10, F12, G6, G10, H6, H10, J5, J8, J9, J10, K5, K6, K7, K10, L10	Supply voltage for digital section.
DGND		A1, D4, D5, D7, D9, D11, E5, E8, F5, F6, F8, F9, G5, G7, G8, G9, H5, H7, H8, H9, J6, J7, K8, K9, L7	Ground pins for digital section.
PVdd		E1, F1, F14, G14, J1, J14, K1, K14,P5, P6, P9, P10	Supply voltage for PLL circuitry.
PGND		A14, B12, D10, G1, G2, G13, H1, H13, H14, J4, J13, N7, N8, P7, P8	Ground pins for PLL circuitry.
AVdd		A11, B6, B9, C7	Supply voltage for analog circuitry.
AGND		A5, A8, B7, B8, B11	Ground pins for analog circuitry.
$\overline{\text{PWRDWN}}$ [0:5]	3.3V CMOS Input	A12, A13, C3, C12, E11, F11	A low on one of these pins puts the corresponding channel into sleep mode and a high makes the corresponding channel active. There is an internal pull-down on each of these pins that defaults the $\overline{\text{PWRDWNn}}$ input to sleep mode. Active operation requires asserting a high on the $\overline{\text{PWRDWNn}}$ and $\overline{\text{MS\_PWRDWN}}$ input.
$\overline{\text{MS\_PWRDWN}}$	3.3V CMOS Input	B5	A low on this pin puts the device into sleep mode and a high makes the part active. There is an internal pull-down that defaults the $\overline{\text{MS\_PWRDWNn}}$ input to sleep mode. Active operation requires asserting a high on the $\overline{\text{MS\_PWRDWNn}}$ input.
REN	3.3V CMOS Input	A2	Enables the ROUTn[0:9], RCLKn, outputs. There is an internal pull-down that defaults REN to tri-state the outputs. Active outputs require asserting a high on REN. Please note that $\overline{\text{LOCKn}}$ is not affected by REN.
REFCLK	3.3V CMOS Input	B4	Frequency reference input. Used by the PLL while locking onto incoming LVDS streams.Has no phase relation to RCLK.
$\overline{\text{LOCK}}$[0:5]	3.3V CMOS Output	D13, F3, N3, P1, P12, P13	Indicates the status of the PLLs for the individual deserializers: $\overline{\text{LOCKn}}$= L indicates locked, $\overline{\text{LOCKn}}$= H indicates unlocked.
ROUTn[0:9]	3.3V CMOS Output	E2, E4, E12, E13, E14, F4, G3, G4, G11, G12, H2, H3, H4, H11, H12, J2, J3, J11, J12, K2, K3, K4, K12, K13, L1, L3, L6, L8, L9, L11, L12, L13, L14, M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M14, N1, N2, N4, N6, N9, N11, N12, N13, N14, P2, P3, P4, P11, P14	Outputs for the ten bit deserializers; n = deserializer number. When a channel is not locked, ROUT[0:9] are high for that channel.
RCLK[0:5]	3.3V CMOS Output	F2, F13, L2, M13,N5, N10	Recovered clock for each deserializer's output data. When a channel is not locked, the RCLK for that channel is high.
TMS	3.3V CMOS Input	C1	Test Mode Select input to support IEEE 1149.1. There is a weak internal pull-up on TMS that defaults TRST, TDI, TCK and TDO to be inactive. However, in noisy environments, pulling TMS high ensures the JTAG test access port (TAP) is never activated.
$\overline{\text{TRST}}$	3.3V CMOS Input	C2	Test Reset Input to support IEEE 1149.1. There is a weak internal pull-up on this pin.
TDI	3.3V CMOS Input	D1	Test Data Input to support IEEE 1149.1. There is a weak internal pull-up on this pin.
TCK	3.3V CMOS Input	D2	Test Clock to support IEEE 1149.1

Pin Descriptions (continued)

Pin Name	Type	Pins	Description
TDO	3.3V CMOS Output	D3	Test Data Output to support IEEE 1149.1.
BISTMODE_REQ	3.3V CMOS Input	B10	BIST Alone Error Reporting Mode Select Input.
BIST_SEL[0:2]	3.3V CMOS Input	C14, D8, D14	These pins control which channels are active for the BIST Alone operating mode. The BIST Alone Mode Selection Table describes their function. There are internal pull-ups that default all BIST_SEL[0:2] to high, which is the idle state for all channels in the BIST Alone mode.
BIST_ACT	3.3V CMOS Input	K11	A high on this pin activates the BIST Alone operating mode. There is a weak internal pull-down that should default the BIST_ACT to de-activate the BIST Alone operating mode. In a noisy operating environment, it is recommended that an external pull down be used to ensure that BIST_ACT stays in the low state.
N/C		B13, C13	Unused solder ball location. Do not connect.

REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SCAN926260TUF/NOPB	ACTIVE	NFBGA	NZH	196	119	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	SCAN926260T UF >B	Samples
SCAN926260TUFX/NOPB	ACTIVE	NFBGA	NZH	196	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	SCAN926260T UF >B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

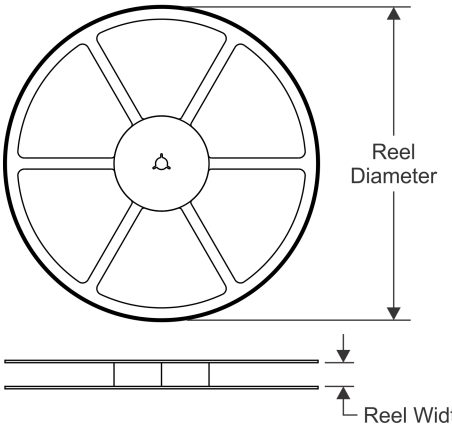
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

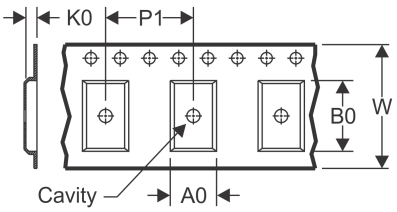
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

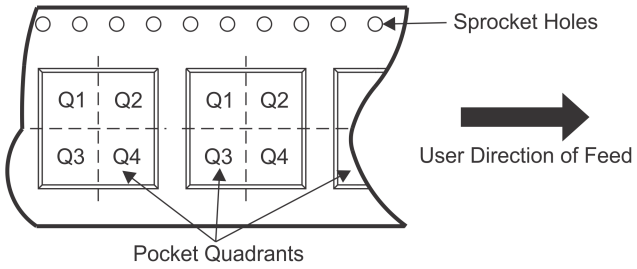


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

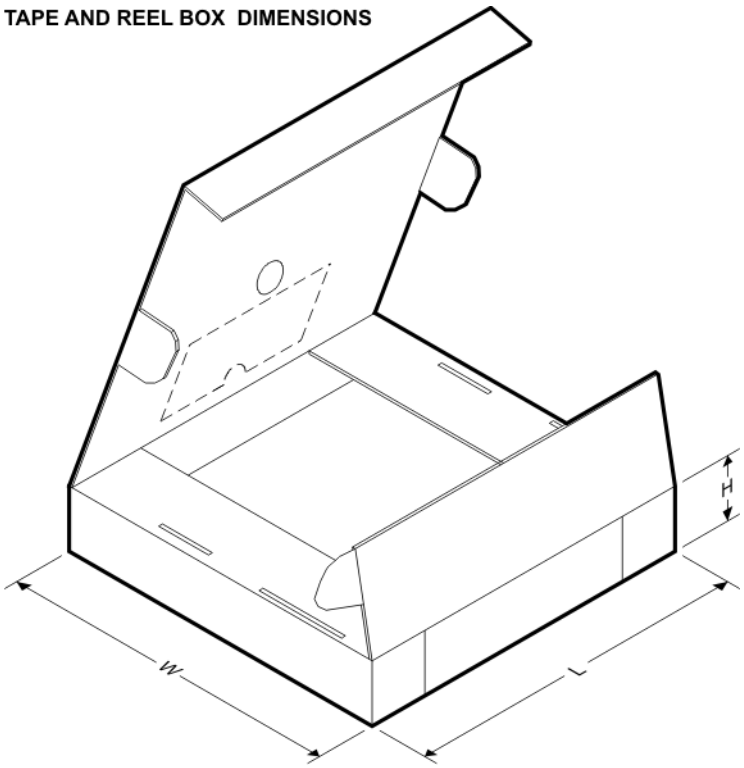
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SCAN926260TUFX/NOPB	NFBGA	NZH	196	1000	330.0	24.4	15.3	15.3	2.5	20.0	24.0	Q1

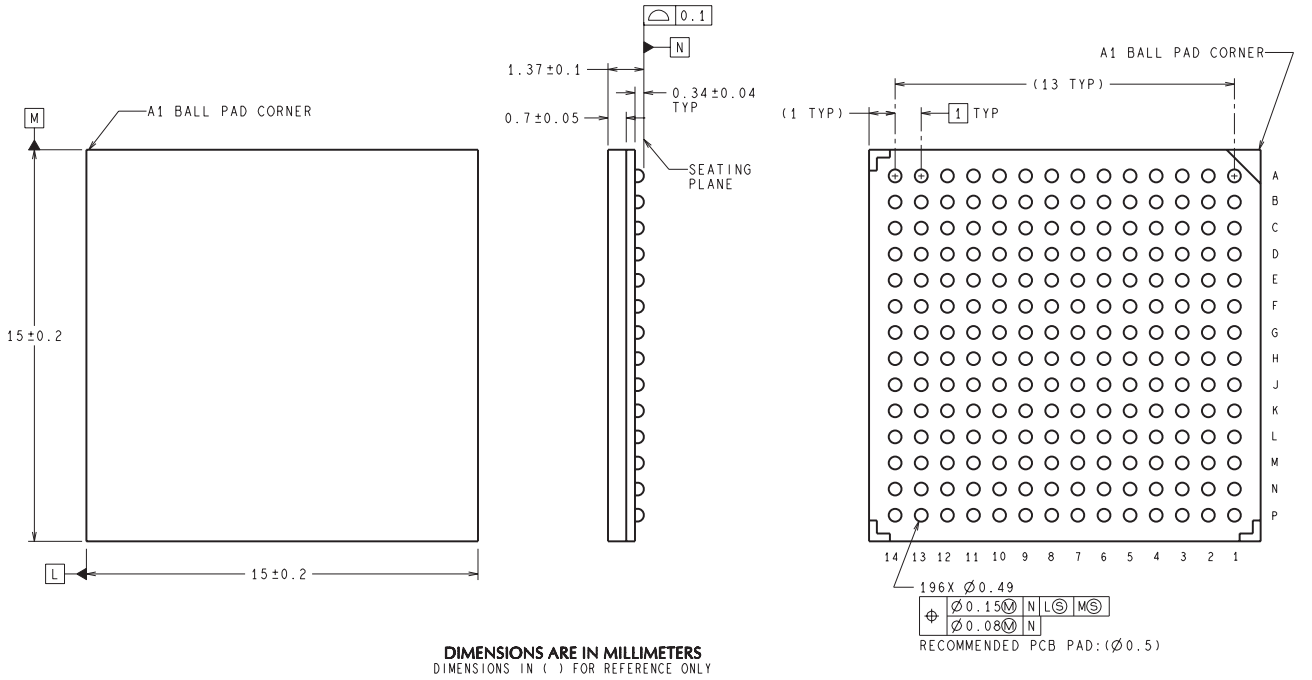
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SCAN926260TUFX/NOPB	NFBGA	NZH	196	1000	367.0	367.0	45.0

NZH0196A



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

UJB196A (Rev C)

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