The QS722X5 Family: Designer-Friendly, 18-Bit-Wide Clocked FIFOs

Application Note AN-26

INTRODUCTION

The new Quality Semiconductor QS722X5-family 18-bit-wide First-In, First-Out memories (FIFOs) are high-speed, synchronous digital specialty-memory devices, useful for local temporary storage and for data-rate-matching applications in high-performance digital systems.

These FIFOs are implemented CMOS static-RAM technology and feature many conveniences and useful options for digital-system designers. One of them can replace two industry-standard 9-bit-wide asynchronous FIFOs of the same depth, and at the same time provide higher-speed operation and more convenient timing characteristics. They also can replace other existing 18-bit-wide FIFOs, in many cases without design changes to the system.

The QS722X5 family includes four pin-compatible FIFOs, differing in depth: QS72215 (51218, meaning 512 x 18-bit words); QS72225 (1024 x 18); QS72235 (2048 x 18); and QS72245 (4096 x 18). As of this writing, the first two of these FIFOs are in production; the other two are in design. These FIFOs are available in speed grades up to 50 MHz (20 ns-cycle-time).

DESIGN ADVANTAGES OF QS722X5-FAMILY FIFOS

The flexible QS722X5 control scheme allows selection of a wide variety of useful operating configurations. Some of these implement Quality Semiconductor-proprietary functionality; the rest either are industry standard, or else support emulation of the behavior of other FIFOs.

These Quality Semiconductor FIFOs are pin-compatible and functionally-compatible with the existing IDT722X5LB industry-standard 18-bit-wide FIFO family. And they are functionally similar, although not quite fully 100% pin-compatible, with the existing TI SN74ACT7801/11/81 18-bit-wide FIFO family.

Figure 1 is the common block diagram for all Quality Semiconductor QS722X5-family FIFOs. Figure 2 shows the pinout common to all QS722X5 family members, for the industry-standard 68-pin PLCC (Plastic Leadless Chip Carrier) package. Table 1 summarizes the meanings of the pin names.

Bold-italic typeface is used in QS722X5-family- related figures, tables, and text to indicate Quality Semiconductor-proprietary functionality and/or signals.

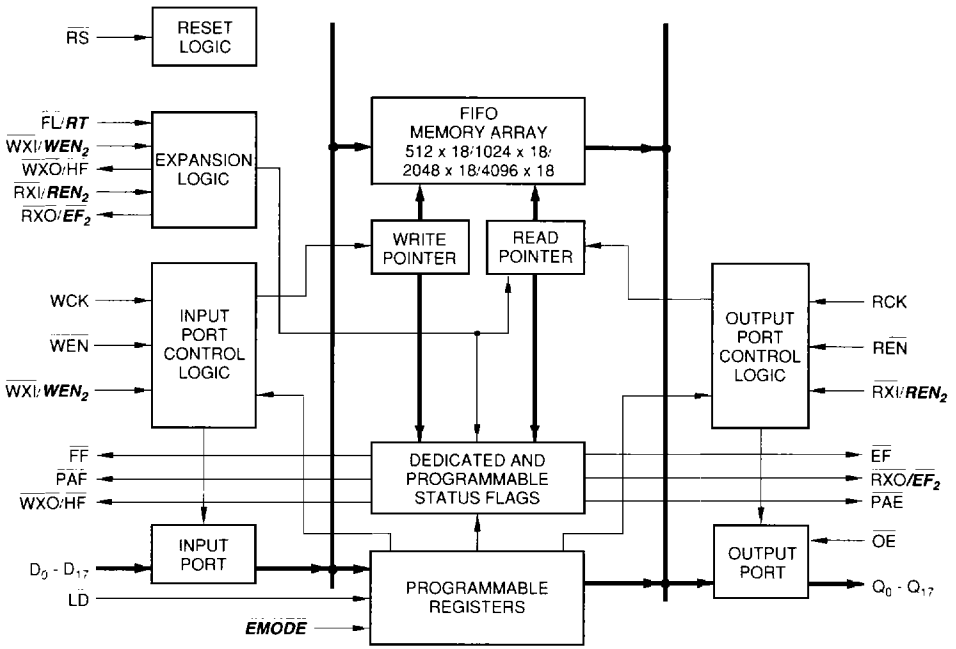
SYNCHRONOUS OPERATION

In QS722X5-family FIFOs, all input and output data-transfer processes and most input control signals are fully synchronized, with respect to one or the other of the two port clocks. If their function relates to the input port, synchronization is to the write clock WCLK. If their function relates to the output port, then it is to the read clock RCLK.

Some of the output status signals ("flags") are fully synchronized by design. Others may be programmed, at any time, to behave either synchronously or asynchronously. When flags are synchronized, it is always to the port clock most likely to be used by the system to synchronize reading them.

In addition to being respectively synchronized by the write clock and the read clock, input and output data-transfer steps likewise must be *enabled* by write-enable and read-enable control signals. These control signals are themselves synchronized to the respective port clocks.

FIGURE 1. QS722X5 BLOCK DIAGRAM



***BOLD ITALIC* = Enhanced Operating Mode.**

High-speed state machines, implemented with registered PLDs (Programmable-Logic Devices), often are used to control the operation of fast synchronous FIFOs such as these QS722X5-family devices. A PLD which is controlling the input side of a synchronous FIFO may itself be synchronized to the same waveform which is being supplied as that FIFO's write clock. Likewise, a PLD which is controlling the output side of a synchronous FIFO may be synchronized to that FIFO's read clock. Simple, easily generated, periodic symmetric square-waves may be used for both of these FIFO clocks, as well as for PLD clocks.

Such a PLD-FIFO combination may be operated at fast cycle times as small as the worst-case sum of a clock-to-output time of one of the two parts added to a setup time of the other part, presumably with some small wiring-delay time factor also added in.

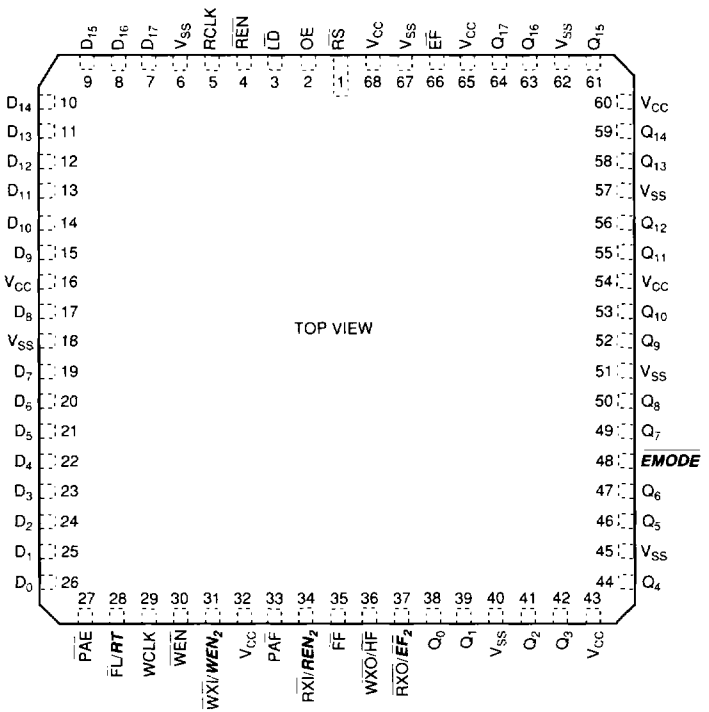
Asynchronous FIFOs are not nearly as amenable to this same state-machine, symmetric-clock control strategy. Most such parts lack the separate write-enable and read-enable control signals, distinct from the write clock and the read clock. Rather, they have write-demand and read-demand control signals, often loosely referred to as "clocks," which *combine* within the same edge-sensitive signal both the clocking and the enabling functionality in a manner which isn't too convenient for control of the FIFO by the system. Carefully shaped, gated, *asymmetric* clock waveforms may in fact be needed to drive these demand signals, at least with optimized timing, whenever asynchronous FIFOs are run at data-transfer repetition rates faster than approximately 20–30 MHz.

TABLE 1. QS722X5 FAMILY COMMON PIN DESIGNATIONS

Name	I/O	DESCRIPTION
D17-D0	I	Data Inputs
$\overline{RS}$	I	Reset
$\overline{EMODE}$	I	***Enhanced Operating Mode***
WCLK	I	Write Clock
$\overline{WEN}$	I	Write Enable
RCLK	I	Read Clock
$\overline{REN}$	I	Read Enable
$\overline{OE}$	I	Output Enable
$\overline{LD}$	I	Load
$\overline{FL}$/***RT***	I	First Load/***Retransmit***
$\overline{WXI}$/***WEN2***	I	Write Expansion Input/ ***Write Enable 2***

Name	I/O	Function
$\overline{RXI}$/***REN2***	I	Read Expansion Input/ ***Read Enable 2***
$\overline{FF}$	O	Full Flag
$\overline{PAF}$	O	Programmable Almost-Full Flag
$\overline{WXO}$/$\overline{HF}$	O	Write Expansion Output/Half-Full Flag
$\overline{EF}$	O	Empty Flag
$\overline{PAE}$	O	Programmable Almost-Empty Flag
$\overline{RXO}$/$\overline{EF2}$	O	Read Expansion Output/***Empty Flag 2***
Q17-Q0	O	Data Outputs
Vcc		Power
Vss		Ground

FIGURE 2. QS722X5 FAMILY PLCC PINOUT DIAGRAM



BOLD ITALIC = Enhanced Operating Mode.

COMPATIBILITY WITH OTHER FIFO FAMILIES

The Quality Semiconductor QS722X5-family FIFOs have a pinout identical to that of the Integrated Device Technology IDT722X5LB-family FIFOs, and can directly replace them in existing applications with no system-design changes whatever.

The pinout shown in Figure 2 also is the pinout for IDT722X5LB-family FIFOs, with only the following changes: *all* signal names written in bold-italic type are disregarded, and V_{CC} is substituted for ***$\overline{EMODE}$*** (pin 48).

However, the Quality Semiconductor FIFOs have functionality and flexibility which go beyond that of the IDT FIFOs. A QS722X5 master-control pin, ***$\overline{EMODE}$ (Enhanced Operating Mode)***, selects strict IDT-compatible operation when tied HIGH, but enables additional non-IDT Quality Semiconductor ***"Enhanced-Operating-Mode"*** features when tied LOW. Since the ***$\overline{EMODE}$*** pin was a V_{CC} pin in the original IDT pinout, it *always* will have been tied HIGH in any design originally based on IDT722X5LB FIFOs.

Several of these ***Enhanced-Operating-Mode*** features are directed at emulating the functionality of the Texas Instruments SN74ACT7801/11/81 FIFOs, which have a pinout very similar to, although not fully identical to, the Quality Semiconductor and IDT FIFOs. In particular, all input-data and output-data pins are in the same locations, and likewise for many power and ground voltage-supply pins. Refer to Figure 3a and Figure 3b for the exact pinout similarities and differences.

Thus, the Quality Semiconductor FIFOs can replace the IDT FIFOs, with *no* wiring or control-logic changes; and they also can replace the TI FIFOs, with minor wiring and control-logic changes. When operated in an appropriately chosen mode, the Quality Semiconductor FIFOs exhibit no major behavioral differences which would affect a *system-level* block diagram for a system design originally based either on IDT722X5LB FIFOs or on TI SN74ACT7801/11/81 FIFOs.

One proprietary Quality Semiconductor feature, ***Retransmit*** capability, is available regardless of the state of ***$\overline{EMODE}$***. However, the ***Retransmit*** capability never becomes activated when a Quality Semiconductor FIFO is used in a socket already prewired for an IDT FIFO, which has the $\overline{RT}$ pin grounded.

CONFIGURABILITY

As already mentioned, the Quality Semiconductor QS722X5 FIFOs use one IDT722X5LB V_{CC} pin for their ***$\overline{EMODE}$*** control signal; otherwise, they strictly follow the IDT722X5LB pinout. When ***$\overline{EMODE}$*** is tied HIGH, as it always would be in any design originally based on IDT722X5LB FIFOs, IDT-compatible behavior is selected. However, when ***$\overline{EMODE}$*** is tied LOW, Quality Semiconductor's proprietary ***Enhanced-Operating-Mode*** features are activated.

Switching this ***$\overline{EMODE}$*** signal dynamically during FIFO operation is *not* recommended. ***$\overline{EMODE}$*** should remain in the same state following any FIFO reset operation, during subsequent system operation, until another FIFO reset operation occurs.

Tying ***$\overline{EMODE}$*** LOW in and of itself changes the functionality of three QS722X5 pins. In IDT-Compatible Operating Mode, these three pins are used to link together successive FIFOs being cascaded according to the IDT "two-wire-token-passing" principle. Tying ***$\overline{EMODE}$*** LOW also makes the Quality Semiconductor-proprietary ***Control Register*** visible and accessible to the system, via the normal FIFO input and output data ports.

When ***$\overline{EMODE}$*** is LOW during a reset operation, the ***Control Register*** is initialized to activate *all* of Quality Semiconductor's proprietary programmable ***Enhanced-Operating-Mode***

features. If any of these features are not desired in a given application, they may be disabled individually by writing different contents into bits 00-05 of the ***Control Register***. They also may be subsequently re-enabled, at any time, in the same manner.

The programmable QS722X5 features include: synchronizing the three "middle" flags (almost-full, half-full, almost-empty) to the appropriate port clocks; suppressing the advancement of the internal read-address pointer whenever the data outputs are disabled ("data-loss prevention"); and simplifying the procedure for programming, or verification readback, of the FIFO's loadable registers.

When the ***Control Register*** is active, the Almost-Full flag may be synchronized to the write clock; the Almost-Empty flag may be synchronized to the read clock; and the Half-Full flag may be synchronized to either one of these clocks. The Full flag and the Empty flag are not programmable in this manner; they always are synchronized respectively to the write clock and to the read clock. This scheme assigns the synchronization of each flag to that clock most likely to be used for synchronizing the reading of the flag by the system, in order to minimize metastability hazards. The Almost-Empty, Half, and Almost-Full flags, when chosen to be synchronous, utilize two-stage synchronizers for a high level of metastability protection.

However, it is possible to program any or all of the three "middle" flags to operate asynchronously, even in the ***Enhanced Operating Mode.*** In the IDT-Compatible Operating Mode, they *always* operate asynchronously. In *either* mode, they operate faster than the corresponding flags of the same speed grade of the equivalent IDT device.

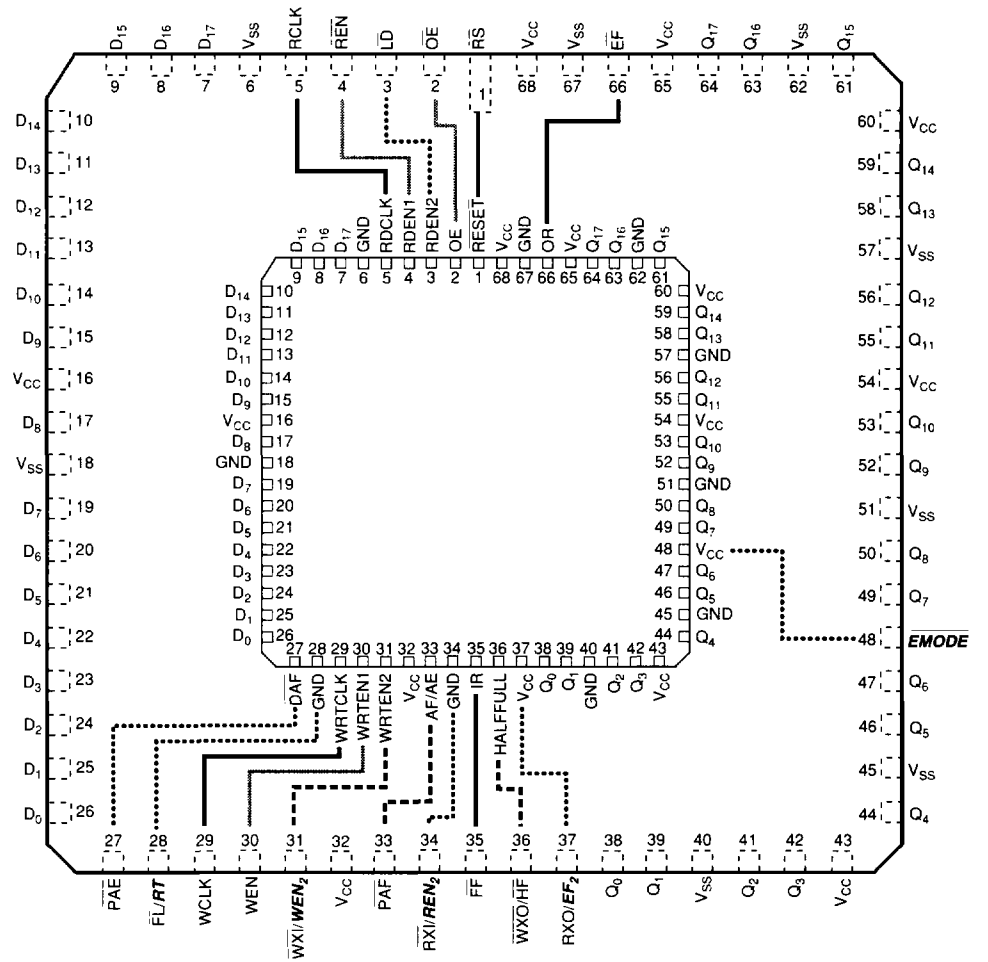
The QS722X5 architecture also includes two other configuration-control registers, the "offset" registers. These offset registers define the system meaning of the Almost-Full flag and the Almost-Empty flag, respectively, and are fully equivalent to the similar registers in the IDT722X5LB architecture. The number of bits actually implemented in these registers and their default contents after a reset operation increase somewhat for the deeper QS722X5-family members.

The prewired default values contained in these offset registers vary somewhat according to FIFO depth. For the smaller QS722X5-family members, these default values are one-eighth of the FIFO depth, minus one: respectively, 63_{10} for the QS72215 and 127_{10} for the QS72225. For both the QS72235 and QS72245 the default values are again 127_{10}. Whenever the prewired default values are acceptable for an application, no reprogramming is necessary.

The offset registers and the control register may be programmed with new contents from the input-data bus, and their contents may be read back out for verification on the output-data bus. Asserting a special control signal, $\overline{LD}$ (load), distinguishes configuration-register accesses from normal FIFO-memory accesses. Two simple state machines, one for each data bus, select the register to be written into or to be read back from, according to a fixed sequence.

In ***Enhanced Operating Mode***, each of these two state machines has *three* states apiece, so that all three registers are accessible and visible. However, in IDT-Compatible Operating Mode, the two state machines have only *two* states apiece, and the control register is neither accessible nor visible.

FIGURE 3A. COMMON PIN LOCATIONS FOR VOLTAGE-SUPPLY AND DATA PINS IN QSI AND TI 18-BIT-WIDE FIFOS



Notes:

Same ——————

Same except for polarity ~~~~~~~

Similar, not the same - - - - - -

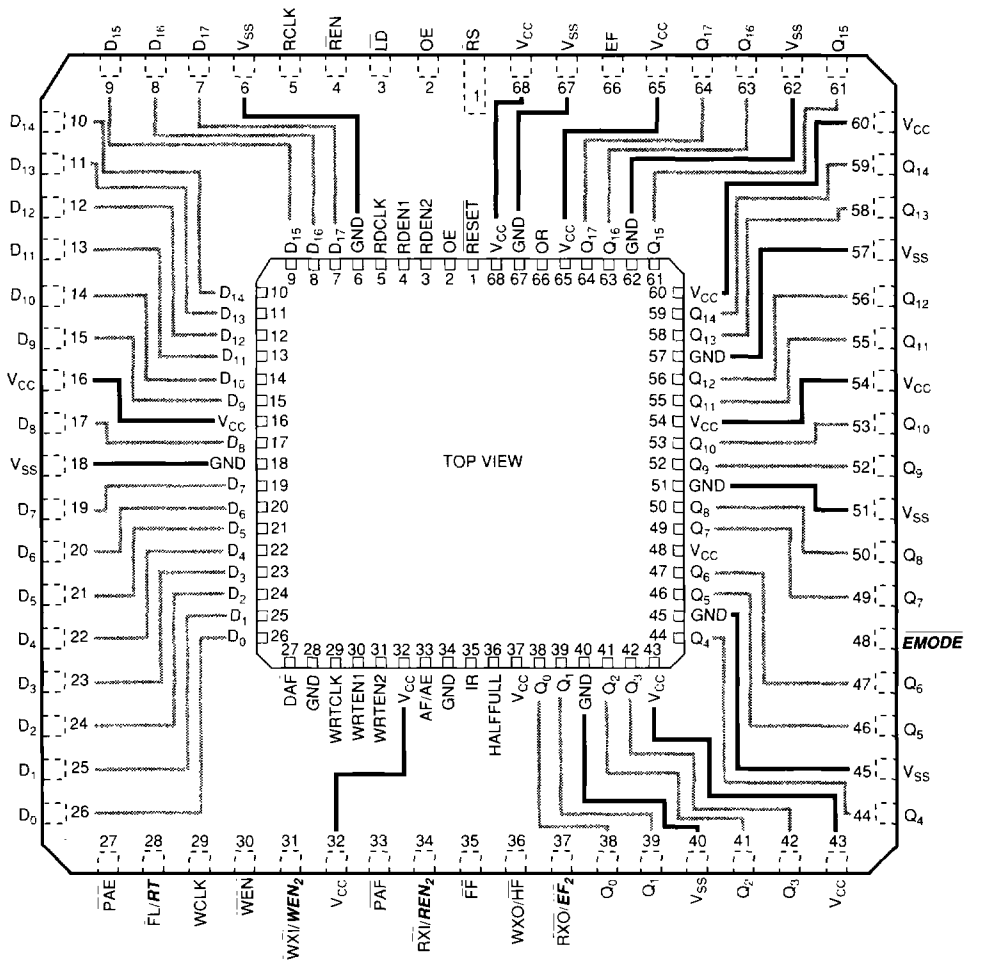
Different ·····

Inner package symbol is TI SN74ACT7801/11/81 pinout.

Outer package symbol is QS722x5-family pinout.

BOLD ITALIC = Enhanced Operating Mode.

FIGURE 3B. CONTROL PIN DIFFERENCES BETEWEEN QSI AND TI 18-BIT-WIDE FIFOS



Notes:

Voltage supply ——

Data ~~~~~~~~~~

Inner package symbol is TI SN74ACT7801/11/81 pinout.

Outer package symbol is QS722x5-family pinout.

BOLD ITALIC = Enhanced Operating Mode.

CASCADING AND PARALLELING QS722X5-FAMILY FIFOS

For FIFOs, as for other semiconductor memories, there is always a memory-capacity gap between the largest FIFOs currently in production and the largest FIFOs which customers need for the new state-of-the-art digital systems they are attempting to design. Over time, *both* the immediately available FIFOs and the needed-but-not-yet-available FIFOs get larger and larger; but the gap between them always remains!

An approach which semiconductor manufacturers have taken, trying to address customers' perceived needs for ever-larger FIFOs, is to provide support within FIFO architectures for combining individual FIFO devices into larger "effective FIFOs." This support takes the form of extra control inputs and status outputs ("hooks") for control connections between FIFOs, and sometimes also of other additional on-chip resources.

There are two fundamental ways in which FIFO devices may thus be combined: *cascading*, or "depth-cascading," in which the effective FIFO has *more* memory words than do each of the individual FIFO devices; and *paralleling*, sometimes rather confusingly called "width-cascading," in which the effective FIFO has *wider* memory words than do each of the individual FIFO devices. Sometimes, both cascading and paralleling are used within a single FIFO application to implement an effective FIFO which is *both* deeper and wider than one individual FIFO device.

QS722X5-family FIFOs feature architectural support for *two* entirely different FIFO-cascading schemes: "two-wire token passing," which is the scheme used by IDT722X5LB-family FIFOs; and "handclasp" or "pipelining," which is the scheme used by TI SN74ACT7801/11/81 FIFOs. They also support one "interlocked" paralleling scheme, in which two FIFOs side-by-side operate together in strictly synchronized lockstep.

In principle, the two-wire token-passing cascading scheme also "parallels" FIFOs, but in a fundamentally different manner, as *alternates*, with a common input bus and a common output bus, arranged like a bunch of bananas (see Figure 4a). The pipelining cascading scheme, on the other hand, arranges FIFOs one after another in series, connected like a string of sausages (see Figure 4b).

CASCADING BY TWO-WIRE TOKEN PASSING

In the two-wire token-passing scheme, two or more individual QS722X5 FIFO devices are connected in parallel (see Figure 5). Their input data buses (pins D_0-D_{17}) are all tied together; and their output data buses (pins Q_0-Q_{17}) also are all tied together. However, only one of the paralleled FIFOs may be written into at any given time. Likewise, only one of the paralleled FIFOs may be read from at any given time. A data word passing through the effective FIFO passes through only one single physical FIFO device and gets handled just once.

The FIFO which is currently activated for writing is not necessarily the same one which is currently activated for reading, except under system-startup conditions that is, when all FIFOs have just completed being reset, and FIFO operation has only recently commenced.

QS722X5 FIFOs must have their $\overline{EMODE}$ control pins held at V_{CC} whenever they are being cascaded according to the two-wire token-passing scheme.

Exactly one of the QS722X5 FIFOs in the cascade must have its $\overline{RT}$ pin grounded; the $\overline{RT}$ pins of the remaining FIFOs are tied to V_{CC}. In this operating mode, the $\overline{RT}$ pin is being used to designate one of the FIFOs as the "first-load" or "master" device; the remaining FIFOs are sometimes referred to as "slave" devices. After a reset operation has initialized the entire FIFO cascade, each FIFO has figured out whether it is serving as a master device, or as a slave device, and both the "write token" and the "read token" reside within the first-load FIFO.

FIGURE 4A. PARALLEL CONNECTION OF DEPTH-CASCADED FIFOS

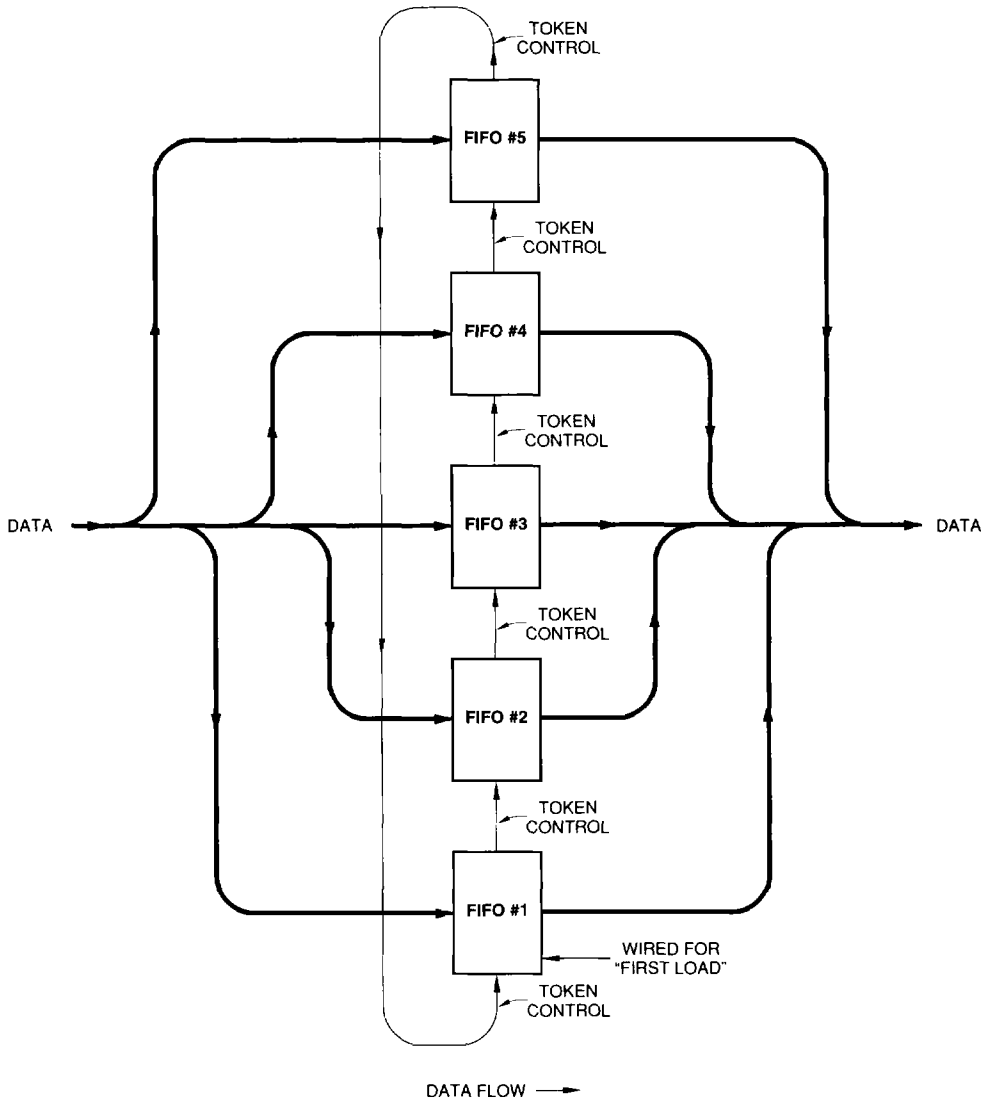


FIGURE 4B. SERIES CONNECTION OF DEPTH-CASCADED FIFOS

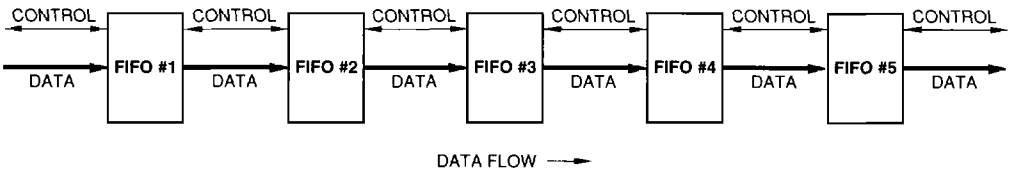
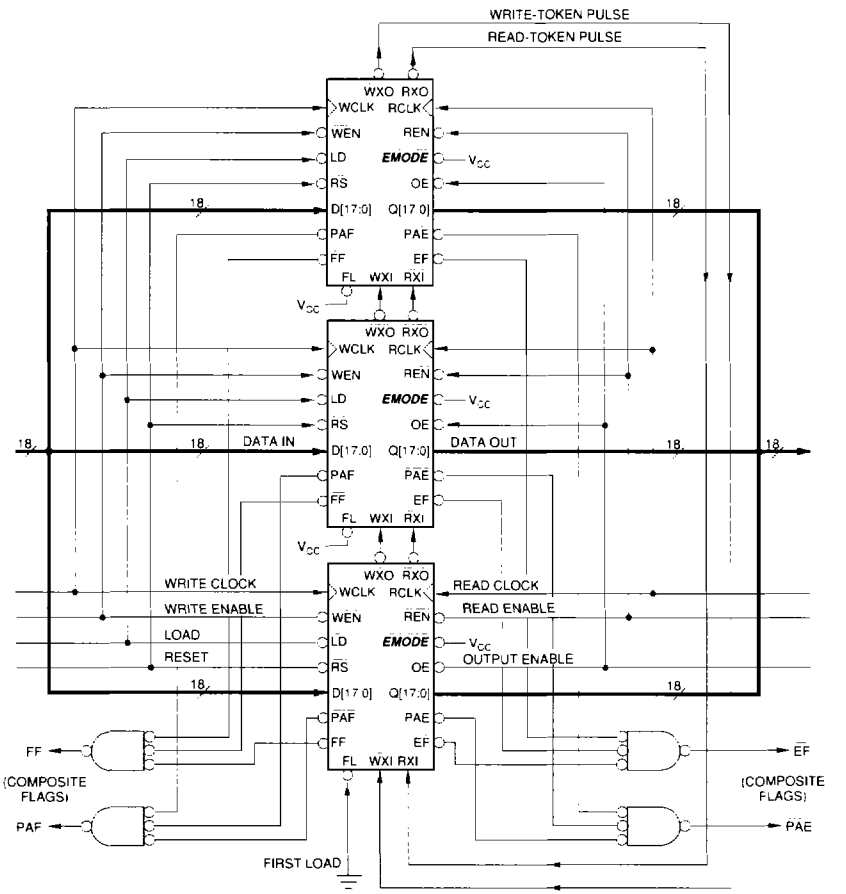


FIGURE 5. QS722X5 FAMILY FIFO DEPTH CASCADING USING IDT-COMPATIBLE "TOKEN-PASSING SCHEME"



Notes :
Grounding $\overline{FL}$ designates the "first-load" FIFO ("master" FIFO). The remaining FIFOs are "slave" FIFOs.
***BOLD ITALIC* = Enhanced Operating Mode.**

which is activated to respond and perform the requested operation whenever a write-enable or read-enable control signal is broadcast to all the FIFOs within the cascade. Obviously, one and *only* one FIFO device should respond for each requested operation. One consequence is that any FIFO which "does not have the read token" has its outputs *disabled*, in a high-impedance state, *even if* its $\overline{OE}$ (output enable) control signal currently is being asserted (LOW).

However, when the "token" (associated with the counter within the FIFO) has traversed all of the FIFO's memory locations, it does *not* return to physical location zero of that FIFO device, even though the counter does thus return. Rather, the token briefly becomes explicit; it takes the form of a narrow LOW-going pulse on one of the two expansion out outputs, $\overline{WXO}$ and $\overline{RXO}$. These are connected respectively to the expansion in inputs, $\overline{WXI}$ and $\overline{RXI}$, of the next FIFO device in the cascade. After the (write or read) token pulse has been transmitted and received, the sending FIFO becomes deactivated for writing or reading, as the case may be, and the receiving FIFO immediately becomes activated in its place, so that there never is any hiatus in the effective FIFOs' capability of performing a required operation.

The Half-Full flag status output, $\overline{HF}$, shares a pin with the $\overline{WXO}$ token output. Hence, $\overline{HF}$ is not available from a cascaded QS722X5-family FIFO, which has been initialized by a reset operation to be either a master or a slave. $\overline{HF}$ is available only from a FIFO which has been initialized to be a "standalone."[4] In any case, this signal does not have any really useful meaning for FIFOs within a cascade.

The two-wire token-passing cascading scheme was developed to eliminate one difficulty with the much-older one-wire token-passing cascading scheme: an occasional, intermittent, serious extra logic delay, in the event that the read pointer catches up with the write pointer in a FIFO, just as that FIFO is about to emit a write or a read expansion out token pulse. Of course, that combination of circumstances is infrequent; but it is by no means impossible! In cascaded FIFOs which use the one-wire scheme, if this delay is not explicitly allowed for in the system timing, then data may be lost unpredictably.

Now, in the one-wire token-passing architecture, *both* the write token pulse and the read token pulse must travel along to the next FIFO over the very same wire. Thus, every so often, *both* pulses must pass over that wire within one single word time, with enough of a gap in between them that they are recognized clearly at the other end as *two* distinct pulses. So, once in a great while, and at unforeseeable intervals, the system must halt briefly between two words in order to head off the occurrence of an unrecoverable system error, or else the data rate must be slowed down greatly in order to allow the time for this occasional extra pulse during *every* word time.

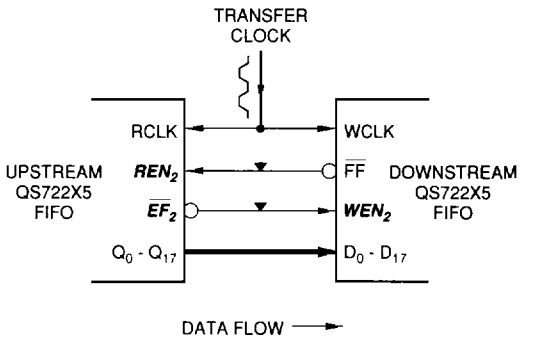
Because the two-wire token-passing cascading scheme avoids this troublesome flaw of the older one-wire scheme, it is much more appropriate for state-of-the-art high-performance synchronous FIFOs.

CASCADING BY PIPELINING

In the pipelined cascading scheme, two or more individual QS722X5 FIFO devices are connected in series; the output data bus (pins Q_0-Q_{17}) of the (n–1)st FIFO connects to the input data bus (pins D_0-D_{17}) of the (n)th FIFO.

A crosscoupled "handclasp" signaling scheme is used between successive FIFOs in the cascade, so that they coordinate their operations with each other properly (see Figure 6). The handclasp ensures that the upstream FIFO device does not attempt to force another data word upon the downstream FIFO device when the latter is full and, conversely, that the downstream device does not attempt to read another word from the upstream device when the latter is empty.

FIGURE 6. "HANDCLASP" DEPTH CASCADING INTERFACE BETWEEN QS722X5 FAMILY FIFOS



Note: ***BOLD ITALIC = Enhanced Operating Mode.***

In this scheme, all of the QS722X5 FIFOs must have their ***EMODE*** and $\overline{OE}$ control inputs grounded. A data word passing through the effective FIFO passes through every physical FIFO device in the cascade and gets handled once per device.

A "transfer clock" signal must be provided, at each FIFO-to-FIFO interface, to synchronize passing data from the (n-1)st FIFO to the (n)th FIFO. To optimize smoothness of operation, the same transfer-clock waveform may be used everywhere within a given FIFO cascade. Now, the write clock at the input end of the first FIFO in the cascade, and the read clock at the output end of the last FIFO in the cascade, may or may not be synchronous periodic waveforms. If both of these clocks are periodic waveforms, the faster one is an excellent choice for use also as the transfer-clock signal.

Grounding the ***EMODE*** control input of an QS722X5-family FIFO changes the functionality of several dual-purpose control pins: $\overline{WXI}$/***WEN$_2$***, $\overline{RXI}$/***REN$_2$***, and $\overline{RXO}$/*EF*. The **Enhanced-Operating-Mode** functionality is in each case that which is indicated by the second signal name, the one written in bold-italic type.

WEN$_2$ and ***REN$_2$*** are alternative, assertive-HIGH write-enable and read-enable control inputs, respectively. They have the correct polarity for the handclasp signaling scheme to operate properly with the assertive-LOW Full flag and empty flag status signals.

EF$_2$ is an exact duplicate of the usual Empty flag *EF*, except that it is delayed by one full read-clock interval with respect to *EF*. This extra-clock-interval delay is necessary for the handclasp signaling scheme to operate with the proper timing.

Within a FIFO, these tokens are *implicit*. When a FIFO "has one of the tokens," that simply means that it is the FIFO device.

For an QS722X5 FIFO-to-FIFO interface connected as shown in Figure 6, whenever the upstream FIFO device is not empty and the downstream FIFO device is not full, a data word is transferred from the upstream device to the downstream device after *every* transfer-clock rising edge.

If some interval of time passes without the entire FIFO cascade either being written into or being read from, the meaningful data within the cascade will accumulate in the FIFOs furthest downstream, "fall to the bottom of the hopper" as it were. In fact, "hopper" is one of the many technojargon synonyms for "FIFO."

PARALLELING

The QS722X5-family architecture supports "interlocked" paralleling of two identical side-by-side 18-bit-wide physical FIFO devices, so that they function as a 36-bit-wide effective FIFO of the same depth (see Figure 7). The QS722X5 interlocking scheme is the same one used with TI SN74ACT7801/11/81 FIFOs; however, the pinout and the signal nomenclature are somewhat different.

The purpose of "interlocking" is to ensure that the two side-by-side FIFO devices never get out of step with each other: one cannot write a word unless the other one also is ready to write a word, and similarly for reading a word. Without interlocking, very minor timing differences between the two physical devices, or circuit-board wire-length differences affecting them, occasionally might result in one FIFO having half of some word present on its outputs, while the other FIFO has the other half of the *previous* word in the data block present on *its* outputs!

Such a mistake may occur, for instance, when the two FIFO devices have been entirely emptied out and another full 36-bit word is written in, at such a time that t_{FRL} (first-read-latency time) is not quite met, so that one device responds properly with the next word, but the other device does not quite make it. A similar and logically dual possibility exists when the two FIFO devices have been entirely filled, and one word is read out at exactly the worst-case time, and one of the two devices takes slightly longer to become ready to receive another word, than does the other one.

This type of problem may arise either with synchronous FIFOs or with asynchronous FIFOs, although the latter are much more vulnerable to it. Thus, the interlocking scheme of Figure 7 is recommended whenever QS722X5-family FIFOs are used two abreast, to handle 36-bit data words. For wider data words, variations on this same scheme are possible; but they require external logic in addition to the FIFO devices themselves, since now more than two write enables and two read enables per physical device become necessary.

The architecture of QS722X5-family FIFOs supports combining interlocked paralleling with pipelined cascading, which is the recommended approach to implementing large effective FIFOs using arrays of QS722X5 devices (see Figure 8). Unfortunately, these devices cannot offer any similar support for combining interlocked paralleling with two-wire token-passing cascading; the additional pins which would be required are not available.

SUMMARY

The new Quality Semiconductor QS722X5-family 18-bit-wide FIFOs provide attractive alternatives for local-temporary-storage and data-rate-matching applications in contemporary high-speed digital systems. Members of this family range in capacity from 512 to 4096 18-bit words, with programmable choices between synchronous and asynchronous operation for three status-flag signals.

QS722X5-family FIFOs are eminently suitable for use in new high-performance designs. A single such FIFO can replace two paralleled conventional 9-bit-wide asynchronous FIFOs in many applications. Also, these FIFOs can seamlessly replace IDT722X5LB-family FIFOs in existing 18-bit-wide designs, without any rewiring. Moreover, they have certain architectural features which support emulating TI SN74ACT7801/11/81 FIFOs, although their compatibility with these TI FIFOs is not quite 100%.

QS722X5 FIFOs may be used individually, in "standalone" mode. Also, they have many architectural features which support "cascading", putting them together to create deeper "effective FIFOs." Still other features support "interlocked paralleling," to create wider "effective FIFOs."

FIGURE 7. INTERLOCKED PARALLEL 36-BIT-WIDE CONFIGURATION FOR TWO QS722X5-FAMILY FIFOS.

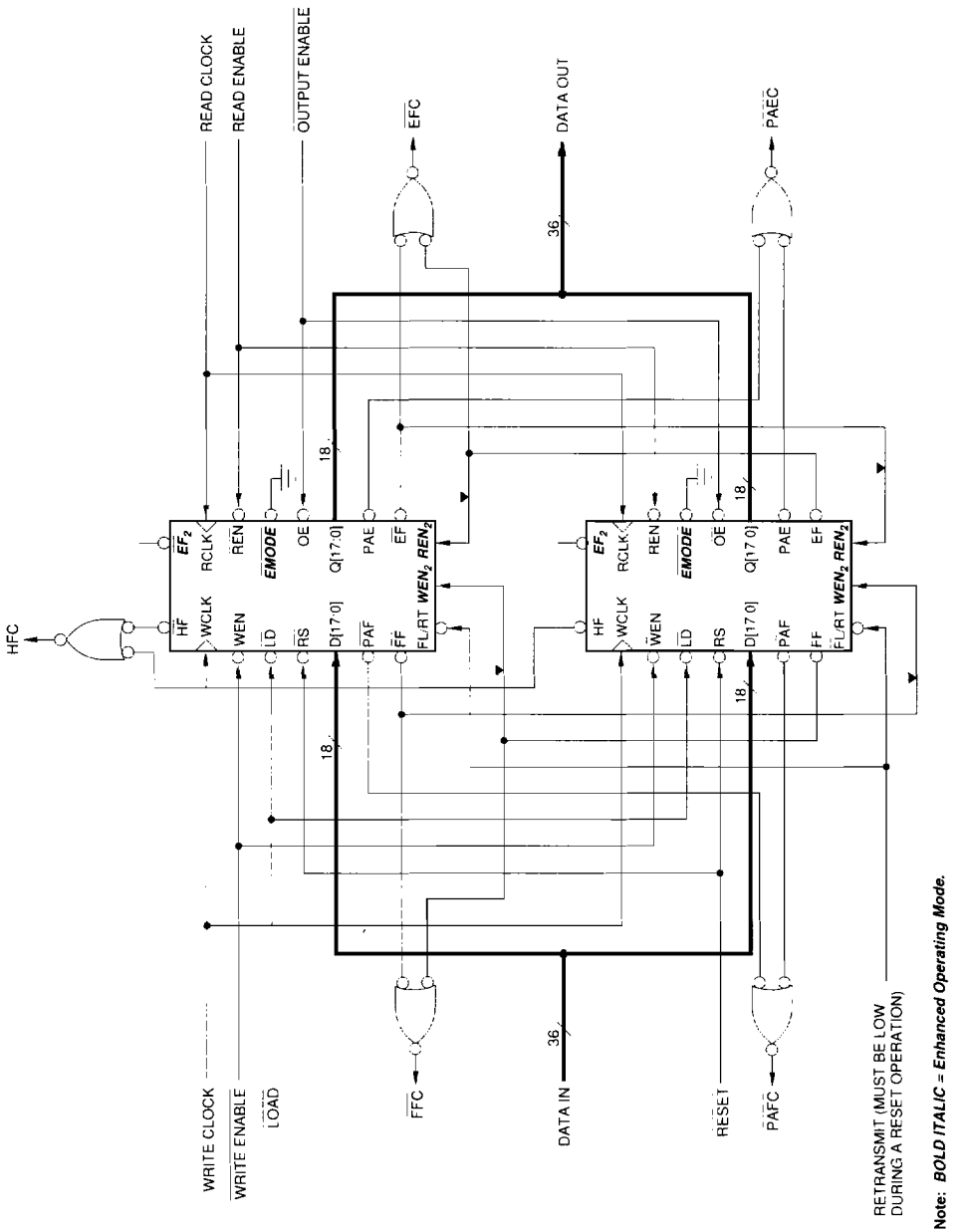
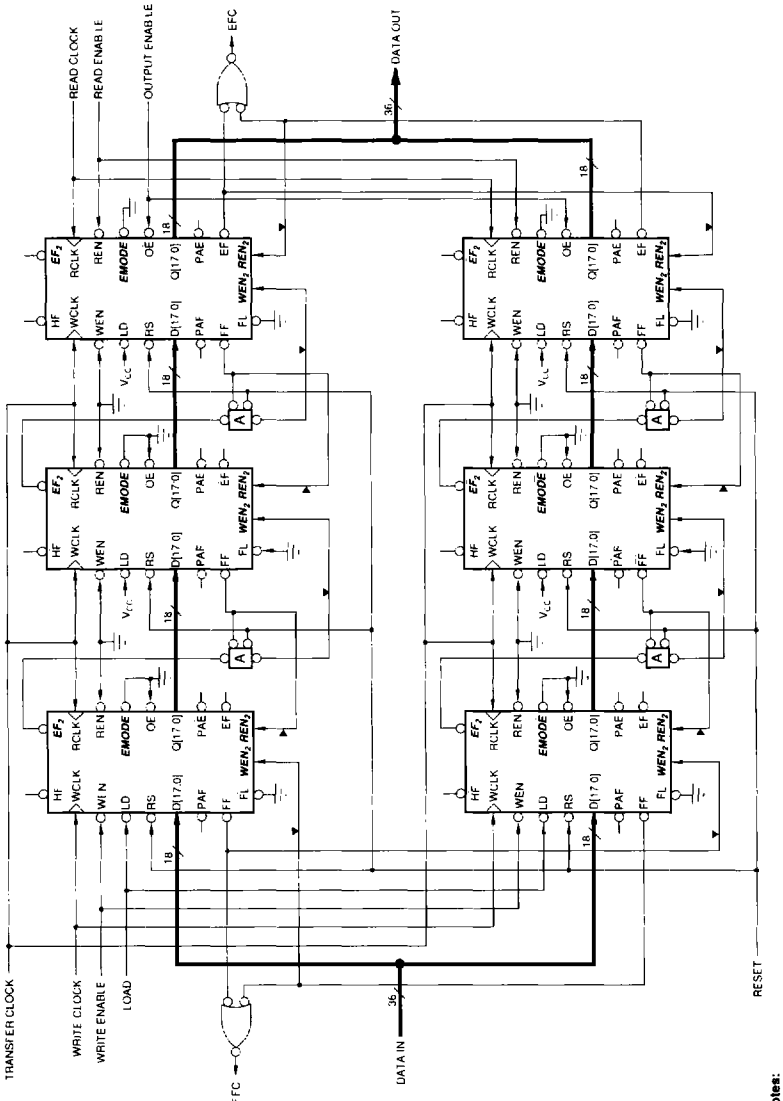


FIGURE 8. INTERLOCKED PARALLEL AND PIPELINED DEPTH-CASCADED 2 X 3 ARRAY OF QS772X5 FAMILY FIFOS



Notes:

1. The transfer clock may be any free-running clock. However, it is recommended that the faster of the write clock and the read clock 2 be used. If both of these are free-running clocks.
2. Block "A" contains the circuit shown in Figure 29b.

BOLD ITALIC = Enhanced Operating Mode.