NTF5P03T3

Preferred Device

Power MOSFET 5.2 Amps, 30 Volts

P−Channel SOT−223

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature SOT−223 Surface Mount Package
- Avalanche Energy Specified
- Pb−Free Package is Available

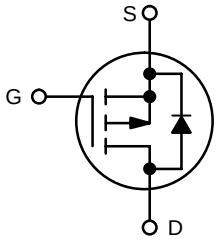
Applications

- DC−DC Converters
- Power Management
- Motor Controls
- Inductive Loads
- Replaces MMFT5P03HD

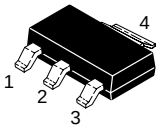
ON Semiconductor®

http://onsemi.com

5.2 AMPERES, 30 VOLTS
$R_{DS(on)}$ = 100 mΩ

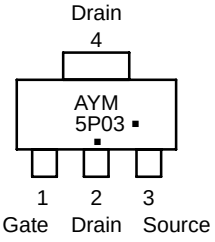


P−Channel MOSFET



SOT−223
CASE 318E
STYLE 3

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location
Y = Year
M = Date Code
5P03 = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTF5P03T3	SOT−223	4000/Tape & Reel
NTF5P03T3G	SOT−223 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)
Negative sign for P−Channel devices omitted for clarity

Rating		Symbol	Max	Unit
Drain−to−Source Voltage		V_{DSS}	−30	V
Drain−to−Gate Voltage (R_{GS} = 1.0 MΩ)		V_{DGR}	−30	V
Gate−to−Source Voltage − Continuous		V_{GS}	± 20	V
1 sq in FR−4 or G−10 PCB	Thermal Resistance − Junction to Ambient Total Power Dissipation @ T_A = 25°C Linear Derating Factor Drain Current − Continuous @ T_A = 25°C	R_{THJA} P_D I_D	40 3.13 25 −5.2	°C/W Watts mW/°C A
10 seconds	Continuous @ T_A = 70°C Pulsed Drain Current (Note 1)	I_D I_{DM}	−4.1 −26	A A
Minimum FR−4 or G−10 PCB	Thermal Resistance − Junction to Ambient Total Power Dissipation @ T_A = 25°C Linear Derating Factor Drain Current − Continuous @ T_A = 25°C	R_{THJA} P_D I_D	80 1.56 12.5 −3.7	°C/W Watts mW/°C A
10 seconds	Continuous @ T_A = 70°C Pulsed Drain Current (Note 1)	I_D I_{DM}	−2.9 −19	A A
Operating and Storage Temperature Range		T_J, T_{stg}	− 55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = −30 Vdc, V_{GS} = −10 Vdc, Peak I_L = −12 Apk, L = 3.5 mH, R_G = 25 Ω)		E_{AS}	250	mJ

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Repetitive rating; pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 2 and 4) (V_{GS} = 0 Vdc, I_D = −0.25 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	−30 −	− −28	− −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = −24 Vdc, V_{GS} = 0 Vdc) (V_{DS} = −24 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	− −	− −	−1.0 −25	μAdc
Gate−Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	± 100	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (Cpk ≥ 2.0) (Notes 2 and 4) (V_{DS} = V_{GS}, I_D = −0.25 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	−1.0 −	−1.75 3.5	−3.0 −	Vdc mV/°C
Static Drain−to−Source On−Resistance (Cpk ≥ 2.0) (Notes 2 and 4) (V_{GS} = −10 Vdc, I_D = −5.2 Adc) (V_{GS} = −4.5 Vdc, I_D = −2.6Adc)		$R_{DS(on)}$	−	76 107	100 150	mΩ
Forward Transconductance (Note 2) (V_{DS} = −15 Vdc, I_D = −2.0 Adc)		g_{fs}	2.0	3.9	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = −25 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	−	500	950	pF
Output Capacitance		C_{oss}	−	153	440	
Transfer Capacitance		C_{rss}	−	58	140	
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	(V_{DD} = −15 Vdc, I_D = −4.0 Adc, V_{GS} = −10 Vdc, R_G = 6.0 Ω) (Note 2)	$t_{d(on)}$	−	10	24	ns
Rise Time		t_r	−	33	48	
Turn−Off Delay Time		$t_{d(off)}$	−	38	94	
Fall Time		t_f	−	20	92	
Turn−On Delay Time	(V_{DD} = −15 Vdc, I_D = −2.0 Adc, V_{GS} = −10 Vdc, R_G = 6.0 Ω) (Note 2)	$t_{d(on)}$	−	16	38	ns
Rise Time		t_r	−	45	110	
Turn−Off Delay Time		$t_{d(off)}$	−	23	60	
Fall Time		t_f	−	24	80	
Gate Charge	(V_{DS} = −24 Vdc, I_D = −4.0 Adc, V_{GS} = −10 Vdc) (Note 2)	Q_T	−	15	38	nC
		Q_1	−	1.6	−	
		Q_2	−	3.5	−	
		Q3	−	2.6	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = −4.0 Adc, V_{GS} = 0 Vdc) (I_S = −4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C) (Note 2)	V_{SD}	− −	−1.1 −0.89	−1.5 −	Vdc
Reverse Recovery Time	(I_S = −4.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 2)	t_{rr}	−	34	−	ns
		t_a	−	20	−	
		t_b	−	14	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.036	−	μC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. Switching characteristics are independent of operating junction temperatures.
4. Reflects typical values. $\text{Cpk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

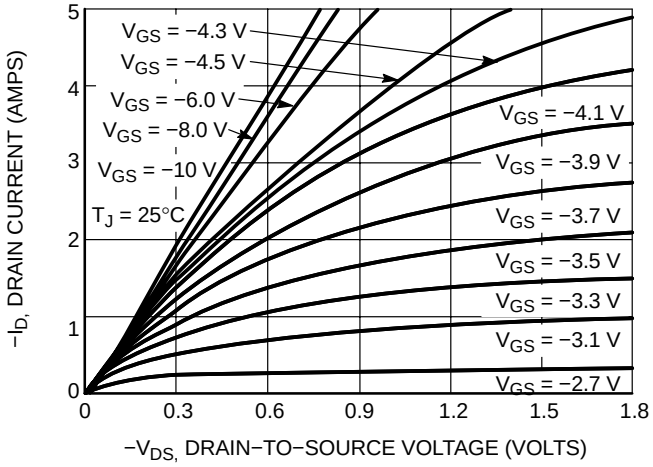


Figure 1. On−Region Characteristics

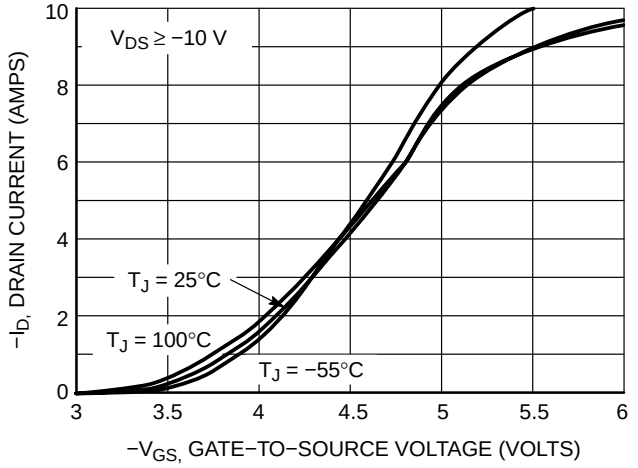


Figure 2. Transfer Characteristics

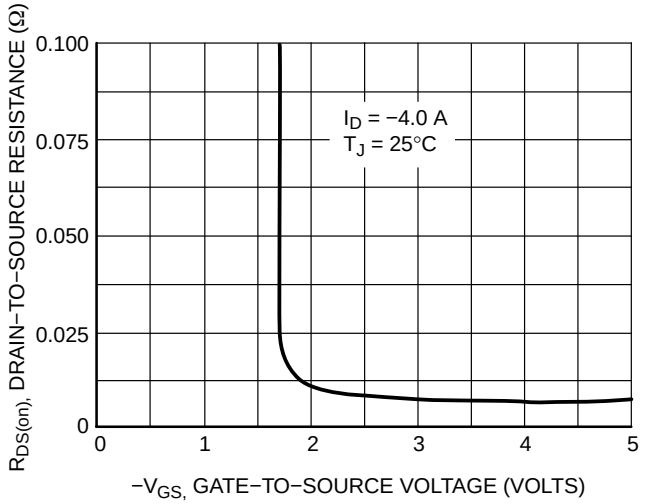


Figure 3. On−Resistance versus Gate−to−Source Voltage

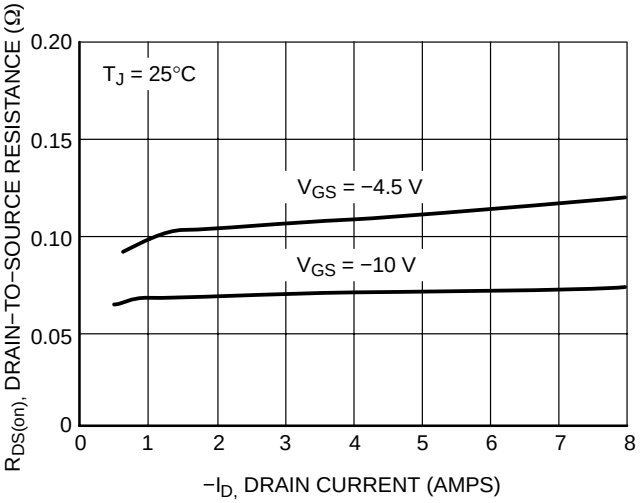


Figure 4. On−Resistance versus Drain Current and Gate Voltage

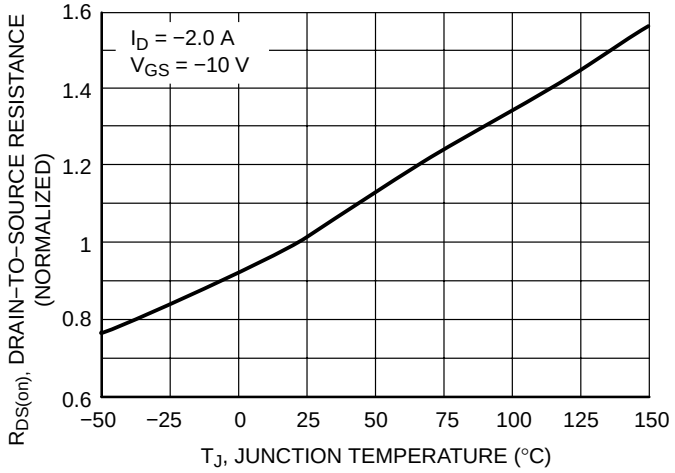


Figure 5. On−Resistance Variation with Temperature

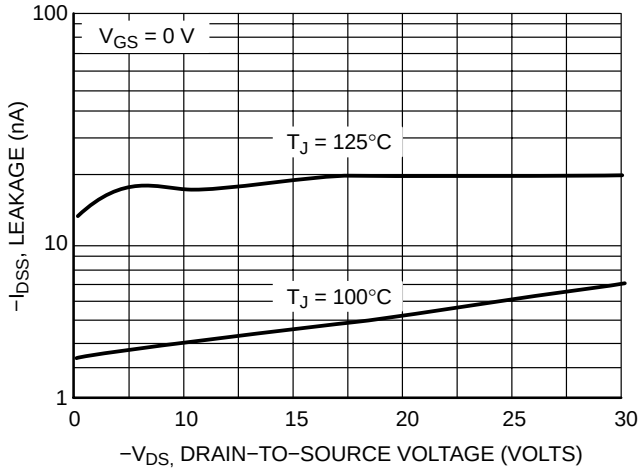


Figure 6. Drain−to−Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

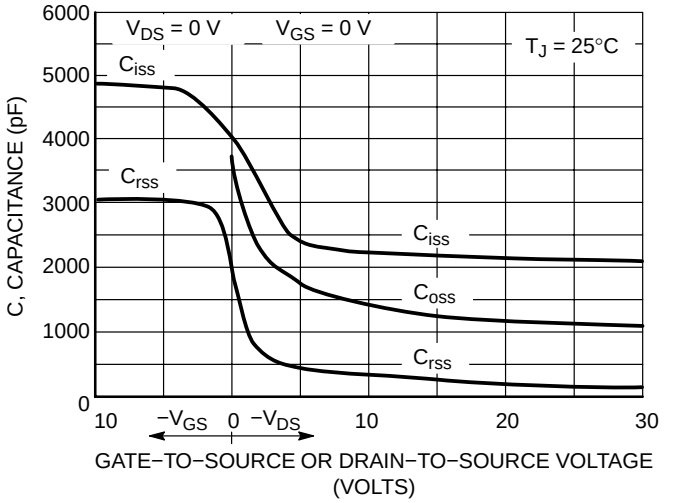


Figure 7. Capacitance Variation

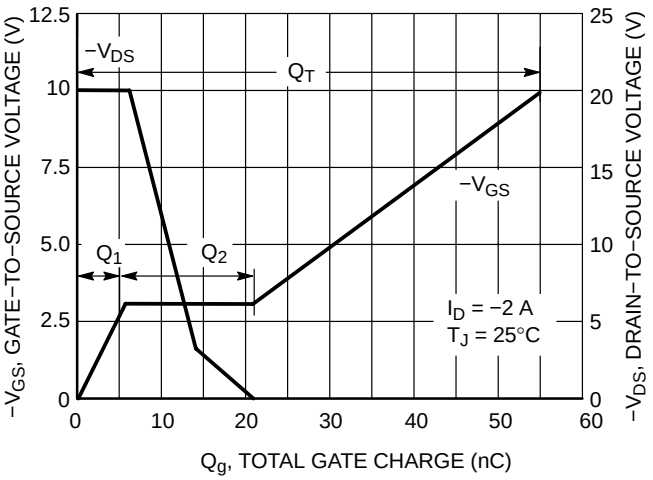


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

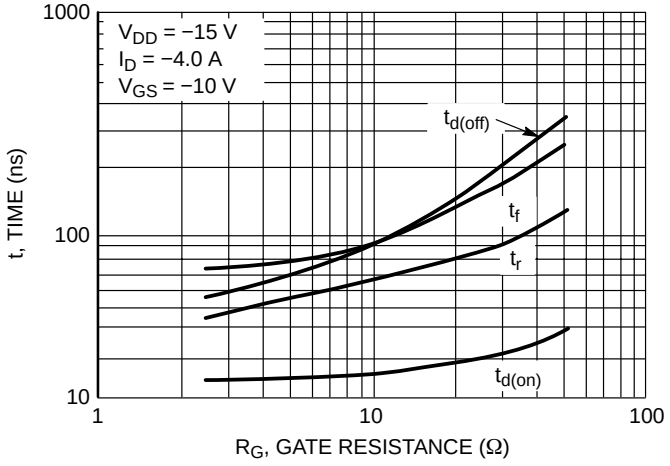


Figure 9. Resistive Switching Time Variation versus Gate Resistance

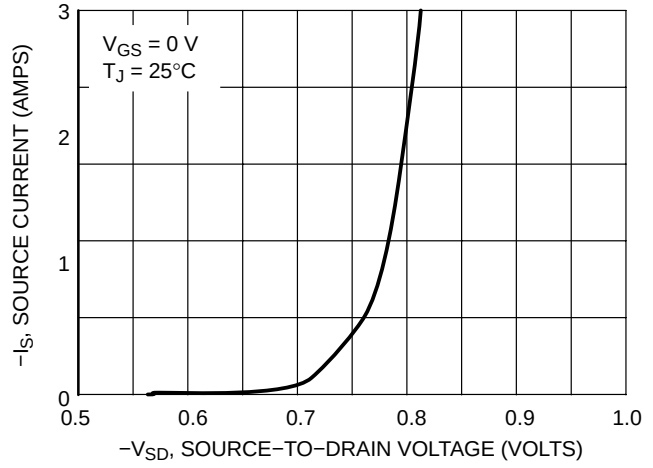
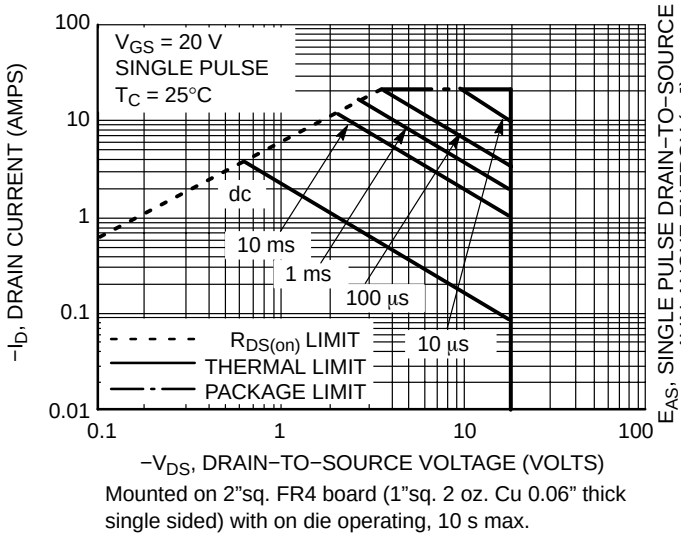


Figure 10. Diode Forward Voltage versus Current



Mounted on 2”sq. FR4 board (1”sq. 2 oz. Cu 0.06” thick single sided) with on die operating, 10 s max.

Figure 11. Maximum Rated Forward Biased Safe Operating Area

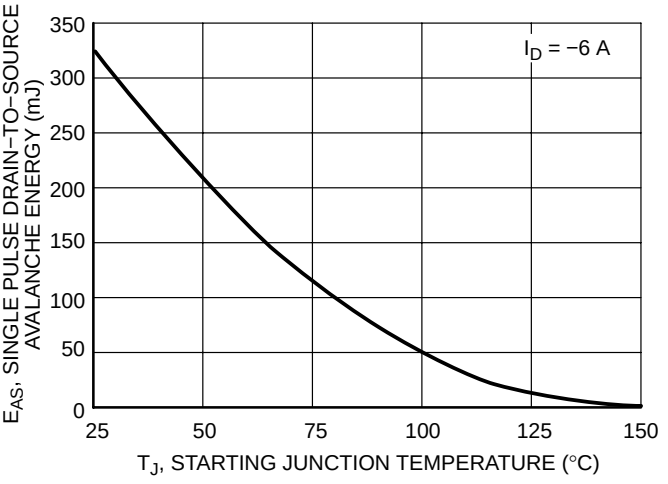


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

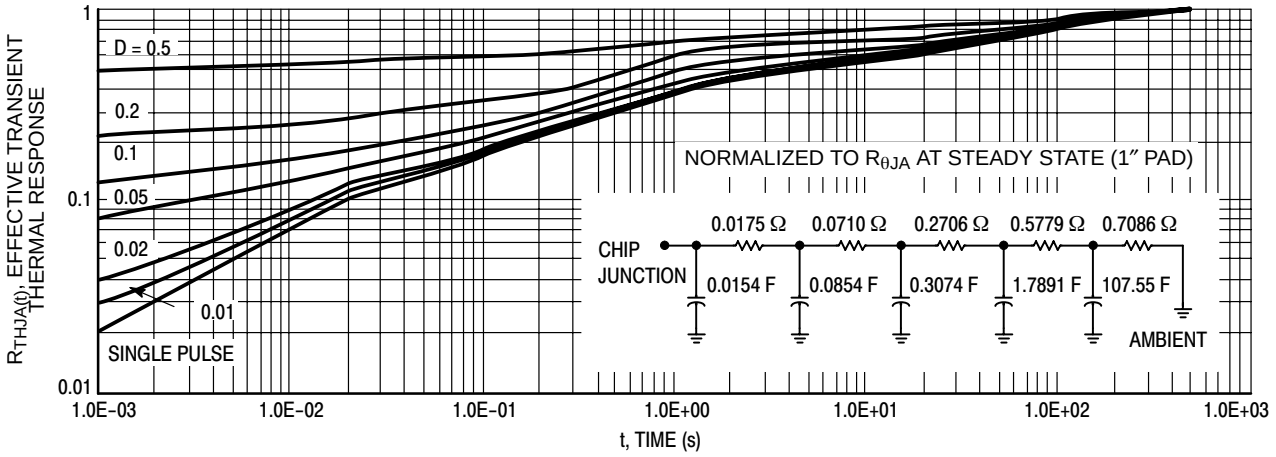
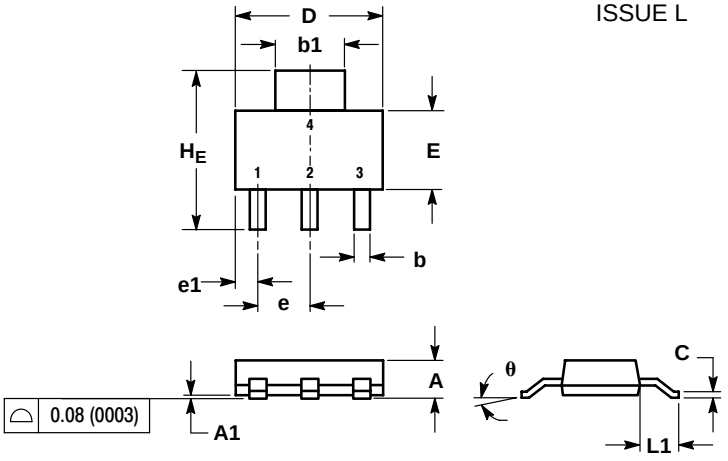


Figure 13. FET Thermal Response

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE L

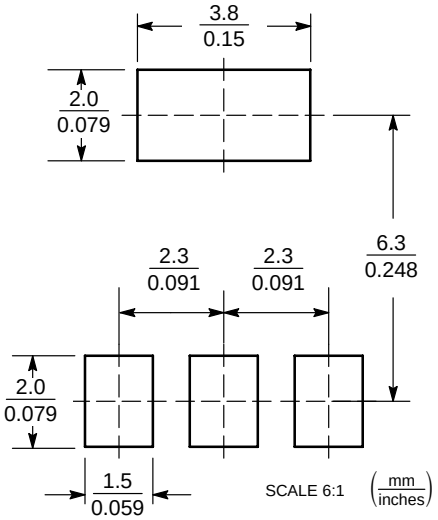


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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