# Programmable Maximum Power Point Tracking Controller for Photovoltaic Solar Panels

**Check for Samples: SM72442**

## FEATURES

- **Renewable Energy Grade**
- **Programmable Maximum Power Point Tracking**
- **Photovoltaic Solar Panel Voltage and Current Diagnostic**
- **Single Inductor Four Switch Buck-Boost Converter Control**
- **I2C Interface for Communication**
- **VOUT Overvoltage Protection**
- **Over-Current Protection**
- **Package: TSSOP-28**

## DESCRIPTION

The SM72442 is a programmable MPPT controller capable of controlling four PWM gate drive signals for a 4-switch buck-boost converter. The SM72442 also features a proprietary algorithm called Panel Mode which allows for the panel to be connected directly to the output of your power optimizer circuit. Along with the SM72295 (Photovoltaic Full Bridge Driver), it creates a solution for an MPPT configured DC-DC converter with efficiencies up to 99.5%. Integrated into the chip is an 8-channel, 12 bit A/D converter used to sense input and output voltages and currents, as well as board configuration. Externally programmable values include maximum output voltage and current as well as different settings forslew rate, soft-start and Panel Mode.

## Block Diagram

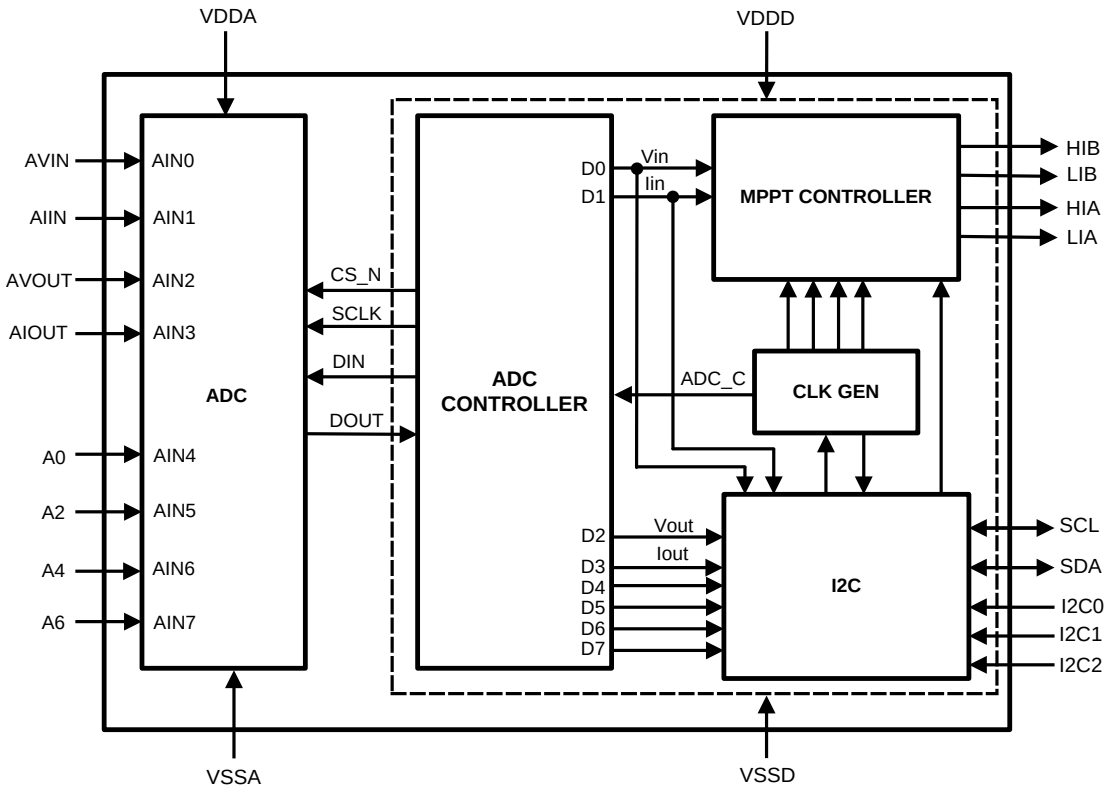



**Figure 1. Block Diagram**

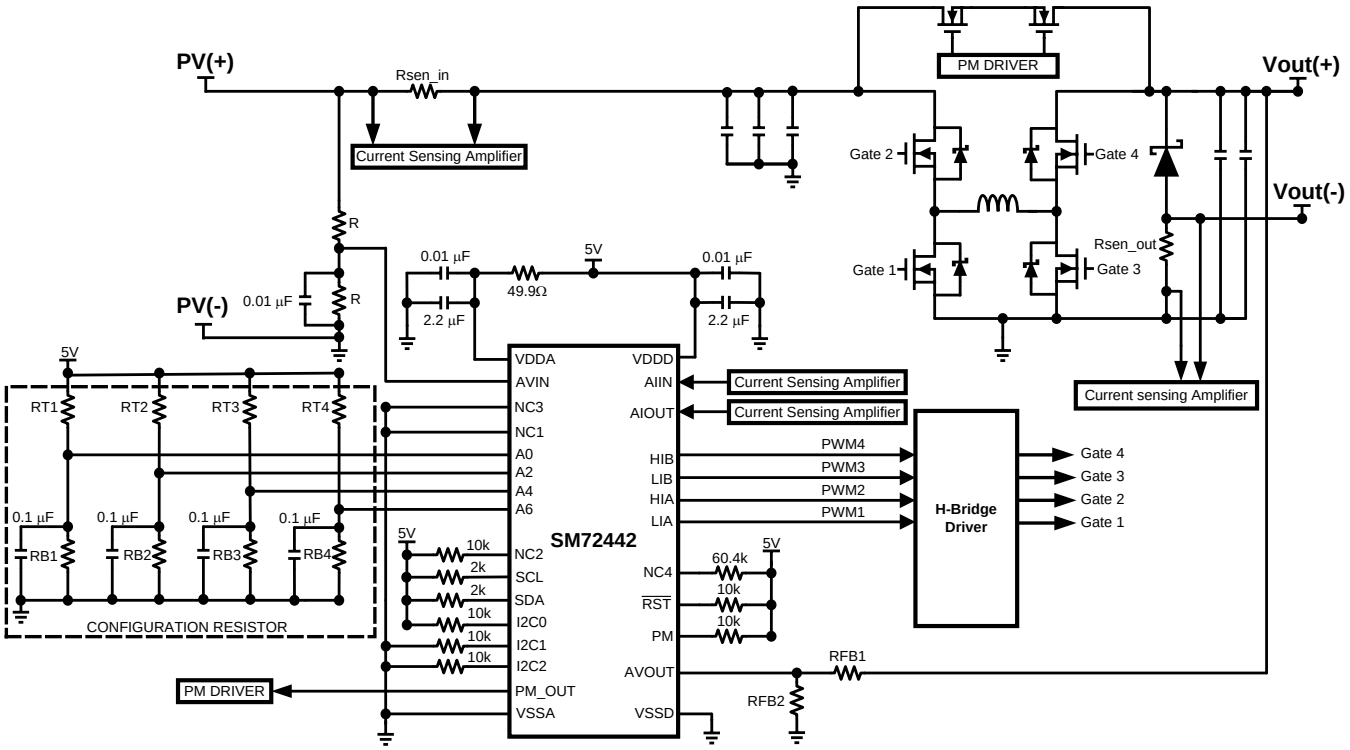



**Figure 2. Typical Application Circuit**

## Connection Diagram

**Top View**

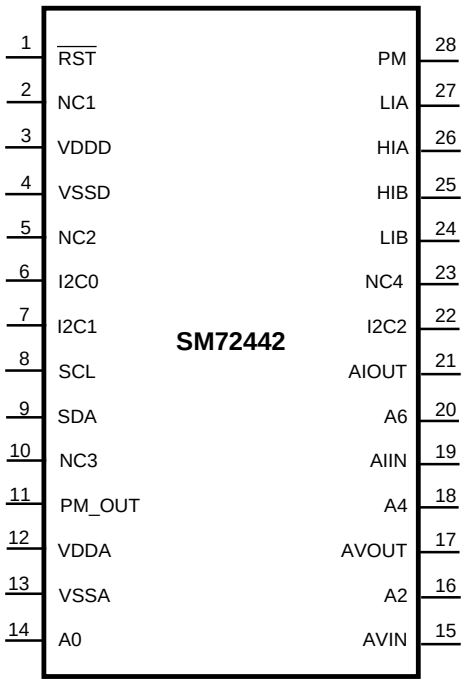



**Figure 3. TSSOP-28 Package**
**See Package Number PW0028A**

## PIN DESCRIPTIONS

| Pin | Name | Description |
|---|---|---|
| 1 | $\overline{RST}$ | Active low signal. External reset input signal to the digital circuit. |
| 2 | NC1 | Reserved for test only. This pin should be grounded. |
| 3 | VDDD | Digital supply voltage. This pin should be connected to a 5V supply, and bypassed to VSSD with a 0.1 µF monolithic ceramic capacitor. |
| 4 | VSSD | Digital ground. The ground return for the digital supply and signals. |
| 5 | NC2 | No Connect. This pin should be pulled up to the 5V supply using 10k resistor. |
| 6 | I2C0 | Addressing for I2C communication. |
| 7 | I2C1 | Addressing for I2C communication. |
| 8 | SCL | I2C clock. |
| 9 | SDA | I2C data. |
| 10 | NC3 | Reserved for test only. This pin should be grounded. |
| 11 | PM_OUT | When Panel Mode is active, this pin will output a 400 kHz square wave signal with amplitude of 5V. Otherwise, it stays low. |
| 12 | VDDA | Analog supply voltage. This voltage is also used as the reference voltage. This pin should be connected to a 5V supply, and bypassed to VSSA with a 1 µF and 0.1 µF monolithic ceramic capacitor. |
| 13 | VSSA | Analog ground. The ground return for the analog supply and signals. |
| 14 | A0 | A/D Input Channel 0. Connect a resistor divider to 5V supply to set the maximum output voltage. Please refer to the application section for more information on setting the resistor value. |
| 15 | AVIN | Input voltage sensing pin. |
| 16 | A2 | A/D Input Channel 2. Connect a resistor divider to a 5V supply to set the condition to enter and exit Panel Mode (PM). Refer to configurable modes for SM72442 in the application section. |
| 17 | AVOUT | Output voltage sensing pin. |
| 18 | A4 | A/D Input Channel 4. Connect a resistor divider to a 5V supply to set the maximum output current. Please refer to the application section for more information on setting the resistor value. |
| 19 | AIIN | Input current sensing pin. |
| 20 | A6 | A/D Input Channel 6. Connect a resistor divider to a 5V supply to set the output voltage slew rate and various PM configurations. Refer to configurable modes for SM72442 in the application section. |
| 21 | AIOUT | Output current sensing pin. |
| 22 | I2C2 | Addressing for I2C communication. |
| 23 | NC4 | No Connect. This pin should be connected with 60.4k pull-up resistor to 5V. |
| 24 | LIB | Low side boost PWM output. |
| 25 | HIB | High side boost PWM output. |
| 26 | HIA | High side buck PWM output. |
| 27 | LIA | Low side buck PWM output. |
| 28 | PM | Panel Mode Pin. Active low. Pulling this pin low will force the chip into Panel Mode. |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)

| | | |
|---|---|---|
| Analog Supply Voltage $V_A$ (VDDA - VSSA) | | -0.3 to 6.0V |
| Digital Supply Voltage $V_D$ (VDDD - VSSD) | | -0.3 to $V_A$ +0.3V max 6.0V |
| Voltage on Any Pin to GND | | -0.3 to $V_A$ +0.3V |
| Input Current at Any Pin (2) | | ±10 mA |
| Package Input Current (2) | | ±20 mA |
| Storage Temperature Range | | -65°C to +150°C |
| ESD Rating (3) | Human Body Model | 2 kV |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

## Recommended Operating Conditions

| | |
|---|---|
| Operating Temperature | -40°C to 105°C |
| $V_A$ Supply Voltage | +4.75V to +5.25V |
| $V_D$ Supply Voltage | +4.75V to $V_A$ |
| Digital Input Voltage | 0 to $V_A$ |
| Analog Input Voltage | 0 to $V_A$ |
| Junction Temperature | -40°C to 125°C |

## Electrical Characteristics

Specifications in standard typeface are for $T_J$ = 25°C, and those in boldface type apply over the full operating junction temperature range(1)

| Parameter | | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **ANALOG INPUT CHARACTERISTICS** | | | | | | |
| AVin, Alin AVout, Alout | Input Range | | - | 0 to $V_A$ | - | V |
| $I_{DCL}$ | DC Leakage Current | | - | - | **±1** | µA |
| $C_{INA}$ | Input Capacitance(2) | Track Mode | - | 33 | - | pF |
| | | Hold Mode | - | 3 | - | pF |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| $V_{IL}$ | Input Low Voltage | | - | - | **0.8** | V |
| $V_{IH}$ | Input High Voltage | | **2.8** | - | - | V |
| $C_{IND}$ | Digital Input Capacitance(2) | | - | 2 | **4** | pF |
| $I_{IN}$ | Input Current | | - | ±0.01 | **±1** | µA |
| **DIGITAL OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{OH}$ | Output High Voltage | $I_{SOURCE}$ = 200 µA $V_A = V_D$ = 5V | **$V_D$ - 0.5** | - | - | V |
| $V_{OL}$ | Output Low Voltage | $I_{SINK}$ = 200 µA to 1.0 mA $V_A = V_D$ = 5V | - | - | **0.4** | V |
| $I_{OZH}$ , $I_{OZL}$ | Hi-Impedance Output Leakage Current | $V_A = V_D$ = 5V | | | **±1** | µA |
| $C_{OUT}$ | Hi-Impedance Output Capacitance(2) | | | 2 | **4** | pF |
| **POWER SUPPLY CHARACTERISTICS ($C_L$ = 10 pF)** | | | | | | |
| $V_A$ ,$V_D$ | Analog and Digital Supply Voltages | $V_A \geq V_D$ | **4.75** | 5 | **5.25** | V |
| $I_A + I_D$ | Total Supply Current | $V_A = V_D$ = 4.75V to 5.25V | - | 11.5 | **15** | mA |
| $P_C$ | Power Consumption | $V_A = V_D$ = 4.75V to 5.25V | | 57.5 | **78.75** | mW |

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Not tested. Ensured by design.

## Electrical Characteristics (continued)

Specifications in standard typeface are for $T_J$ = 25°C, and those in boldface type apply over the full operating junction temperature range(1)

| Parameter | | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **PWM OUTPUT CHARACTERISTICS** | | | | | | |
| $f_{PWM}$ | PWM switching frequency | | | 220 | | kHz |

## Operation Description

### OVERVIEW

The SM72442 is a programmable MPPT controller capable of outputting four PWM gate drive signals for a 4-switch buck-boost converter with an independent Panel Mode. The typical application circuit is shown in Figure 2.

The SM72442 uses an advanced digital controller to generate its PWM signals. A maximum power point tracking (MPPT) algorithm monitors the input current and voltage and controls the PWM duty cycle to maximize energy harvested from the photovoltaic module. MPPT performance is very fast. Convergence to the maximum power point of the module typically occurs within 0.01s. This enables the controller to maintain optimum performance under fast-changing irradiance conditions.

Transitions between buck, boost, and Panel Mode are smoothed and advanced digital PWM dithering techniques are employed to increase effective PWM resolution. Output voltage and current limiting functionality are integrated into the digital control logic. The controller is capable of handling both shorted and no-load conditions and will recover smoothly from both conditions.

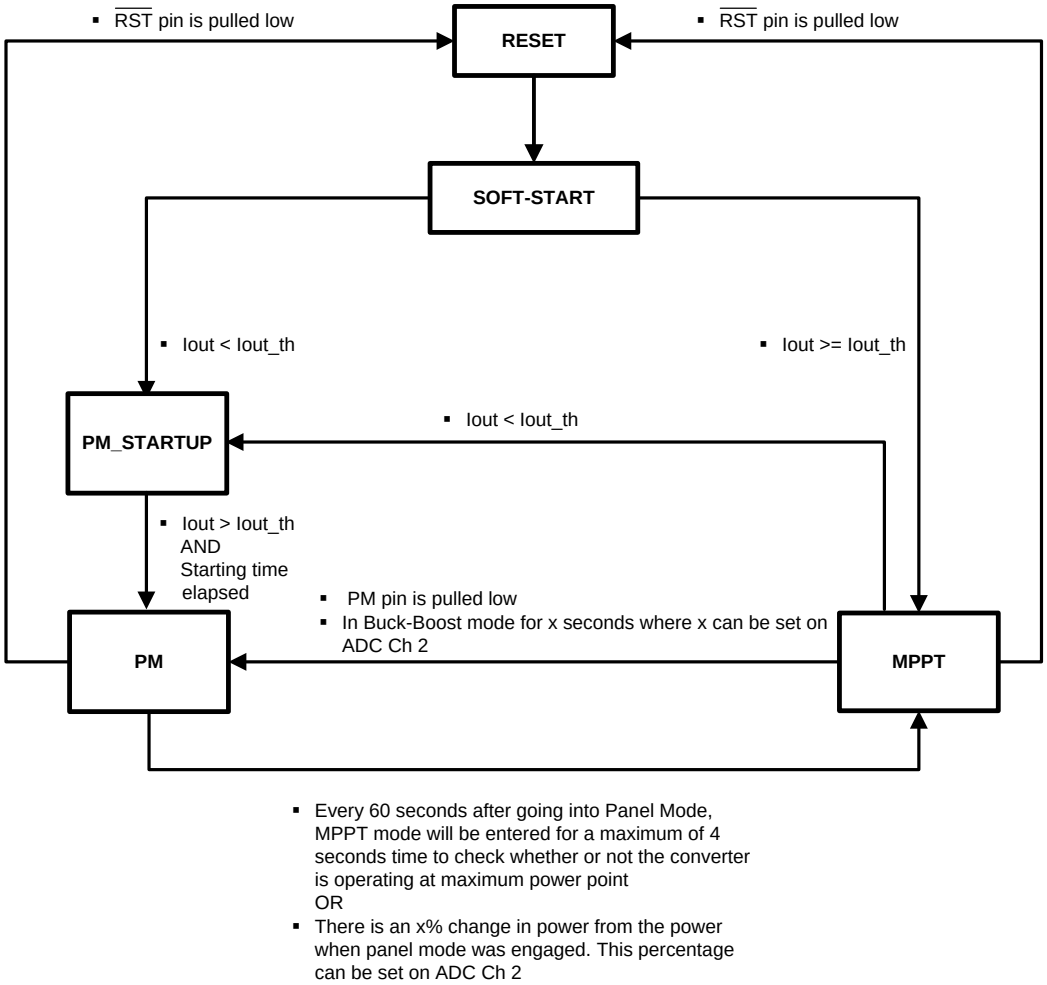



**Figure 4. High Level State Diagram for Startup**

## STARTUP

SM72442 has a soft start feature that will ramp its output voltage for a fixed time of 250ms.

If no output current is detected during soft-start time, the chip will then be in Panel Mode for 60 seconds. A counter will start once the minimum output current threshold is met (set by ADC input channel 4). During these 60 seconds, any variation on the output power will not cause the chip to enter MPPT mode. Once 60 seconds have elapsed, at a certain power level variation at the output (set by ADC input channel 2) will engage the chip in MPPT mode.

If the output current exceeded the current threshold set at A/D Channel 6 (A6) during soft-start, the chip will then engage in MPPT mode.

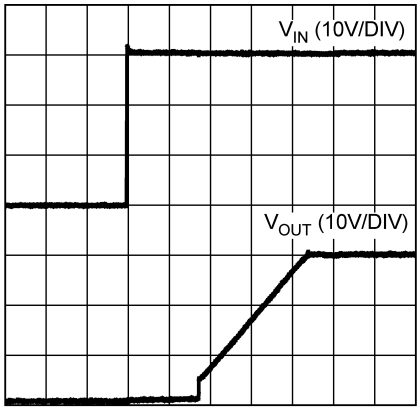



**Figure 5. Startup Sequence**

## MAXIMUM OUTPUT VOLTAGE

Maximum output voltage on the SM72442 is set by resistor divider ratio on pin A0. (Please refer to Figure 2 Typical Application Circuit).

$$V_{OUT\_MAX} = 5 \times \frac{RB1}{RT1 + RB1} \times \frac{(RFB1 + RFB2)}{RFB2} \quad (1)$$

where

- RT1 and RB1 are the resistor divider on the ADC pin A0
- RFB1 and RFB2 are the output voltage sense resistors. A typical value for RFB2 is about 2 kΩ

## CURRENT LIMIT SETTING

Maximum output current can be set by changing the resistor divider on A4 (pin 18). Refer to Figure 2. Overcurrent at the output is detected when the voltage on AIOUT (pin 21) equals the voltage on A4 (pin 18). The voltage on A4 can be set by a resistor divider connected to 5V whereas the voltage on AIOUT can be set by a current sense amplifier.

## AVIN PIN

AVIN is an A/D input to sense the input voltage of the SM72442. A resistor divider can be used to scale max voltage to about 4V, which is 80% of the full scale of the A/D input.

## CONFIGURABLE SETTINGS

A/D pins A0, A2, A4, and A6 are used to configure the behavior of the SM72442 by adjusting the voltage applied to them. One way to do this is through resistor dividers as shown in Figure 2, where RT1 to RT4 should be in the range of 20 kΩ.

Different conditions to enter and exit Panel Mode can be set on the ADC input channel 2. Listed below are different conditions that a user can select on pin A2. “1:1” refers to the state in which the DC/DC converter operates with its output voltage equal to its input voltage (also referred to as “Buck-Boost” mode in Figure 4.)

| A2 | Entering Panel Mode | Exiting Panel Mode |
|---|---|---|
| 4.69 V | 2s in 1:1 Mode | 3.1% power variation |
| 4.06 V | 1s in 1:1 Mode | 3.1% power variation |
| 3.44 V | 0.4s in 1:1 Mode | 3.1% power variation |
| 2.81 V | 0.2s in 1:1 Mode | 3.1% power variation |
| 2.19 V | 2s in 1:1 Mode | 1.6% power variation |
| 1.56 V | 1s in 1:1 Mode | 1.6% power variation |
| 0.94 V | 0.4s in 1:1 Mode | 1.6% power variation |
| 0.31 V | 0.2s in 1:1 Mode | 1.6% power variation |

The user can also select the output voltage slew rate, minimum current threshold and duration of Panel Mode after the soft-start period has finished, by changing the voltage level on pin A6 which is the input of ADC channel 6.

| A6 | Output Voltage Slew Rate Limit | Starting Panel Mode Time | MPPT Exit Threshold | MPPT Start Threshold | Starting boost ratio |
|---|---|---|---|---|---|
| 4.69 V | Slow | Not applicable | 0 mA | 0 mA | 1:1 |
| 4.06 V | Slow | 60s | 75mA | 125mA | 1:1 |
| 3.44 V | Slow | 0s | 300mA | 500mA | 1:1 |
| 2.81 V | Slow | 120s | 300mA | 500mA | 1:1 |
| 2.19 V | Slow | Not applicable | 300mA | 500mA | 1:1.2 |
| 1.56 V | Slow | 60s | 300mA | 500mA | 1:1 |
| 0.94 V | Fast | 60s | 300mA | 500mA | 1:1 |
| 0.31 V | No slew rate limit | 60s | 300mA | 500mA | 1:1 |

## PARAMETER DEFINITIONS

**Output Voltage Slew Rate Limit Settling Time:** Time constant of the internal filter used to limit output voltage change. For fast slew rate, every 1V increase, the output voltage will be held for 30 ms whereas in a slow slew rate, the output voltage will be held for 62 ms for every 1V increase. (See Figure 6).

**Starting PM Time:** After initial power-up or reset, the output soft-starts and then enters Panel Mode for this amount of time.

**MPPT Exit Threshold and MPPT Start Threshold:** These are the hysteretic thresholds for Iout_th.

**Starting Boost Ratio** – This is the end-point of the soft-start voltage ramp. 1:1 ratio means it stops when Vout = Vin, 1:1.2 means it stops when Vout = 1.2 x Vin.

## PANEL MODE PIN (PM) PIN

The SM72442 can be forced into Panel Mode by pulling the PM pin low. One sample application is to connect this pin to the output of an external temperature sensor; therefore whenever an over-temperature condition is detected the chip will enter a Panel Mode.

Once Panel Mode is enabled either when buck-boost mode is entered for a certain period of time (adjustable on channel 2 of ADC) or when PM is pulled low, the PM_OUT pin will output a 400 kHz square wave signal. Using a gate driver and transformer, this square wave signal can then be used to drive a Panel Mode FET as shown in Figure 7.

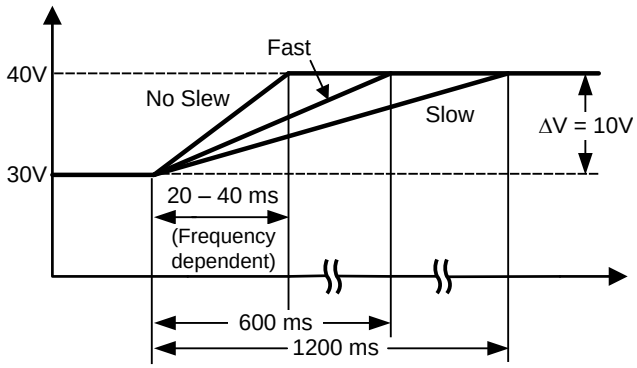



**Figure 6. Slew Rate Limitation Circuit**

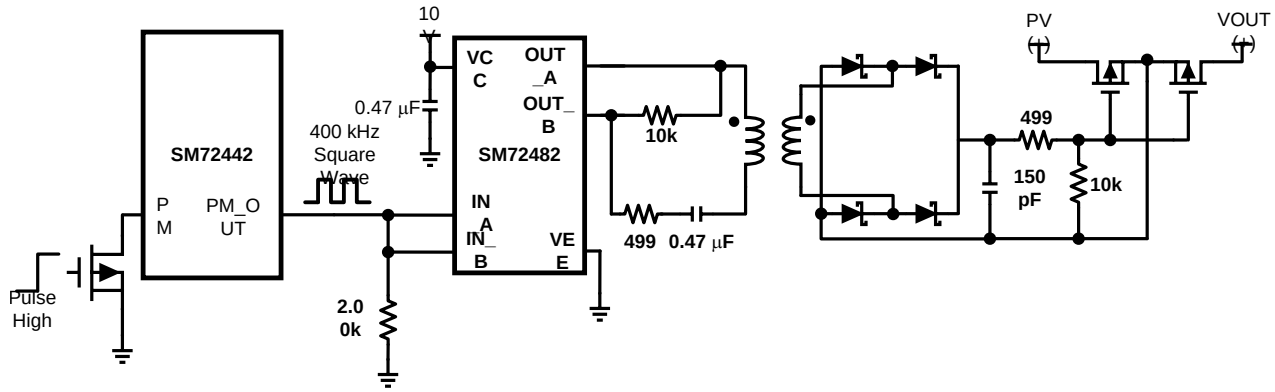



**Figure 7. Sample Application for Panel Mode Operation**

## RESET PIN

When the reset pin is pulled low, the chip will cease its normal operation and turn-off all of its PWM outputs including the output of PM_OUT pin. Below is an oscilloscope capture of a forced reset condition.

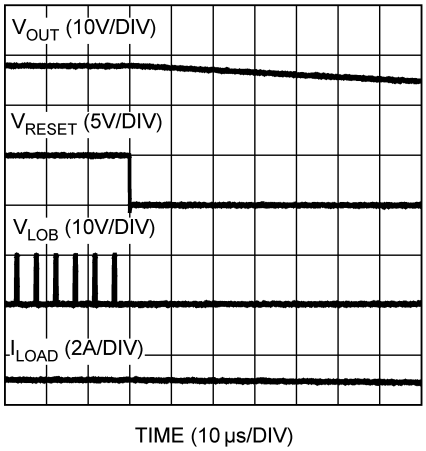



**Figure 8. Forced Reset Condition**

As seen in Figure 8, the initial value for output voltage and load current are 28V and 1A respectively. After the reset pin is grounded both the output voltage and load current decreases immediately. MOSFET switching on the buck-boost converter also stops immediately. VLOB indicates the low side boost output from the SM72295.

## ANALOG INPUT

An equivalent circuit for one of the ADC input channels is shown in Figure 9. Diode D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0V to $V_A$. Going beyond this range will cause the ESD diodes to conduct and result in erratic operation.

The capacitor C1 in Figure 9 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch; it is typically 500Ω. Capacitor C2 is the ADC sampling capacitor; it is typically 30 pF. The ADC will deliver best performance when driven by a low-impedance source (less than 100Ω). This is specially important when sampling dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonic and noise in the input. These filters are often referred to as anti-aliasing filters.

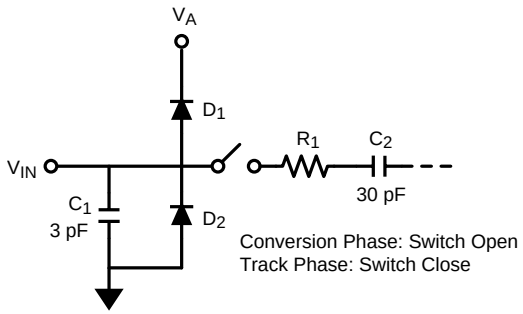



**Figure 9. Equivalent Input Circuit**

## DIGITAL INPUTS and OUTPUTS

The digital input signals have an operating range of 0V to $V_A$, where $V_A$ = VDDA – VSSA. They are not prone to latch-up and may be asserted before the digital supply $V_D$, where $V_D$ = VDDD – VSSD, without any risk. The digital output signals operating range is controlled by $V_D$. The output high voltage is $V_D$ – 0.5V (min) while the output low voltage is 0.4V (max).

## SDA and SCL OPEN DRAIN OUTPUT

SCL and SDA output is an open-drain output and does not have internal pull-ups. A “high” level will not be observed on this pin until pull-up current is provided by some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors; load capacitance, trace length, etc. A typical value of pull- up resistor for SM72442 ranges from 2 kΩ to 10 kΩ. For more information, refer to the I2C Bus specification for selecting the pull-up resistor value . The SCL and SDA outputs can operate while being pulled up to 5V and 3.3V.

## I2C CONFIGURATION REGISTERS

The operation of the SM72442 can be configured through its I2C interface. Complete register settings for I2C lines are shown below.

**Table 1. reg0 Register Description**

| Bits | Field | Reset Value | R/W | Bit Field Description |
|---|---|---|---|---|
| 55:40 | RSVD | 16'h0 | R | Reserved for future use. |
| 39:30 | ADC6 | 10'h0 | R | Analog Channel 6 (slew rate detection time constant, see adc config worksheet) |
| 29:20 | ADC4 | 10'h0 | R | Analog Channel 4 (iout_max: maximum allowed output current) |
| 19:10 | ADC2 | 10'h0 | R | Analog Channel 2 (operating mode, see adc_config worksheet) |
| 9:0 | ADC0 | 10'h0 | R | Analog Channel 0 (vout_max: maximum allowed output voltage) |

**Table 2. reg1 Register Description**

| Bits | Field | Reset Value | R/W | Bit Field Description |
|---|---|---|---|---|
| 55:41 | RSVD | 15'h0 | R | Reserved for future use. |
| 40 | mppt_ok | 1'h0 | R | Internal mppt_start signal (test only) |
| 39:30 | Vout | 10'h0 | R | Voltage out |
| 29:20 | Iout | 10'h0 | R | Current out |
| 19:10 | Vin | 10'h0 | R | Voltage in |
| 9:0 | Iin | 10'h0 | R | Current in |

**Table 3. reg3 Register Description**

| Bits | Field | Reset Value | R/W | Bit Field Description |
|---|---|---|---|---|
| 55:47 | RSVD | 9'd0 | R/W | Reserved |
| 46 | overide_adcprog | 1'b0 | R/W | When set to 1'b1,the below overide registers used instead of ADC |
| 45 | RSVD | 1'b0 | R/W | Reserved |
| 44:43 | RSVD | 2'b01 | R/W | Reserved |
| 42 | power_thr_sel | 1'b0 | R/W | Register override alternative for ADC2[9] when reg3[46] is set ( 1/2^^5 or 1/2^^6 ) |
| 41:40 | bb_in_ptmode_sel | 2'd0 | R/W | Register override alternative for ADC2[8:7] when reg3[46] is set ( 5%,10%,25% or 50%) |
| 39:30 | iout_max | 10'd1023 | R/W | Register override alternative when reg3[46] is set for maximum current threshold instead of ADC ch4 |
| 29:20 | vout_max | 10'd1023 | R/W | Register override alternative when reg3[46] is set for maximum voltage threshold instead of ADC ch0 |
| 19:17 | tdoff | 3'h3 | R/W | Dead time Off Time |
| 16:14 | tdon | 3'h3 | R/W | Dead time On time |
| 13:5 | dc_open | 9'hFF | R/W | Open loop duty cycle (test only) |
| 4 | pass_through_sel | 1'b0 | R/W | Overrides PM pin 28 and use reg3[3] |
| 3 | pass_through_manual | 1'b0 | R/W | Control Panel Mode when pass_through_sel bit is 1'b1 |
| 2 | bb_reset | 1'b0 | R/W | Soft reset |
| 1 | clk_oe_manual | 1'b0 | R/W | Enable the PLL clock to appear on pin 5 |
| 0 | Open Loop operation | 1'b0 | R/W | Open Loop operation (MPPT disabled, receives duty cycle command from reg 3b13:5); set to 1 and then assert & deassert bb_reset to put the device in openloop (test only) |

**Table 4. reg4 Register Description**

| Bits | Field | Reset Value | R/W | Bit Field Description |
|---|---|---|---|---|
| 55:32 | RSVD | 24'd0 | R/W | Reserved |
| 31:24 | Vout offset | 8'h0 | R/W | Voltage out offset |
| 23:16 | Iout offset | 8'h0 | R/W | Current out offset |
| 15:8 | Vin offset | 8'h0 | R/W | Voltage in offset |
| 7:0 | Iin offset | 8'h0 | R/W | Current in offset |

**Table 5. reg5 Register Description**

| Bits | Field | Reset Value | R/W | Bit Field Description |
|---|---|---|---|---|
| 55:40 | RSVD | 15'd0 | R/W | Reserved |
| 39:30 | iin_hi_th | 10'd40 | R/W | Current in high threshold for start |
| 29:20 | iin_lo_th | 10'd24 | R/W | Current in low threshold for start |
| 19:10 | iout_hi_th | 10'd40 | R/W | Current out high threshold for start |
| 9:0 | iout_lo_th | 10'd24 | R/W | Current out low threshold for start |

Using the I2C port, the user will be able to control the duty cycle of the PWM signal. Input and output voltage and current offset can also be controlled using I2C on register 4. Control registers are available for additional flexibility.

The thresholds iin_hi_th, iin_lo_th, iout_hi_th, iout_lo_th, in reg5 are compared to the values read in by the ADC on the AIIN and AIOUT pins. Scaling is set by the scaling of the analog signal fed into AIIN and AIOUT. These 10–bit values determine the entry and exit conditions for MPPT.

## COMMUNICATING WITH THE SM72442

The SCL line is an input, the SDA line is bidirectional, and the device address can be set by I2C0, I2C1 and I2C2 pins. Three device address pins allow connection of up to 7 SM72444s to the same I2C master. A pull-up resistor (10k) to a 5V supply is used to set a bit 1 on the device address. Device addressing for slaves are as follows:

| I2C0 | I2C1 | I2C2 | Hex |
|---|---|---|---|
| 0 | 0 | 1 | 0x1 |
| 0 | 1 | 0 | 0x2 |
| 0 | 1 | 1 | 0x3 |
| 1 | 0 | 0 | 0x4 |
| 1 | 0 | 1 | 0x5 |
| 1 | 1 | 0 | 0x6 |
| 1 | 1 | 1 | 0x7 |

The data registers in the SM72442 are selected by the Command Register. The Command Register is offset from base address 0xE0. Each data register in the SM72442 falls into one of two types of user accessibility:

1) Read only (Reg0, Reg1)

2) Write/Read same address (Reg3, Reg4, Reg5)

There are 7 bytes in each register (56 bits), and data must be read and written in blocks of 7 bytes. Figure 10 depicts the ordering of the bytes transmitted in each frame and the bits within each byte. In the read sequence depicted in Figure 11 the data bytes are transmitted in Frames 5 through 11, starting from the LSByte, DATA1, and ending with MSByte, DATA7. In the write sequence depicted in Figure 12, the data bytes are transmitted in Frames 4 through 11. Only the 100kHz data rate is supported. Please refer to “The I2C Bus Specification” version 2.1 (Doc#: 939839340011) for more documentation on the I2C bus.

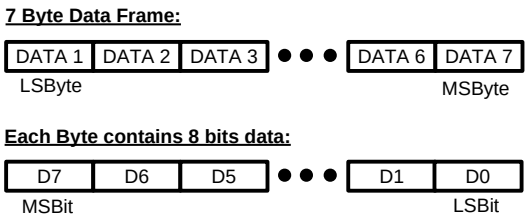



**Figure 10. Endianness Diagram**

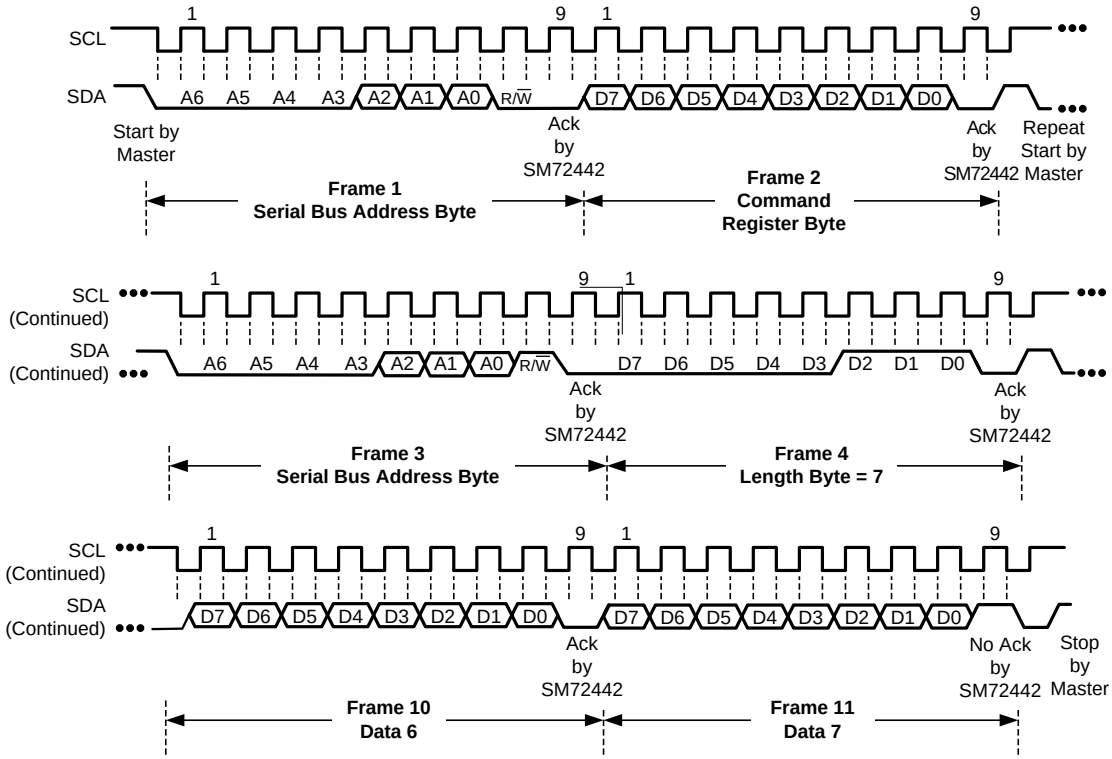



**Figure 11. I2C Read Sequence**

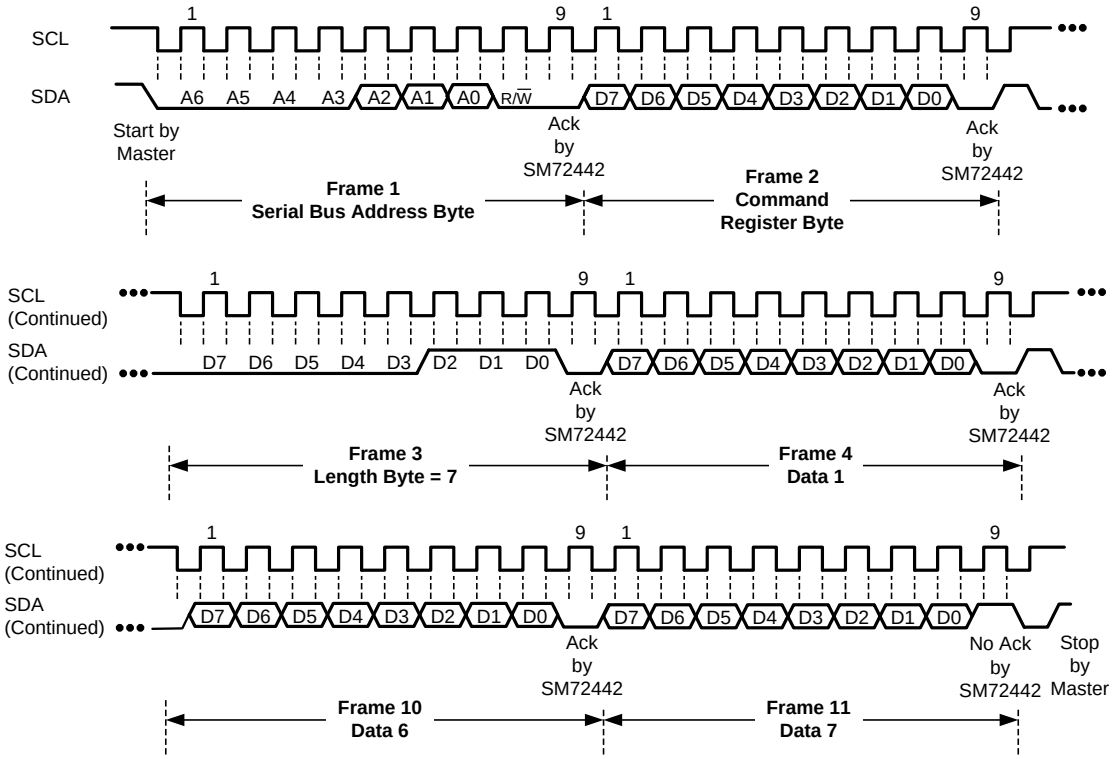



**Figure 12. I2C Write Sequence**

Noise coupling into digital lines greater than 400 mVp-p (typical hysteresis) and undershoot less than 500 mV GND, may prevent successful I2C communication with SM72442. I2C no acknowledge is the most common symptom, causing unnecessary traffic on the bus although the I2C maximum frequency of communication is rather low (400 kHz max), care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed board traces. Additional resistance can be added in series with the SDA and SCL lines to further help filter noise and ringing. Minimize noise coupling by keeping digital races out of switching power supply areas as well as ensuring that digital lines containing high speed data communications cross at right angles to the SDA and SCL lines.

## REVISION HISTORY

| Changes from Revision G (April 2013) to Revision H | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 15 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SM72442MT/NOPB | ACTIVE | TSSOP | PW | 28 | 48 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 125 | SO2442 | Samples |
| SM72442MTE/NOPB | ACTIVE | TSSOP | PW | 28 | 250 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 125 | SO2442 | Samples |
| SM72442MTX/NOPB | ACTIVE | TSSOP | PW | 28 | 2500 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 125 | SO2442 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

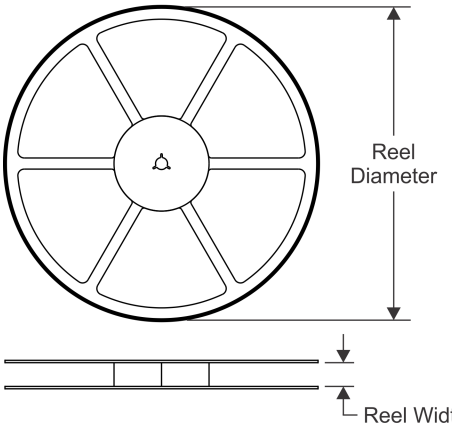
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

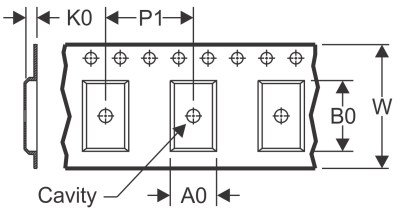
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

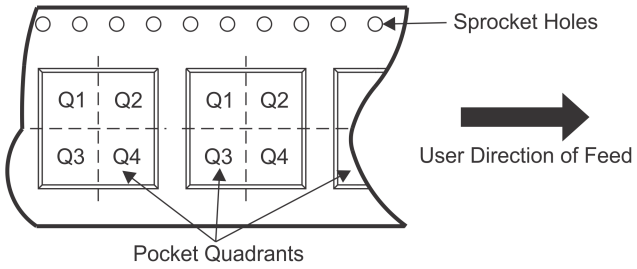



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

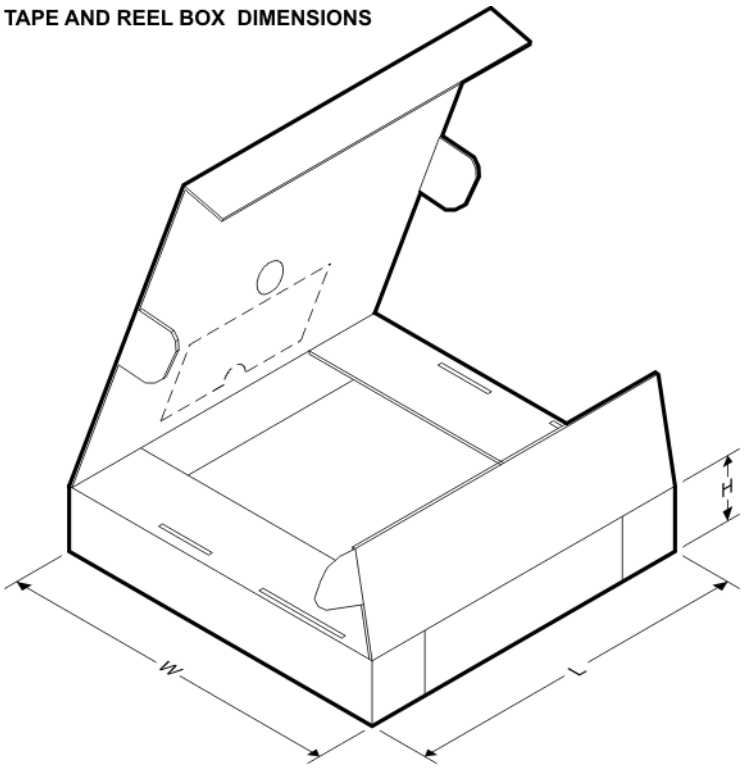
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SM72442MTE/NOPB | TSSOP | PW | 28 | 250 | 178.0 | 16.4 | 6.8 | 10.2 | 1.6 | 8.0 | 16.0 | Q1 |
| SM72442MTX/NOPB | TSSOP | PW | 28 | 2500 | 330.0 | 16.4 | 6.8 | 10.2 | 1.6 | 8.0 | 16.0 | Q1 |

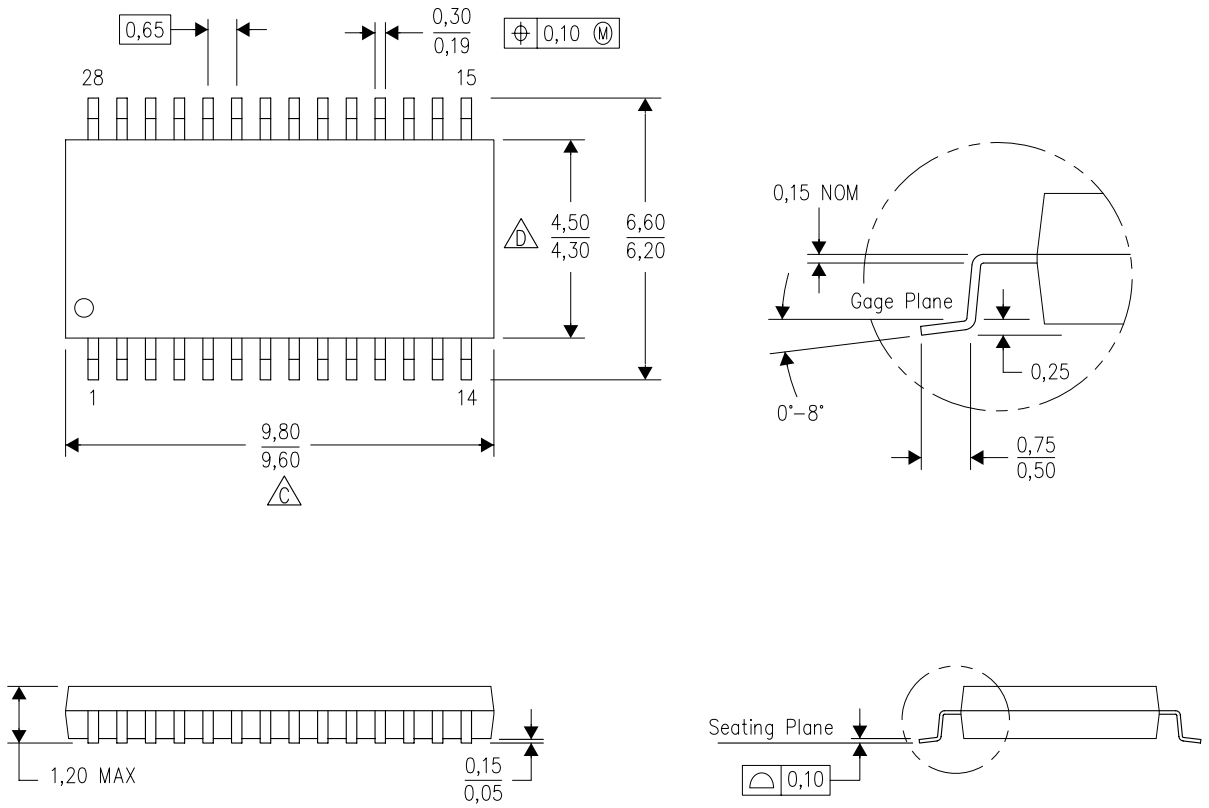
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SM72442MTE/NOPB | TSSOP | PW | 28 | 250 | 210.0 | 185.0 | 35.0 |
| SM72442MTX/NOPB | TSSOP | PW | 28 | 2500 | 367.0 | 367.0 | 38.0 |

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE




4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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