HARRIS SEMICONDUCTOR

CD74FCT16841T, CD74FCT162841T

December 1996

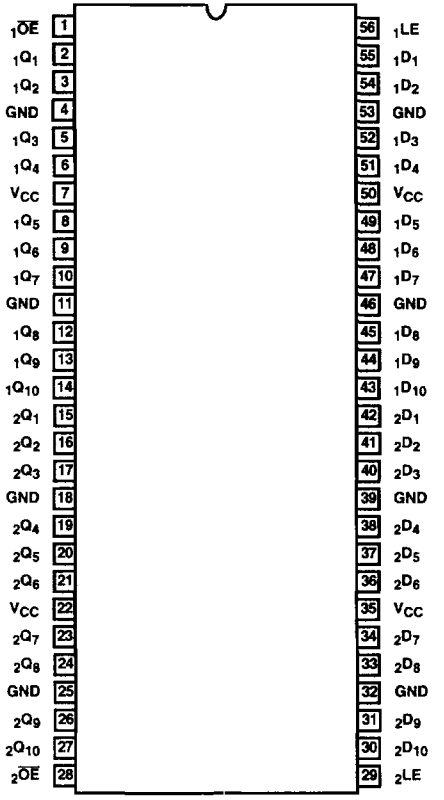
Fast CMOS 20-Bit Transparent Latches

Features

- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16841T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162841T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Pinouts

CD74FCT16841T, CD74FCT162841T
(SSOP, TSSOP)
TOP VIEW



Description

Harris' CD74FCT16841T and CD74FCT162841T are produced in an advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

These devices are 20-bit wide transparent latches designed to provide temporary storage of data and can be used as I/O ports, memory address latches, and bus drivers. The Output Enable and Latch Enable controls allow the devices to be operated as two 10-bit latches or one 20-bit latch. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The output buffers are especially designed for driving high-capacitance loads and low impedance backplanes and include a Power-Off Disable function allowing "live insertion" of boards when the devices are used as backplane drivers.

The CD74FCT162841T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications..

Ordering Information

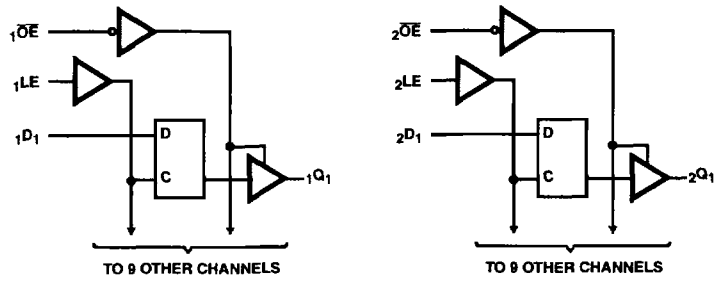
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16841ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16841BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16841CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16841DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16841ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841ETSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4204.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$_xD_x$	$_xLE$	$_x\overline{OE}$	$_xQ_x$
H	H	L	H
L	H	L	L
X	L	L	Q (Note 2)
X	X	H	Z

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before the $_xLE$ HIGH-to-LOW Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$_xD_x$	Data Inputs
$_xLE$	Latch Enable Input (Active LOW)
$_x\overline{OE}$	Output Enable Input (Active LOW)
$_xQ_x$	Three-State Outputs

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only. . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16841T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V		-	-	±100	µA
CD74FCT162841T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 8)	-	0.5	2.5	mA
Supply Current per Input per MHz (Note 9)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND, LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 11)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} f_i = 5MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.7	4.0 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.0 (Note 10)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} Eight Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.2	6.5 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.2	14.5 (Note 10)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	AT (NOTE 13) MIN	AT MAX	BT (NOTE 13) MIN	BT MAX	CT (NOTE 13) MIN	CT MAX	DT (NOTE 13) MIN	DT MAX	ET (NOTE 13) MIN	ET MAX	UNITS
Propagation Delay $_xD_x$ to $_xQ_x$ (LE = HIGH)	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	1.5	4.2	1.5	3.4	ns
		C_L = 300pF (Note 14) R_L = 500Ω	1.5	13.0	1.5	13.0	1.5	13.0	1.5	13.0	1.5	7.5	ns
Propagation Delay $_xLE$ to $_xQ_x$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	1.5	4.0	1.5	3.7	ns
		C_L = 30pF (Note 14) R_L = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	1.5	8.0	1.5	7.5	ns
Output Enable Time $_x\overline{OE}$ to $_xQ_x$	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	11.5	1.5	8.0	1.5	6.5	1.5	4.8	1.5	4.4	ns
		C_L = 300pF (Note 15) R_L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	1.5	9.0	1.5	9.0	ns
Output Disable Time (Note 14) $_x\overline{OE}$ to $_xQ_x$	t_{PHZ}, t_{PLZ}	C_L = 5pF (Note 14) R_L = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	1.5	4.0	1.5	3.6	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	1.5	5.4	1.5	3.6	ns

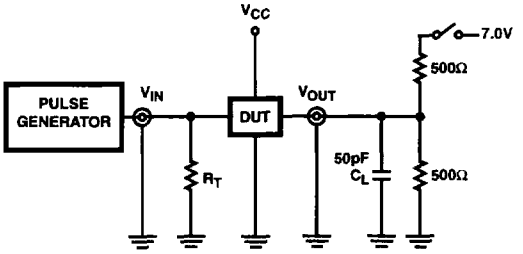
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	AT		BT		CT		DT		ET		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
Setup Time HIGH or LOW, $_XD_X$ to $_X$LE	t_{SU}	C_L = 50pF, R_L = 500Ω	2.5	-	2.5	-	2.5	-	1.0	-	1.0	-	ns
Hold Time HIGH or LOW, $_XD_X$ to $_X$LE	t_H		2.5	-	2.5	-	2.5	-	1.0	-	1.0	-	ns
$_X$LE Pulse Width HIGH (Note 14)	t_W		4.0	-	4.0	-	4.0	-	4.0	-	3.0	-	ns
Output Skew (Note 15)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
12. See test circuit and wave forms.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. This parameter is guaranteed but not production tested.
15. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

16. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_f, $t_r \leq 2.5$ns.

FIGURE 1. TEST CIRCUIT

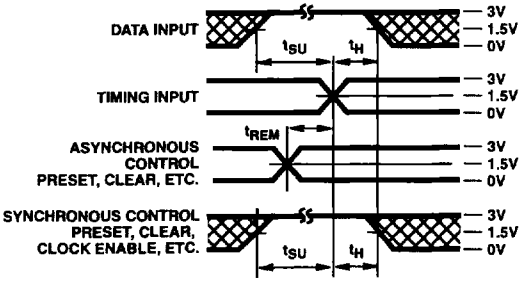


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

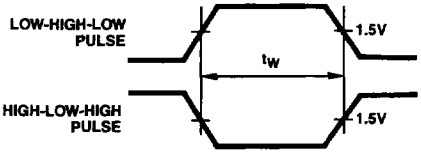


FIGURE 3. PULSE WIDTH

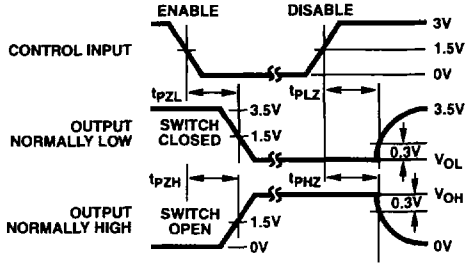


FIGURE 4. ENABLE AND DISABLE TIMING

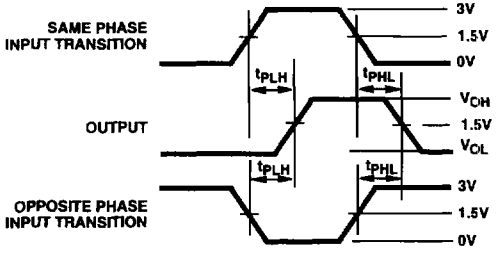


FIGURE 5. PROPAGATION DELAY