Rochester Electronics

Datasheet

PART NUMBER

MQ87C196KD-20R-ROCV

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

M87C196KC, M87C196KD

16-Bit High-Performance CHMOS Microcontrollers with On-Chip EPROM

The M87C196KC/KD 16-bit microcontroller is a high performance member of the MCS-96 microcontroller family. The M87C196KC/KD is an enhanced M80C196KD device with on-chip RAM and EPROM. Intel's CHMOS III-E process provides a high performance processor along with low power consumption.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

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PRELIMINARY

M87C196KC/M87C196KD
16-BIT HIGH-PERFORMANCE CHMOS MICROCONTROLLERS WITH ON-CHIP EPROM

Special Environment

M87C196KC—16 KBytes EPROM, 512 Bytes RAM
M87C196KD—32 KBytes EPROM, 1024 Bytes RAM

- **M87C196KC: 16 MHz Operation**
- **M87C196KD: 16 and 20 MHz Operation**
- **Register-to-Register Architecture**
- **28 Interrupt Sources/16 Vectors**
- **Peripheral Transaction Server**
- **1.4 μs 16 x 16 Multiply (20 MHz)**
- **1.75 μs 16 x 16 Multiply (16 MHz)**
- **2.4 μs 32/16 Divide (20 MHz)**
- **3.0 μs 32/16 Divide (16 MHz)**
- **Powerdown and Idle Modes**
- **Five 8-Bit I/O Ports**
- **16-Bit Watchdog Timer**
- **Available in 68-Lead PGA and 68-Lead Ceramic Quad Flatpack Packages**
- **Dynamically Configurable 8-Bit or 16-Bit Buswidth**
- **Full Duplex Serial Port**
- **High Speed I/O Subsystem**
- **16-Bit Timer**
- **16-Bit Up/Down Counter with Capture**
- **3 Pulse-Width-Modulated Outputs**
- **Four 16-Bit Software Timers**
- **8- or 10-Bit A/D Converter with Sample/Hold**
- **$\overline{\text{HOLD}}/\overline{\text{HLDA}}$ Bus Protocol**
- **Product Grades**
  - **— SE1 (QML): −55°C to +125°C**
  - **— SE2 (QML): −40°C to +125°C (M87C196KD only)**

The M87C196KC/KD 16-bit microcontroller is a high performance member of the MCS®-96 microcontroller family. The M87C196KC/KD is an enhanced M80C196KB device with on-chip RAM and EPROM. Intel's CHMOS III-E process provides a high performance processor along with low power consumption.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

For bus design information, configuration, and programming, please see the 8XC196KC/8XC196KD User's Manual (order #272238).

MCS®-96 is a registered trademark of Intel Corporation.

February 1996 **Order Number: 271116-005**

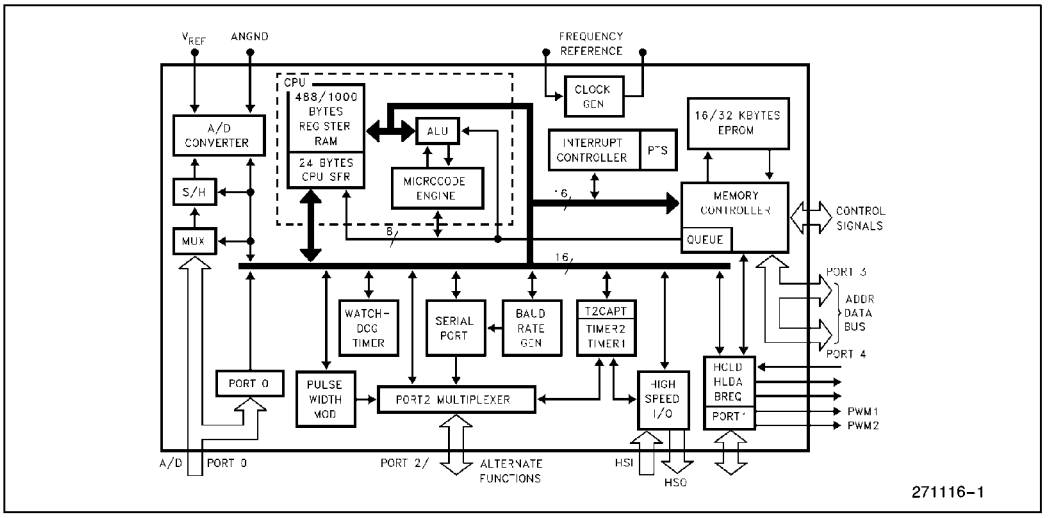


Figure 1. M87C196KC/KD Block Diagram

PACKAGING

PGA	CQFP	Signal
1	9	ACH7/P0.7
2	8	ACH6/P0.6
3	7	ACH2/P0.2
4	6	ACH0/P0.0
5	5	ACH1/P0.1
6	4	ACH3/P0.3
7	3	NMI
8	2	$\overline{EA}$
9	1	V_{CC}
10	68	V_{SS}
11	67	XTAL1
12	66	XTAL2
13	65	CLKOUT
14	64	BUSWIDTH
15	63	INST
16	62	ALE/$\overline{ADV}$
17	61	$\overline{RD}$
18	60	AD0/P3.0
19	59	AD1/P3.1
20	58	AD2/P3.2
21	57	AD3/P3.3
22	56	AD4/P3.4
23	55	AD5/P3.5

PGA	CQFP	Signal
24	54	AD6/P3.6
25	53	AD7/P3.7
26	52	AD8/P4.0
27	51	AD9/P4.1
28	50	AD10/P4.2
29	49	AD11/P4.3
30	48	AD12/P4.4
31	47	AD13/P4.5
32	46	AD14/P4.6
33	45	AD15/P4.7
34	44	T2CLK/P2.3
35	43	READY
36	42	T2RST/P2.4/$\overline{AINC}$
37	41	$\overline{BHE}$/$\overline{WRH}$
38	40	$\overline{WR}$/$\overline{WRL}$
39	39	PWM0/P2.5
40	38	T2CAPTURE/P2.7/$\overline{PACT}$
41	37	V_{PP}
42	36	V_{SS}
43	35	HS0.3
44	34	HS0.2
45	33	T2UP-DN/P2.6
46	32	P1.7/$\overline{HOLD}$

PGA	CQFP	Signal
47	31	P1.6/$\overline{HLDA}$
48	30	P1.5/$\overline{BREQ}$
49	29	HSO.1
50	28	HSO.0
51	27	HSO.5/HSI.3
52	26	HSO.4/HSI.2
53	25	HSI.1
54	24	HSI.0
55	23	P1.4/PWM2
56	22	P1.3/PWM1
57	21	P1.2
58	20	P1.1
59	19	P1.0
60	18	TXD/P2.0
61	17	RXD/P2.1
62	16	$\overline{RESET}$
63	15	EXTINT/P2.2
64	14	V_{SS}
65	13	V_{REF}
66	12	ANGND
67	11	ACH4/P0.4
68	10	ACH5/P0.5

Figure 2. Pin Definitions

PACKAGING

The M87C196KC/KD is available in a ceramic pin grid array, shown in Figure 3, and a leaded ceramic quad pack shown in Figure 4.

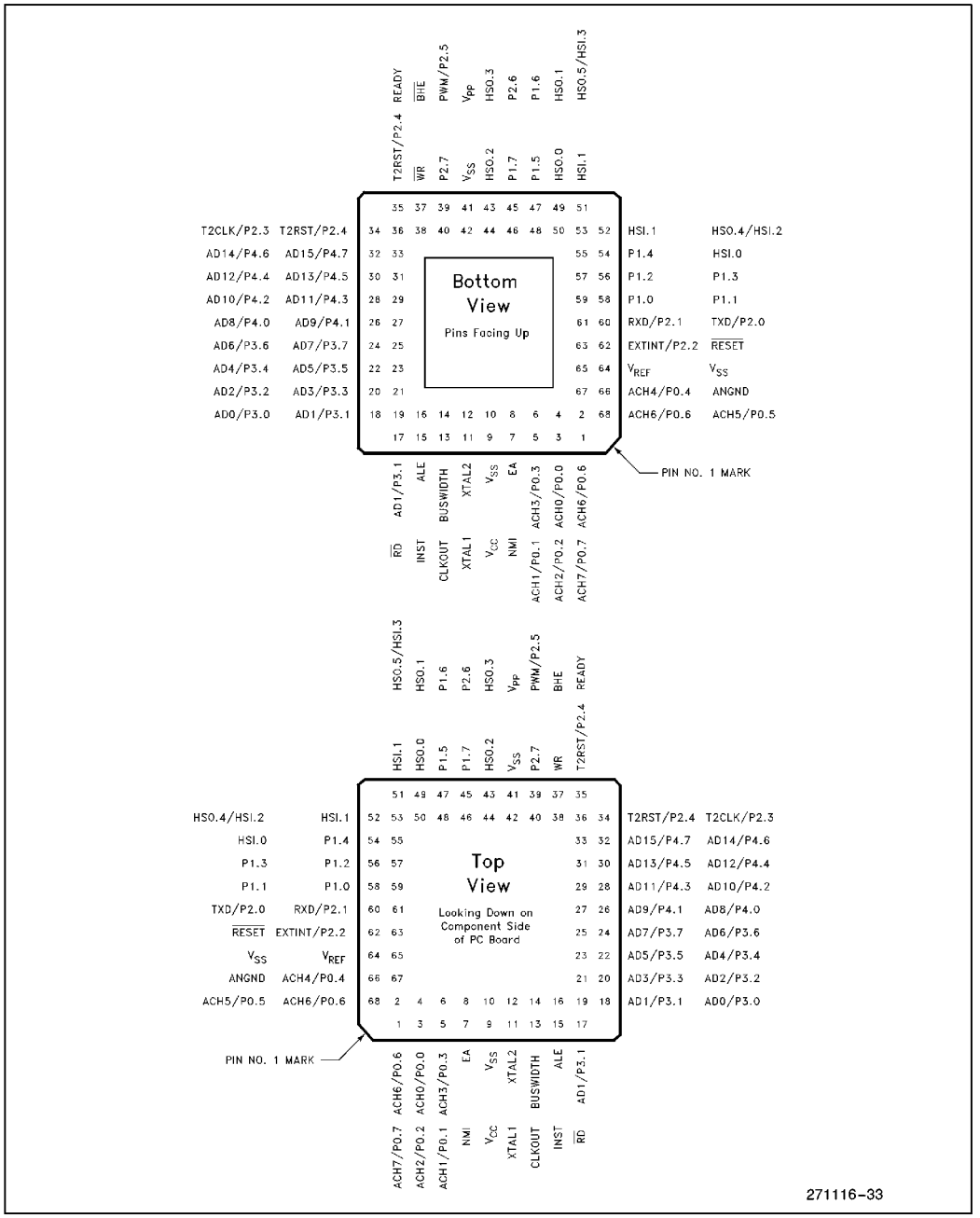


Figure 3. 68-Pin Grid Array Pinout

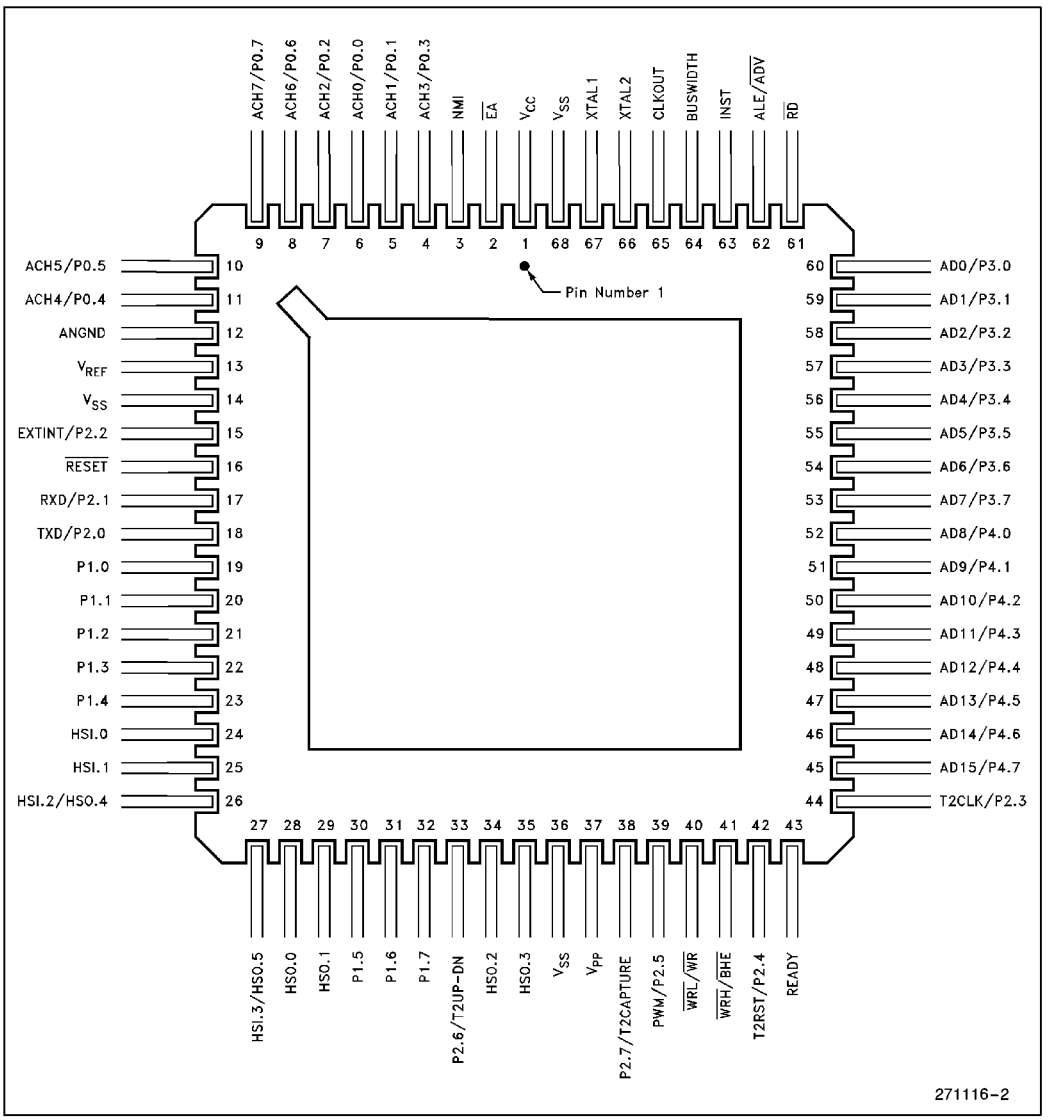


Figure 4. 68-Pin Ceramic Quad Flatpack

PIN DESCRIPTIONS

Symbol	Name and Function
V_{CC}	Main supply voltage (5V).
V_{SS}	Digital circuit ground (0V). There are three V_{SS} pins, all of which must be connected.
V_{REF}	Reference voltage for the A/D converter (5V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Timing pin for the return from powerdown circuit. Connect this pin with a 1 μF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used V_{PP} may be tied to V_{CC}. This pin is the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency.
$\overline{\text{RESET}}$	Reset input to the chip.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{\text{EA}}$	Input for memory select (External Access). $\overline{\text{EA}}$ equal to a TTL-high causes memory accesses to locations 2000H through 5FFFH to be directed to on-chip EPROM. $\overline{\text{EA}}$ equal to a TTL-low causes accesses to those locations to be directed to off-chip memory.
ALE/$\overline{\text{ADV}}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{\text{ADV}}$, it goes inactive high at the end of the bus cycle. ALE/$\overline{\text{ADV}}$ is activated only during external memory accesses.
$\overline{\text{RD}}$	Read signal output to external memory. $\overline{\text{RD}}$ is activated only during external memory reads.
$\overline{\text{WR}}$/$\overline{\text{WRL}}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{\text{WR}}$ will go low for every external write, while $\overline{\text{WRL}}$ will go low only for external writes where an even byte is being written. $\overline{\text{WR}}$/$\overline{\text{WRL}}$ is activated only during external memory writes.
$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{\text{BHE}}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{\text{BHE}}$ = 1), to the high byte only (A0 = 1, $\overline{\text{BHE}}$ = 0), or both bytes (A0 = 0, $\overline{\text{BHE}}$ = 0). If the $\overline{\text{WRH}}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{\text{BHE}}$/$\overline{\text{WRH}}$ is valid only during 16-bit external memory write cycles.

PIN DESCRIPTIONS (Continued)

Symbol	Name and Function
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSI.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the M87C196KC.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.

ELECTRICAL CHARACTERISTICS

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings*

Case Temperature
Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin to V_{SS} ..... −0.5V to +7.0V
Power Dissipation 1.5W

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T_C (SE1)	Case Temperature (Instant On)	−55	+125	°C
T_C (SE2)	Case Temperature (Instant On)	−40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
F_{OSC}	Oscillator Frequency	3.5	16	MHz
F_{OSC}	Oscillator Frequency (M87C196KD-20 only)	3.5	20	MHz

NOTE:
ANGND and V_{SS} should be nominally at the same potential.

DC Characteristics (Over Specified Operating Conditions)

Symbol	Description	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage (Note 1)	0.2 V_{CC} + 1.0	V_{CC}	V	
V_{IH1}	Input High Voltage on XTAL 1, EA	0.7 V_{CC}	V_{CC}	V	
V_{IH2}	Input High Voltage on RESET	2.32	V_{CC}	V	
V_{OL}	Output Low Voltage		0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 2.8 mA I_{OL} = 7 mA
V_{OL1}	Output Low Voltage in RESET on P2.5 (Note 2)		0.8	V	I_{OL} = +0.4 mA

NOTES:
1. All pins except RESET, XTAL1 and EA.
2. Violating these specifications in Reset may cause the part to enter test modes.

DC Characteristics (Over Specified Operating Conditions) (Continued)

Symbol	Description	Min	Max	Units	Test Conditions
V_{OH}	Output High Voltage (Standard Outputs)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$		V V V	$I_{OH} = -200\ \mu A$ $I_{OH} = -3.2$ mA $I_{OH} = -7$ mA
V_{OH1}	Output High Voltage (Quasi-bidirectional Outputs)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$		V V V	$I_{OH} = -10\ \mu A$ $I_{OH} = -30\ \mu A$ $I_{OH} = -60\ \mu A$
V_{OH2}	Output High Voltage in RESET on P2.0 (Note 7)	2.0		V	$I_{OH} = -0.8$ mA
I_{LI}	Input Leakage Current (Std. Inputs)		±10	µA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current (Port 0)		±3	µA	$0 < V_{IN} < V_{REF}$
I_{TL}	1 to 0 Transition Current (QBD Pins)		−650	µA	$V_{IN} = 2.0V$
I_{IL}	Logical 0 Input Current (QBD Pins)		−70	µA	$V_{IN} = 0.45V$
I_{IH}	Logical 1 Input Current (NMI Pin)		250	µA	$V_{IN} = V_{CC} - 0.3V$
I_{CC}	Active Mode Current in Reset		75 93	mA mA	XTAL1 = 16 MHz XTAL1 = 20 MHz
I_{REF}	A/D Converter Reference Current		5	mA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
I_{IDLE}	Idle Mode Current		30	mA	
I_{PD}	Powerdown Mode Current		70	µA	$V_{CC} = V_{PP} = V_{REF} = 5.5V$
R_{RST}	Reset Pullup Resistor	6K	65K	Ω	$V_{CC} = 5.5V, V_{IN} = 4.0V$
C_S	Pin Capacitance (Any Pin to V_{SS})		10	pF	

NOTES:
(Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0, and RXD (in serial mode 0). The V_{OH} specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, READY, BUSWIDTH, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3, and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if V_{OL} is held above 0.45V or V_{OH} is held below $V_{CC} - 0.7V$:
   I_{OL} on Output pins: 10 mA
   I_{OH} on quasi-bidirectional pins: self limiting
   I_{OH} on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

Port 1, P2.6	I_{OL}: 29 mA	I_{OH} is self limiting
HSO, P2.0, RXD, $\overline{RESET}$	I_{OL}: 29 mA	I_{OH}: 26 mA
P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$	I_{OL}: 13 mA	I_{OH}: 11 mA
AD0–AD15	I_{OL}: 52 mA	I_{OH}: 52 mA
$\overline{RD}$, ALE, INST–CLKOUT	I_{OL}: 13 mA	I_{OH}: 13 mA

7. Violating these specifications in Reset may cause the part to enter test modes.

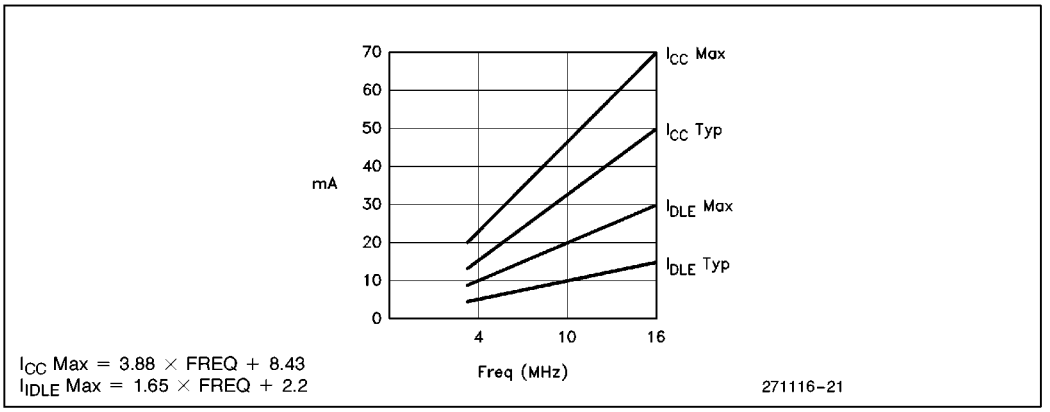


Figure 5. I_{CC} and I_{IDLE} vs Frequency

AC Characteristics

For use over specified operating conditions.

The system must meet these specifications to work with the M87C196KC/KD:

Symbol	Description	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2\,T_{OSC} - 75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 75$	ns	
T_{YLYH}	Non READY Time	No upper limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2\,T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2\,T_{OSC} - 75$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 65$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3\,T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 26$	ns	(Note 2)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 5$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTES:
1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add $2\,T_{OSC} * N$, where N = number of wait states.
3. Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

AC Characteristics (Continued)

For user over specified operating conditions.

The M87C196KC/KD will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F_{XTAL}	Frequency on XTAL1	3.5 3.5	16 20	MHz MHz	KC/KD-16 KD-20
T_{OSC}	$1/F_{XTAL}$	62.5 50	286 286	ns ns	KC/KD-16 KD-20
T_{XHCH}	XTAL1 High to CLKOUT High or Low	10	110	ns	
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC}+20	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−5	15	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−29	+15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	(Note 3)
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC}+15	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 15			
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 49		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 36		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	0	30	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5		ns	(Note 3)
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 1)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		15 30	ns ns	KC-16 KD-16/20
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23			
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−10	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 30		ns	(Note 3)
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 30		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 10	T_{OSC} + 15	ns	(Note 1)
T_{WHBX}	$\overline{BHE}$, INST after $\overline{WR}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 HOLD after $\overline{WR}$ Rising	T_{OSC} − 50		ns	(Note 2)
T_{RHBX}	$\overline{BHE}$, INST after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{RHAX}	AD8–15 HOLD after $\overline{RD}$ Rising	T_{OSC} − 25		ns	(Note 2)

NOTES:
1. Assuming back-to-back bus cycles.
2. 8-Bit bus only.
3. If wait states are used, add 2 T_{OSC} * N, where N = number of wait states.
4. Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz.

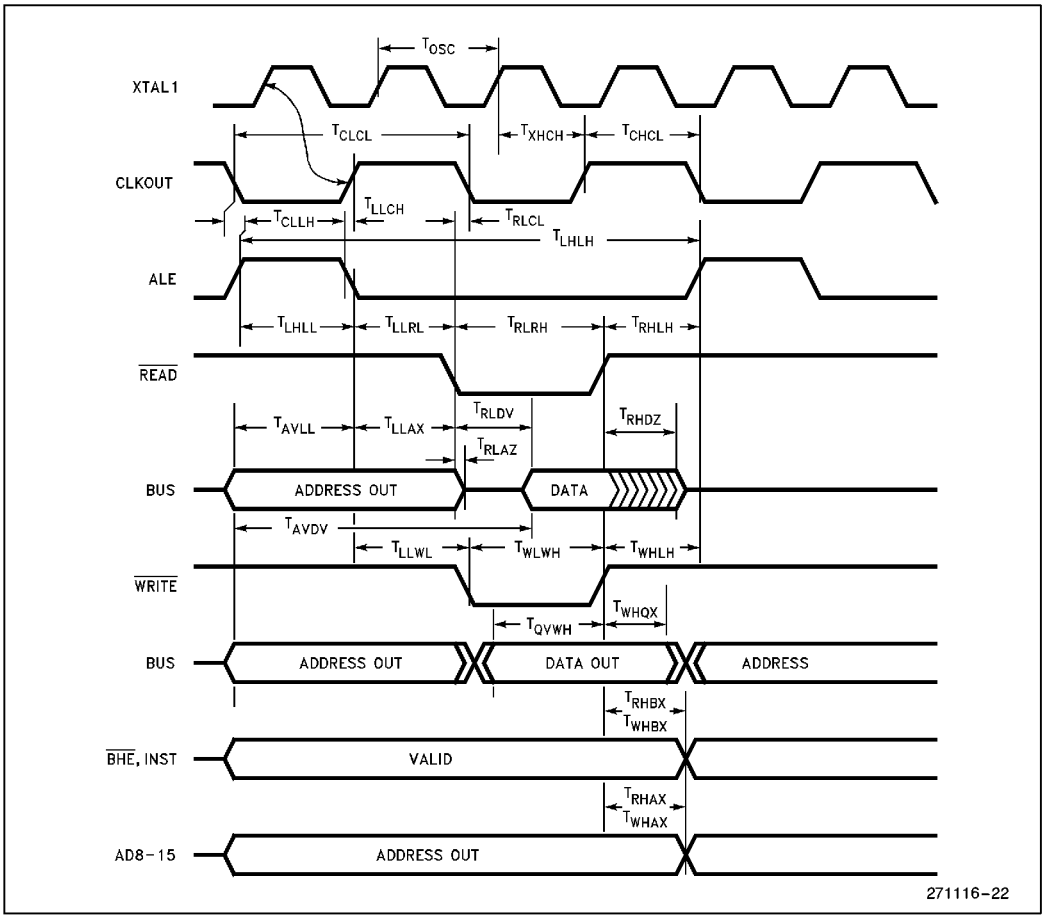


Figure 6. System Bus Timings

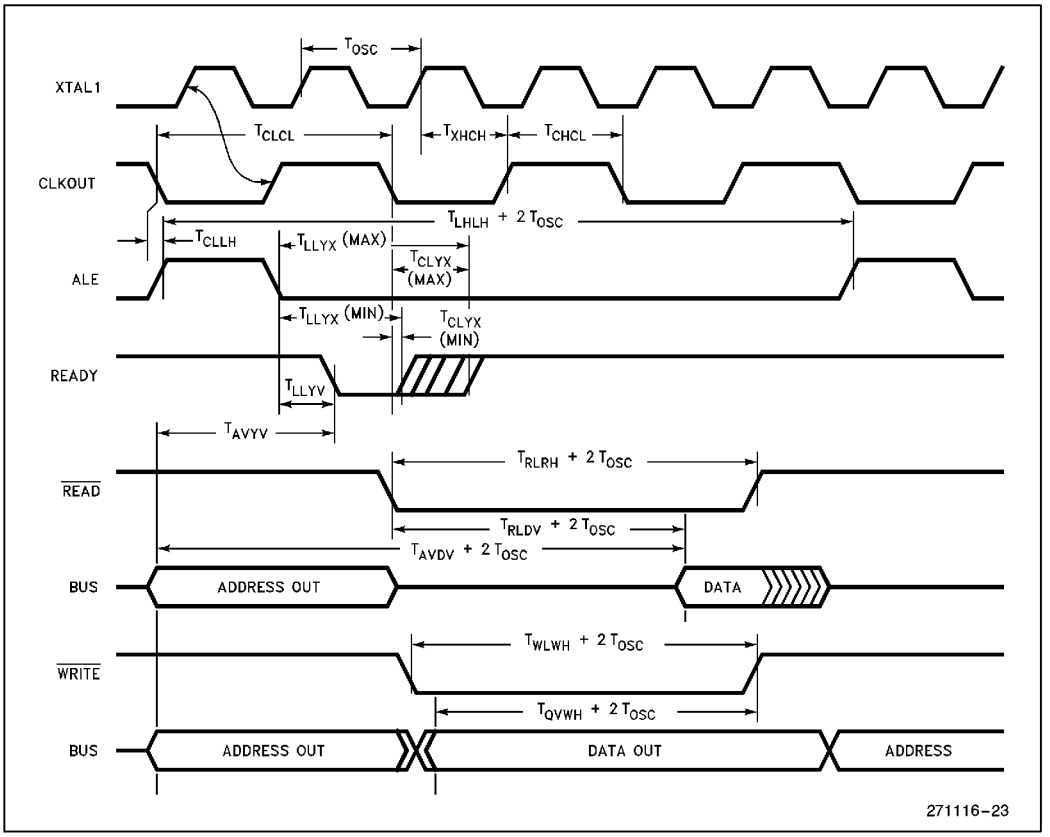


Figure 7. READY Timings (One Waitstate)

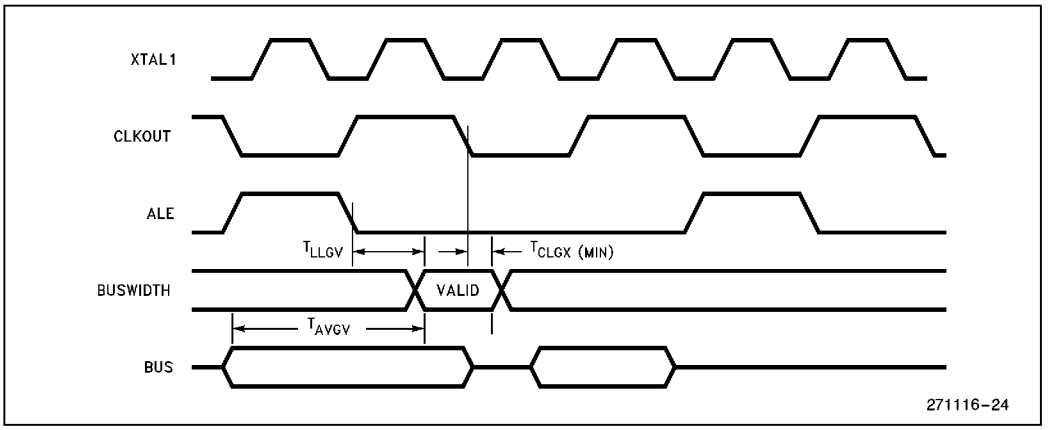


Figure 8. Buswidth Timings

HOLD/HLDA Timings

Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	55		ns	(Note 1)
T_{CLHAL}	CLKOUT Low to HLDA Low	−15	15	ns	
T_{CLBRL}	CLKOUT Low to BREQ Low	−15	15	ns	
T_{HALAZ}	HLDA Low to Address Float		10	ns	
T_{HALBZ}	HLDA Low to BHE, INST, RD, WR Weakly Driven		15	ns	
T_{CLHAH}	CLKOUT Low to HLDA High	−15	15	ns	
T_{CLBRH}	CLKOUT Low to BREQ High	−15	15	ns	
T_{HAHAX}	HLDA High to Address No Longer Float	−15		ns	
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	−10		ns	
T_{CLLH}	CLKOUT Low to ALE High	−5	15	ns	

NOTE:
1. To guarantee recognition at next clock.

DC SPECIFICATIONS IN HOLD

	Min	Max	Units
Weak Pullups on ADV, RD, WR, WRL, BHE	50K	250K	V_{CC} = 5.5V, V_{IN} = 0.45V
Weak Pulldowns on ALE, INST	10K	50K	V_{CC} = 5.5V, V_{IN} = 2.4

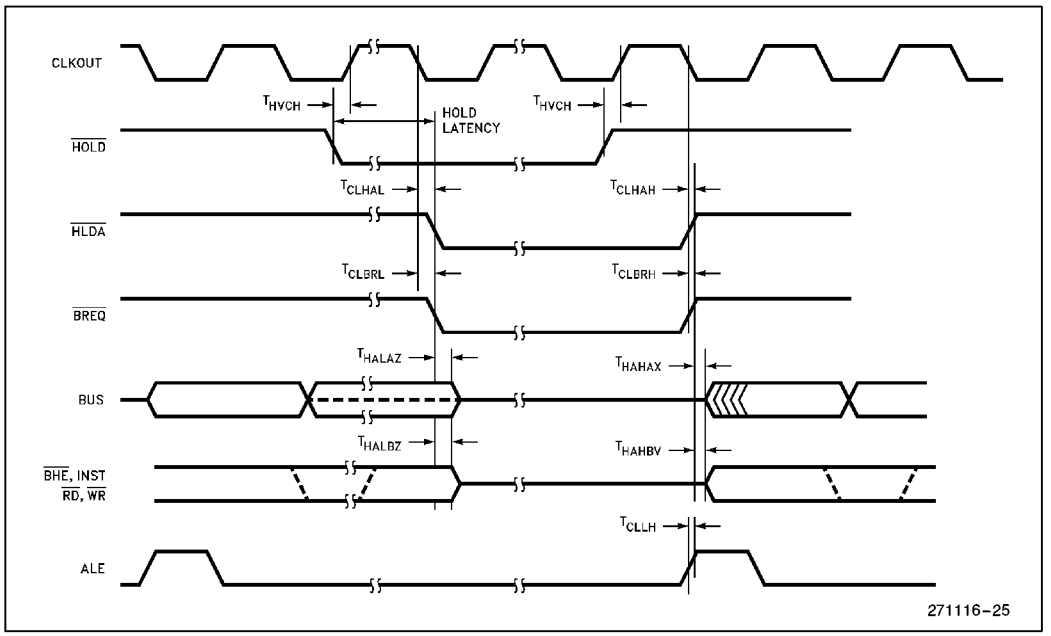


Figure 9. HOLD/HLDA Timings

EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units	Notes
$1/T_{XLXL}$	Oscillator Frequency	3.5 3.5	16.0 20.0	MHz MHz	KC/KD-16 KD-20
T_{XLXL}	Oscillator Frequency	62.5 50	286 286	ns	KC/KD-16 KD-20
T_{XHXX}	High Time	22 17		ns ns	KC/KD-16 KD-20
T_{XLXX}	Low Time	22 17		ns ns	KC/KD-16 KD-20
T_{XLXH}	Rise Time		10	ns	
T_{XHXL}	Fall Time		10	ns	

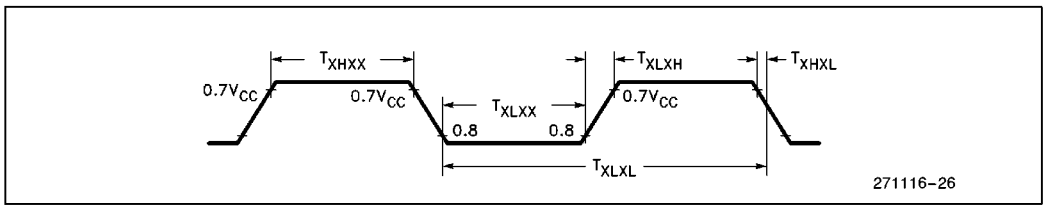
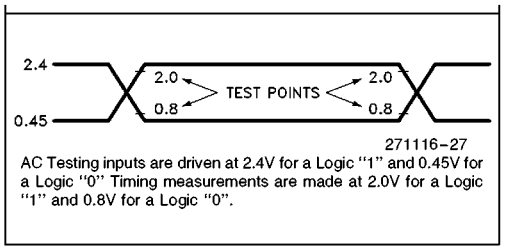
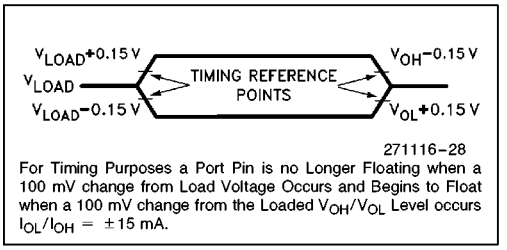


Figure 10. External Clock Drive Waveforms



AC Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

Figure 11. AC Testing Input, Output Waveforms



For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs and Begins to Float when a 100 mV change from the Loaded V_{OH}/V_{OL} Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

Figure 12. Float Waveforms

EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions:

H— High
L— Low
V— Valid
X— No Longer Valid
Z— Floating

Signals:

A— Address
B— $\overline{BHE}$
C— CLKOUT
D— DATA
G— Buswidth
H— $\overline{HOLD}$
HA— $\overline{HLDA}$
L— ALE/$\overline{ADV}$
BR— $\overline{BREQ}$
R— $\overline{RD}$
W— $\overline{WR}/\overline{WRH}/\overline{WRL}$
X— XTAL1
Y— READY
Q— Data Out

AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period (BRR ≥ 8002H)	6 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H)	4 T_{OSC} ±50		ns
T_{XLXL}	Serial Port Clock Period (BRR = 8001H)	4 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	2 T_{OSC} ±50		ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} − 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	T_{OSC} +50		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		1 T_{OSC}	ns

WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

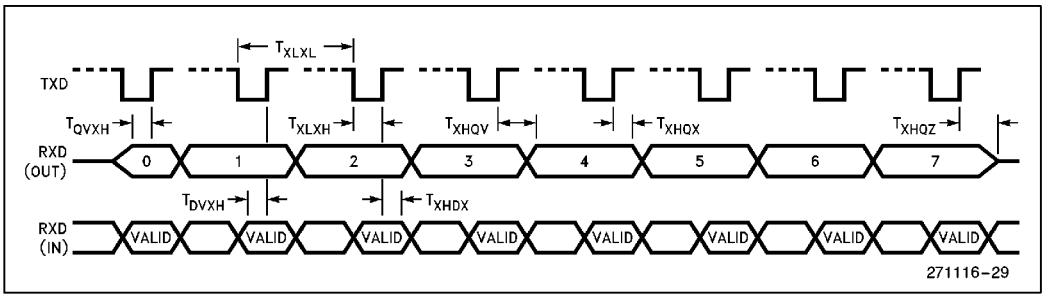


Figure 13. Serial Port Waveform—Shift Register Mode

THERMAL CHARACTERISTICS

	M87C196KC		M87C196KD	
Package Type	θ_{ja}	θ_{jc}	θ_{ja}	θ_{jc}
PGA	29.5°C/W	6°C/W	29°C/W	4°C/W
CQFP	30°C/W	9.5°C/W	30°C/W	11°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

EPROM SPECIFICATIONS

AC EPROM Programming Characteristics

Operating Conditions: Load Capacitance = 150 pF, T_A = +25°C ±5°C, V_{CC}, V_{REF} = 5V, V_{SS}, ANGND = 0V, V_{PP} = 12.50V ±0.25V, EA = 12.50V ±0.25V

Symbol	Description	Min	Max	Units
T_{SHLL}	Reset High to First $\overline{PALE}$ Low	1100		T_{OSC}
T_{LLLH}	$\overline{PALE}$ Pulse Width	50		T_{OSC}
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{PLDV}	$\overline{PROG}$ Low to Word Dump Valid		50	T_{OSC}
T_{PHDX}	Word Dump Data Hold		50	T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{PLPH}(2)	$\overline{PROG}$ Pulse Width	50		T_{OSC}
T_{PHLL}	$\overline{PROG}$ High to Next $\overline{PALE}$ Low	220		T_{OSC}
T_{LHPL}	$\overline{PALE}$ High to $\overline{PROG}$ Low	220		T_{OSC}
T_{PHPL}	$\overline{PROG}$ High to Next $\overline{PROG}$ Low	220		T_{OSC}
T_{PHIL}	$\overline{PROG}$ High to AINC Low	0		T_{OSC}
T_{ILIH}	$\overline{AINC}$ Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after $\overline{AINC}$ Low	50		T_{OSC}
T_{ILPL}	$\overline{AINC}$ Low to $\overline{PROG}$ Low	170		T_{OSC}
T_{PHVL}	$\overline{PROG}$ High to $\overline{PVER}$ Valid		220	T_{OSC}

NOTES:
1. Run Time Programming is done with Fosc = 6.0 MHz to 12.0 MHz, V_{REF} = 5V ±0.50V. T_A = +25°C to ±5°C and V_{PP} = 12.50V.
2. This specification is for the Word Dump Mode. For programming pulses, use 300 T_{OSC} + 100 μs.

DC EPROM Programming Characteristics

Symbol	Description	Min	Max	Units
I_{PP}	V_{PP} Supply Current (When Programming)		100	mA

NOTE:
V_{PP} must be within 1V of V_{CC} while V_{CC} < 4.5V. V_{PP} must not have a low impedance path to ground of V_{SS} while V_{CC} > 4.5V.

Erasing the M87C196KC/KD EPROM

Initially, and after each erasure, all bits of the M87C196KC/KD are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The erasure characteristics of the M87C196KC/KD are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Constant exposure to room level fluorescent lighting could erase the typical M87C196KC/KD in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M87C196KC/KD is to be exposed to light for extended periods of time, opaque labels must be placed over the EPROM's window to prevent unintentional erasure.

The recommended erasure procedure for the M87C196KC/KD is exposure to shortwave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 35 to 60 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The M87C196KC/KD should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an M87C196KC/KD can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the M87C196KC/KD to high intensity UV light for long periods may cause permanent damage.

EPROM PROGRAMMING WAVEFORMS

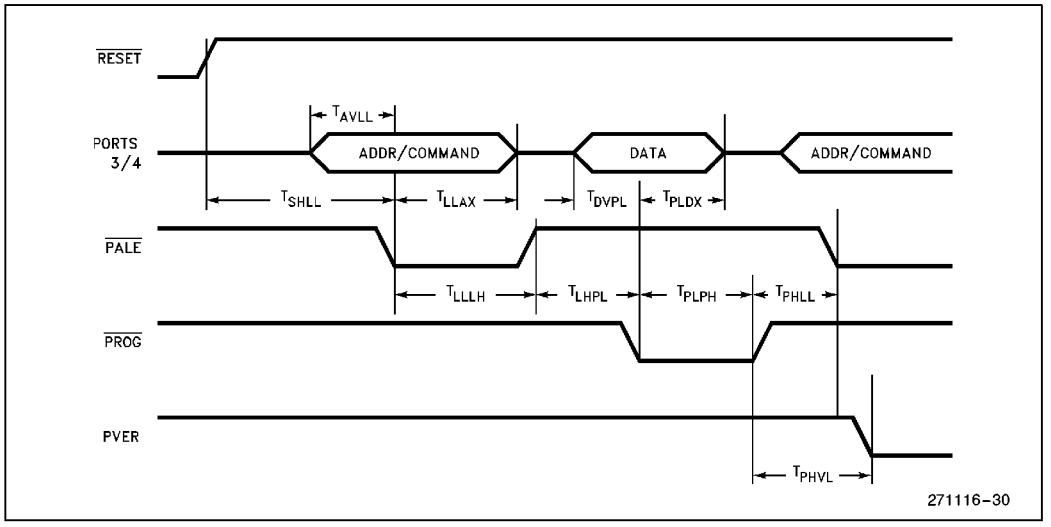


Figure 14. Slave Programming Mode Data Program Mode with Single Program Pulse

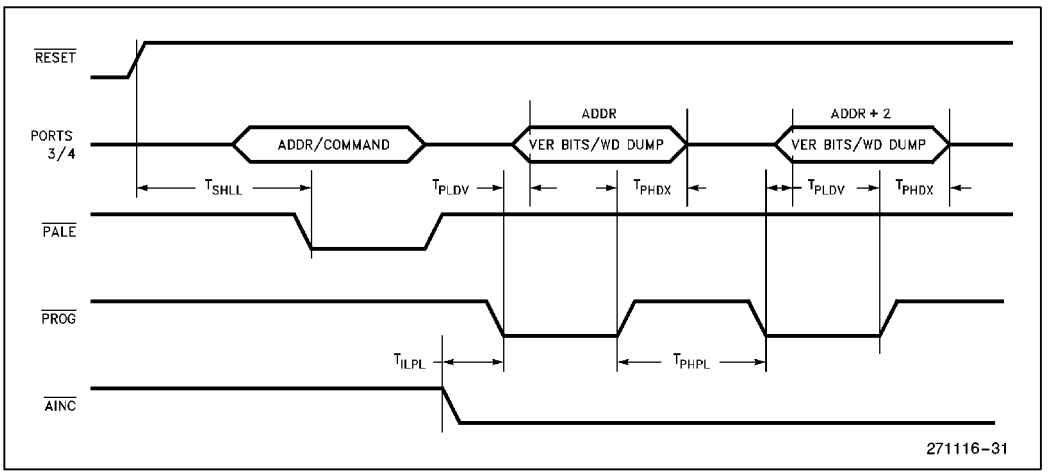


Figure 15. Slave Programming Mode in Word Dump with Auto Increment

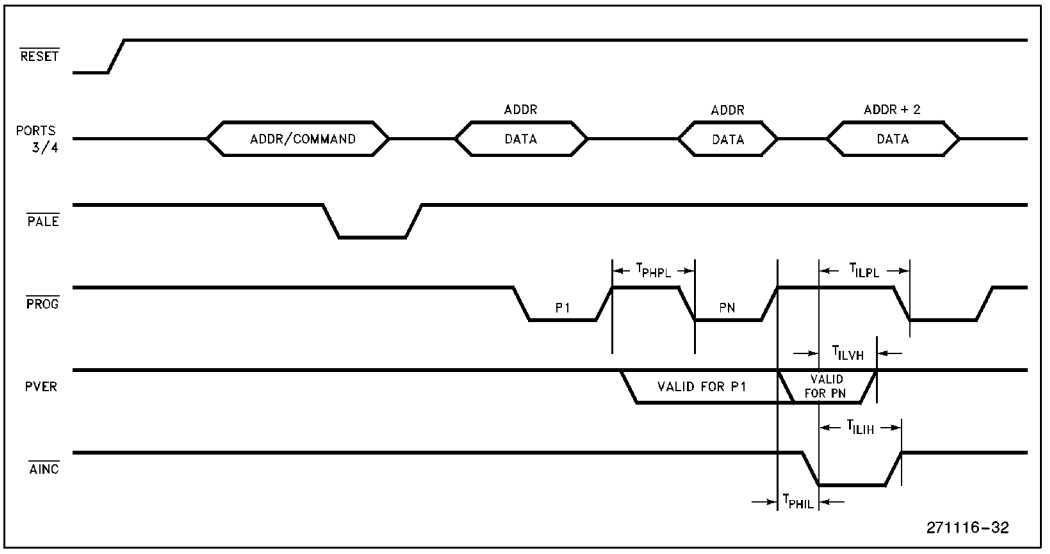


Figure 16. Slave Programming Mode Timing in Data Program with Repeated Prog Pulse and Auto Increment

10-BIT A/D CHARACTERISTICS

The speed of the A/D converter in the 10-bit mode can be adjusted by setting a clock prescaler on or off. At high frequencies more time is needed for the comparator to settle. The maximum frequency with the clock prescaler disabled is 6 MHz. The conversion times with the prescaler turned on or off is shown in the table below. The AD_TIME register has not been characterized for the 10-bit mode.

The converter is ratiometric, so the absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the digital section of the converter.

A/D CONVERTER SPECIFICATIONS

The specifications given below assume adherence to the Operating Conditions section of this data sheet. Testing is performed with V_{REF} = 5.12V.

Clock Prescaler On IOC2.4 = 0	Clock Prescaler Off IOC2.4 = 1
156.5 States 19.5 μs @ 16 MHz	89.5 States 29.8 μs @ 6 MHz

Parameter	Typical(3)	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	±8	LSBs	
Full Scale Error	±3			LSBs	
Zero Offset Error	±3			LSBs	
Non-Linearity		0	±8	LSBs	
Differential Non-Linearity Error		>−1	+2	LSBs	
Channel-to-Channel Matching		0	±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.009 0.009 0.009			 LSB/°C LSB/°C LSB/°C	
Off Isolation		−60		dB	1, 2
Feedthrough	−60			dB	1
V_{CC} Power Supply Rejection	−60			dB	1
Input Resistance		750	1.2K	Ω	
DC Input Leakage		0	3.0	μA	
Sample Time: Prescaler On Prescaler Off	16 8			States States	
Input Capacitance	3			pF	

NOTES:
*An "LSB", as used here, has a value of approximately 5 mV.
1. DC to 100 KHz.
2. Multiplexer Break-Before-Make Guaranteed.
3. Typical values are expected for most devices at 25°C.

8-BIT MODE A/D CHARACTERISTICS

The 8-bit mode trades off resolution for a faster conversion time. The AD_TIME register must be used when performing an 8-bit conversion.

Sample Time 20 States	Convert Time 56 States
A6H in AD_TIME 9.8 μs @ 16 MHz	

The following specifications are tested @ 16 MHz with OA6H in AD_TIME.

Parameter	Typical	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±2	LSBs	
Full Scale Error	±1			LSBs	
Zero Offset Error	±2			LSBs	
Non-Linearity		0	±2	LSBs	
Differential Non-Linearity Error		>−1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	 0.003 0.003 0.003			 LSB/°C LSB/°C LSB/°C	

NOTES:
*An "LSB", as used here, has a value of approximately 20 mV.
1. Typical values are expected for most devices at 25°C.

M87C196KC DESIGN INFORMATION

M87C196KC Enhanced Feature Set over the M80C196KB

1. The M87C196KC has twice the RAM of the M80C196KB and 16 Kbytes of EPROM. Also, a Vertical Register Windowing Scheme allows the extra 256 bytes of RAM to be used as registers. This greatly reduces the context switching time.
2. Peripheral Transaction Server (PTS). The PTS is an alternative way to service an interrupt, reducing latency and overhead. Each interrupt can be mapped to its PTS channel, which acts like a DMA channel. Each interrupt can now do a single or block transfer, without executing an interupt service routine. Special PTS modes exist for the A/D converter, HSI, and HSO.
3. Two extra Pluse Width Modulated outputs. The M87C196KC has added 2 PWM outputs that are functionally compatible to the 80C196KB PWM.
4. Timer2 Internal Clocking. Timer2 can now be clocked with an internal source, every 1 or 8 state times.
5. The A/D can now perform an 8- as well as a 10-bit conversion. This trades off resolution for a faster conversion time.
6. Additional On-chip Memory Security. Two UPROM (Uneraseable Programmable Read Only Memory) bits can be programmed to disable the bus controller for external code and data fetches. Once programmed, a UPROM bit cannot be erased. By shutting off the bus controller for external fetches, no one can try and gain access to your code by executing from external memory.
7. New Instructions. The M87C196KC has 5 new instructions. An exchange (XCHB/XCHW) instruction swaps two memory locations, an Interruptable Block Move Instruction (BMOVI), a Table Indirect Jump (TIJMP) instruction, and two instructions for enabling and disabling the PTS (EPTS/DPTS).

M80C196KB TO M87C196KC DESIGN CONSIDERATIONS

1. Memory Map. The M87C196KC has 512 bytes of RAM/SFRs and 16K of EPROM. The extra 256 bytes of RAM will reside in locations 100H–1FFH and the extra 8K of EPROM will reside in locations 4000H–5FFFH. These locations are external memory on the M80C196KB.
2. EPROM programming. The M87C196KC has a different programming algorithm to support 16K of on-board memory.
3. ONCE Mode Entry. The ONCE mode is entered on the M87C196KC by driving the TXD pin low on the rising edge of RESET. The TXD pin is held high by a pullup that is specified at 1.4 mA and remain at 2.0V. This Pullup must not be overridden or the M87C196KC will enter the ONCE mode.
4. During the bus HOLD state, the M87C196KC weakly holds RD, WR, ALE, BHE and INST in their inactive states. The 80C196KB only holds ALE in its inactive state.
5. A RESET pulse from the M87C196KC is 16 states rather than 4 states as on the 80C196KB (i.e., a watchdog timer overflow). This provides a longer RESET pulse for other devices in the system.
6. The CDE pin on the KB has become a V_{SS} pin on the KC to support 16 MHz operation.

M87C196KC ERRATA

1. **Missed EXTINT on P0.7.**

   The 80C196KC20 could possibly miss an EXTINT on P0.7. See faxback #2049.
2. HIS_MODE divide-by-eight.

   See Faxback #2192.
3. IPD hump.

   See Faxback #2311.

M87C196KD DESIGN INFORMATION

M87C196KD Enhancements over the M87C196KC

The M87C196KD is an enhanced, pin-for-pin compatible upgrade to the M87C196KC. The M87C196KD offers the same functionality, packages, and pin-outs as the M87C196KC with twice the on-chip EPROM and register RAM.

1. Doubling the on-chip EPROM to 32 KBytes allows for larger on-chip programs.
2. Doubling the on-chip RAM to 1000 bytes allows for faster and more optimized code execution.

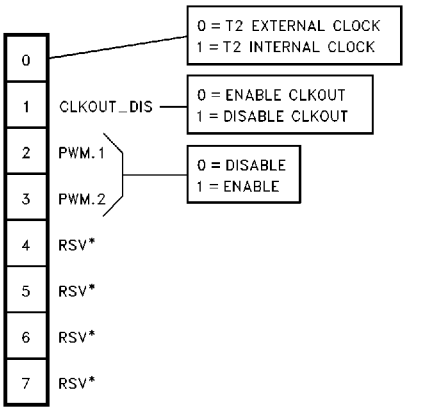
M87C196KC TO M87C196KD DESIGN CONSIDERATIONS

Due to the added memory, a few memory-specific functions have been modified on the M87C196KD.

1. The AC characteristic $\overline{RD}$ Low to Address Float (T_{RLAZ}) maximum has been increased from 15 ns on the M87C196KC to 30 ns on the M87C196KD.
2. The memory map is expanded to accommodate the additional memory. Because the added memory resides in memory locations that were always external to the M87C196KC, M87C196KC code may have to be modified to run on the M87C196KD.
3. The vertical windowing map is extended to allow all 1000 bytes of register RAM to be windowed into the lower register file.
4. The M87C196KD has a different autoprogramming algorithm to support 32 KBytes of on-chip EPROM.

NEW M87C196KC/KD FEATURE

A CLKOUT disable bit has been added to the IOC3 SFR. This can be used to reduce noise in systems that do not require the CLKOUT signal. Figure 17 indicates the placement of the new bit.



NOTE:
*RSV—Reserved bits must be = 0

Figure 17. M87C196KD New SFR Bit (CLKOUT Disable)

DATASHEET REVISION HISTORY

The changes made since the October 1992 revision of the M87C196KC datasheet (271116-004) are as follows:

1. Added M87C196KD information.
2. Deleted the memory map figure.*
3. Deleted the horizontal windowing figure.*
4. Deleted the SFR bit summaries.*
5. Added the new CLKOUT disable feature.
6. Modified the V_{IH2} and I_{CC} DC specifications.
7. Modified the T_{LLYV}, T_{LLGV}, T_{RLDV}, T_{RHDZ}, T_{LLCH}, T_{LHLL}, T_{LLAX}, T_{LLRL}, T_{RLAZ}, and T_{WHQX} AC specifications.
8. Modified the T_{HALBZ} and T_{HAHAX} HOLD/HLDA specifications.
9. Added the package thermal characteristics.

*See the 87C196KC/KD User's Manual (order #272238) for this information.

2.3 Ceramic Pin Grid Array Package

2.3.1 Symbol List for Square Ceramic Pin Grid Array Family

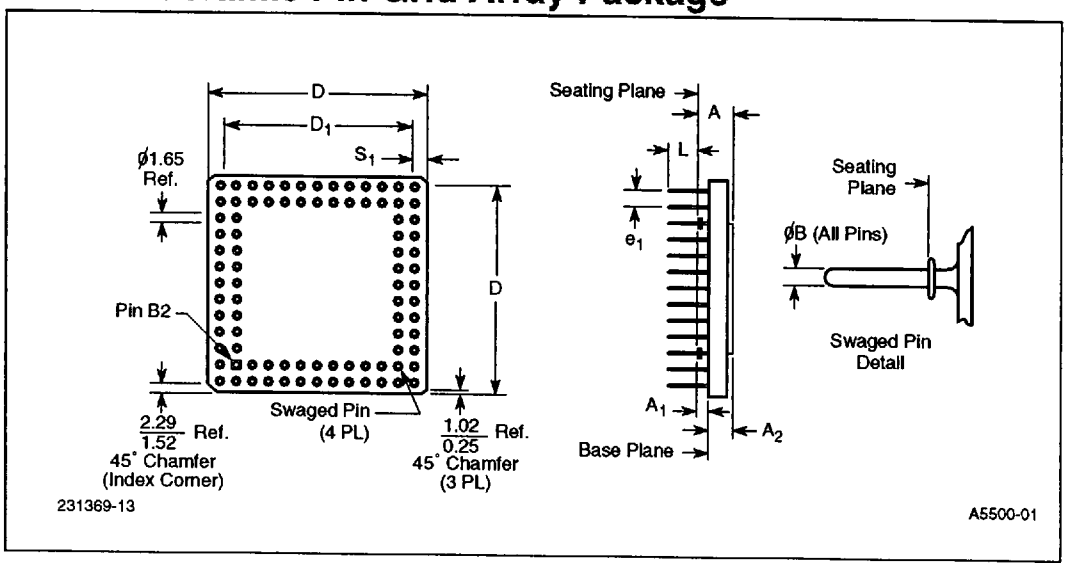
Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A_1	Distance between seating plane and base plane
A_2	Distance from base plane to highest point of body
A_3	Distance from seating plane to bottom of body
A_4	Heat spreader thickness
B	Diameter of terminal lead pin
D	Largest overall package dimension of length
D_1	A body length dimension, outer lead center to outer lead center
D_2	Heat spreader length and width
e_1	Linear spacing between true lead position centerlines
L	Distance from seating plane to end of lead
N	The total number of potentially usable lead positions
S_1	Other body dimension, outer lead center to edge of body

NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415 - 0.0430 inch.
4. Dimensions "B", "B_1" and "C" are normal.
5. Details of Pin 1 identifier are optional

Packaging Family Attributes	
Category	Ceramic Pin Grid Array
Acronym	C-PGA or PGA
Lead Configuration	Array
Lead Counts	68, 88, 132, 168-208, 240-280, 272-320
Lead Finish	Gold Plate, 60 Microinches of Gold over 100-350 Microinches of Nickel Plate
Lead Material	Alloy 42 or Kovar
Lead Braze Material	Copper/Silver Eutectic
Lead Pitch	0.100"
Board Assembly Type	Socket and Insertion Mount

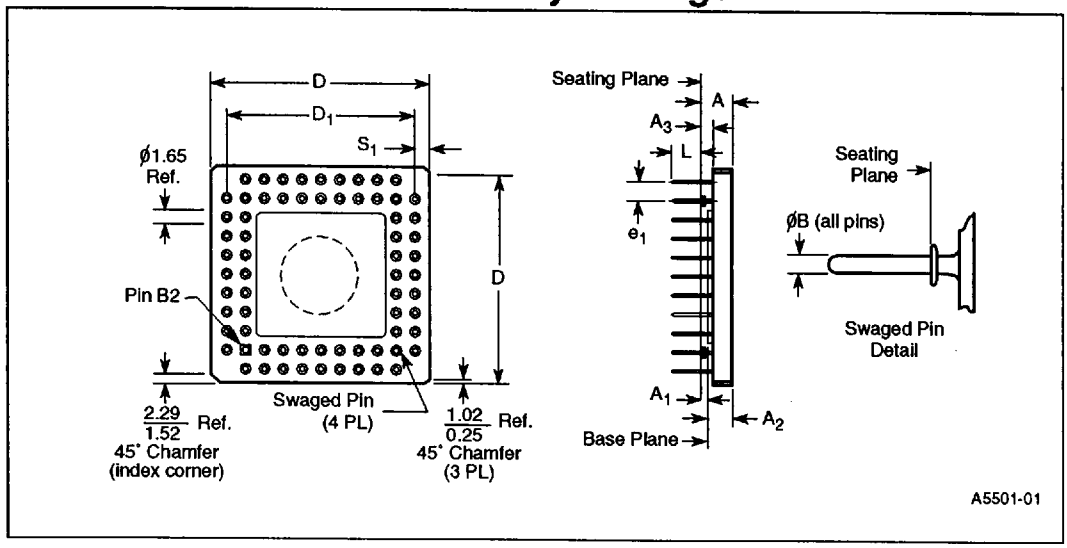
NOTES:
1. Alloy 42 or Kovar Leads.
2. Multilayer Co-Fired Ceramic Body.
3. 240-280 has variable pin count.

2.3.2 88 Lead Ceramic Pin Grid Array Package



Family: Ceramic Pin Grid Array Package (Cavity Up)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	4.06	5.21	EPROM Lid	0.160	0.205	EPROM Lid
A	3.30	4.32	Solid Lid	0.130	0.170	Solid Lid
A_1	1.14	1.40		0.045	0.055	
A_2	2.16	3.18	Solid Lid	0.085	0.125	Solid Lid
A_2	2.67	3.94	EPROM Lid	0.105	0.155	EPROM Lid
B	0.43	0.51		0.017	0.020	
D	34.04	35.05		1.340	1.380	
D_1	30.35	30.61		1.195	1.205	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.56		0.120	0.140	
N	88			88		
S_1	1.27	2.54		0.050	0.100	

2.3.3 68 Lead Ceramic Pin Grid Array Package



Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A_1		0.41	EPROM Lid		0.016	EPROM Lid
A_2	2.72	3.43	Solid Lid	0.107	0.135	Solid Lid
A_2	3.43	4.32	EPROM Lid	0.135	0.170	EPROM Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	28.95	29.97		1.140	1.180	
D_1	25.27	25.53		0.995	1.005	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	68			68		
S_1	1.27	2.54		0.050	0.100	

2.4 Ceramic Quad Flatpack Package

2.4.1 Symbol List for Ceramic Quad Flatpack Family

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body (lid)
A_1	Ceramic body thickness
B	Width of terminal leads
C	Thickness of terminal leads
D	Largest overall package dimension of length
D_1	Largest overall package dimension of length excluding leads
D_2	A body length dimension, outer lead center to outer lead center
e_1	Linear spacing between centerlines of terminal leads
L	Lead dimension free lead length
N	The total number of potentially usable lead positions
S	Distance from true position centerline of end lead position to the extremity of the body
S_1	Linear spacing of true maximum lead position from lead edge to package edge

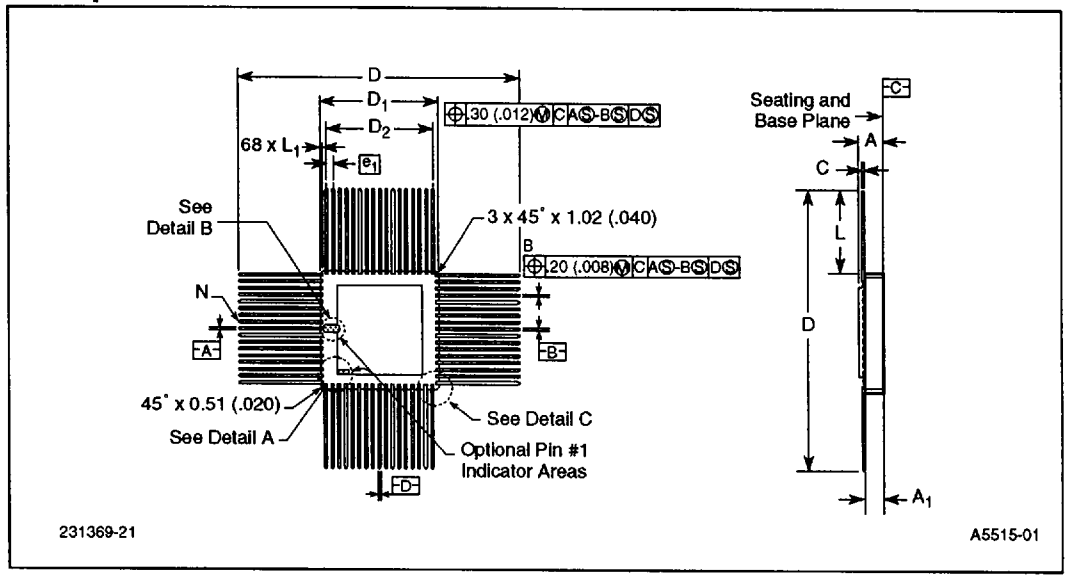
NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Pin numbering is ascending in the counterclockwise direction.
4. Dimensions "B", "B_1" and "C" are nominal.

Packaging Family Attributes	
Category	Ceramic Quad Flatpack
Acronym	CQFP
Lead Configuration	Quad
Lead Counts	68
Lead Finish	Gold Plate or SolderCoat
Lead Pitch	0.050"
Board Assembly Type	Socket and Surface Mount

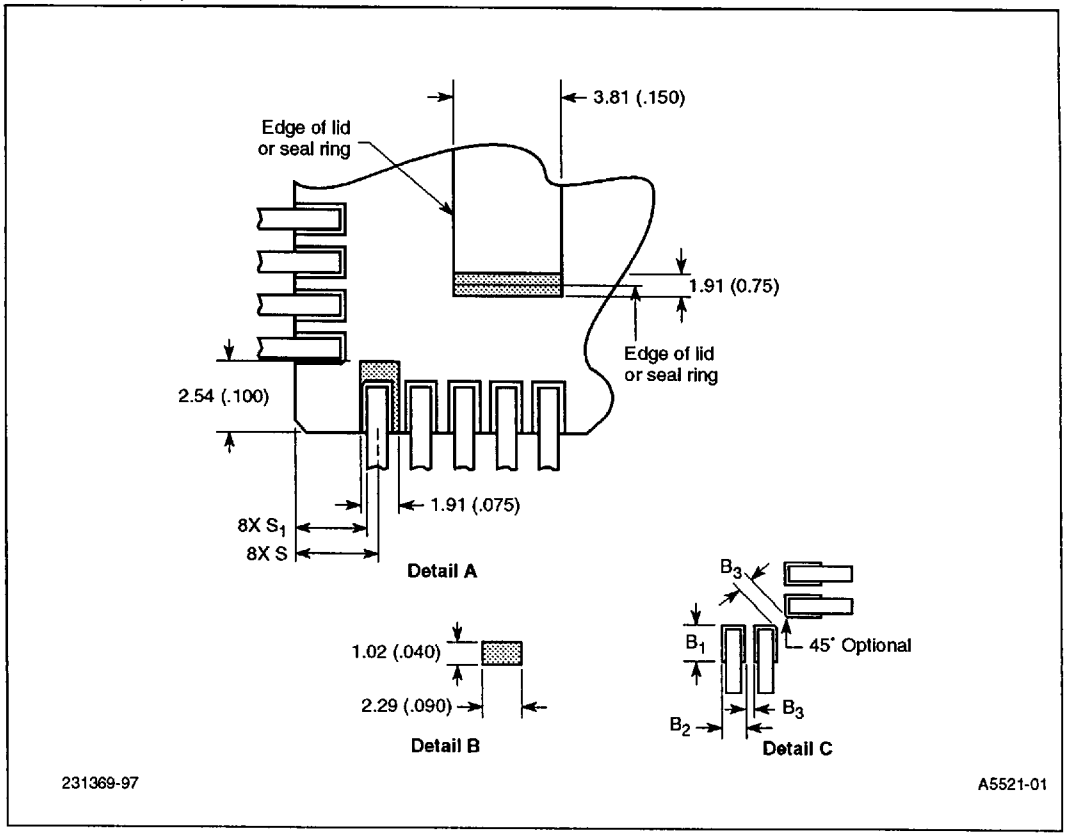
NOTES:
1. Alloy 42 or Kovar leads.
2. Sold unformed in carrier.

2.4.2 68 Lead Ceramic Quad Flatpack Package

2.4.2.1 Principle Dimensions and Datums



2.4.2.2 Details A, B, C



2.4.3 Ceramic Quad Flatpack Package

Family: 68 Lead Ceramic Quad Flatpack Family						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.23	2.69	Solid Lid	0.088	0.106	Solid Lid
A	2.91	3.68	EPROM Lid	0.115	0.145	EPROM Lid
A_1	1.98	2.39		0.078	0.094	
B	0.41	0.53	68 Places	0.016	0.021	68 Places
B_1	1.02	1.52	Typical	0.040	0.060	Typical
B_2	0.76	1.02	Typical	0.030	0.040	Typical
B_3	0.13	0.51	Typical	0.005	0.020	Typical
C	0.20	0.31		0.008	0.012	
D	41.66	47.50		1.640	1.870	
D_1	23.52	24.64		0.926	0.970	
D_2	20.32		BSC	0.800		BSC
e_1	1.27 BSC		64 Places	0.050 BSC		64 Places
L	8.89	11.43		0.350	0.450	
L_1	1.02	1.52		0.040	0.060	
N	68			68		
S	1.91		REF	0.075		REF
S_1	1.27			0.050		