2.5-Gbps Programmable Serial Interface™

Features

- **High-speed (HS) Programmable Serial Interface™ (PSI™)**
- **2.48- to 2.5-Gbps serial signaling rate**
- **Full Bellcore and ITU jitter compliance**
- **Flexible parallel-to-serial conversion in transmit path**
- **Flexible serial-to-parallel conversion in receive path**
- **Multiple selectable loopback/loop-through modes**
- **100K of usable gates of CPLD logic**
- **240K of integrated memory**
  - **192K of synchronous or asynchronous SRAM**
  - **48K of true Dual-Port or FIFO RAM**
- **Internal transmit and receive phase-locked loops (PLLs)**
- **Logic dedicated Spread Aware™ PLL**
- **Transmit FIFO for flexible variable phase clocking**
- **Differential CML serial input with internal termination and DC-restoration**
- **Differential CML serial output with source-matched impedance of 50Ω**
- **240 user-programmable I/Os**
- **Any Volt™ I/O interface**
  - **Programmable as 1.5V, 1.8V, 2.5V, 3.3V**
- **Multiple I/O standards**
  - **LVCMOS, LVTTL, 3.3V PCI, SSTL2(I-II), SSTL3(I-II), HSTL(I-IV), and GTL+**
  - **Fully PCI-compliant (Rev. 2.2)**
- **Direct interface to standard fiber-optic modules**
- **Designed to drive:**
  - **Fiberoptic modules**
  - **Copper cables**
  - **Circuit board traces**
  - **Backplane links**
  - **Box-to-box links**
  - **Chip-to-chip communication**
- **Extremely flexible clocking options**
  - **Four global clocks**
  - **Up to 192 additional product term clocks**
  - **Clock polarity at every register**
- **Carry chain logic for fast and efficient arithmetic operations**
- **JTAG programming interface with boundary scan support**
- **Power-saving mode**
- **Supported standards:**
  - **SONET OC-48 and SDH STM-16**
  - **InfiniBand™**
  - **Custom 2.5-Gbps interface**

Development Software

- ***Warp®***
  - **IEEE 1076/1164 VHDL or IEEE 1364 Verilog context sensitive editing**
  - **Active-HDL FSM graphical finite state machine editor**
  - **Active-HDL SIM post-synthesis timing simulator**
  - **Architecture Explorer for detailed design analysis**
  - **Static Timing Analyzer for critical path analysis**
  - **Available on Windows® 9x, 2000, NT 4.0, XP, and ME**
  - **Supports all Cypress programmable logic products**

2.5-Gbps PSI Family—Standards Supported

	PSI Device	SONET/SDH (OC48/STM16)	InfiniBand	Custom
SONET/SDH	CYS25G01K100	X		X
High Speed	CYP25G01K100		X	X

2.5-Gbps PSI Family—General Features

Device	Typical Gates	Macrocells	Cluster Memory (Kbits)	Channel Memory (Kbits)	Maximum User-Programmable I/O	Package Offering
25G01K100	46K–144K	1536	192	48	240	456-BGA (35 × 35 mm, 1.27-mm pitch)

2.5-Gbps PSI Family—Performance

Device	Channels and Link Speed	Total Bandwidth	f_{MAX2}(Logic)[1] (MHz)	Logic Speed—t_{PD} Pin-to-Pin[1] (ns)
25G01K100	1 × 2.5 Gbps	2.5 Gbps	222	7.5

Note:
1. See the section titled Switching Characteristics for definition.

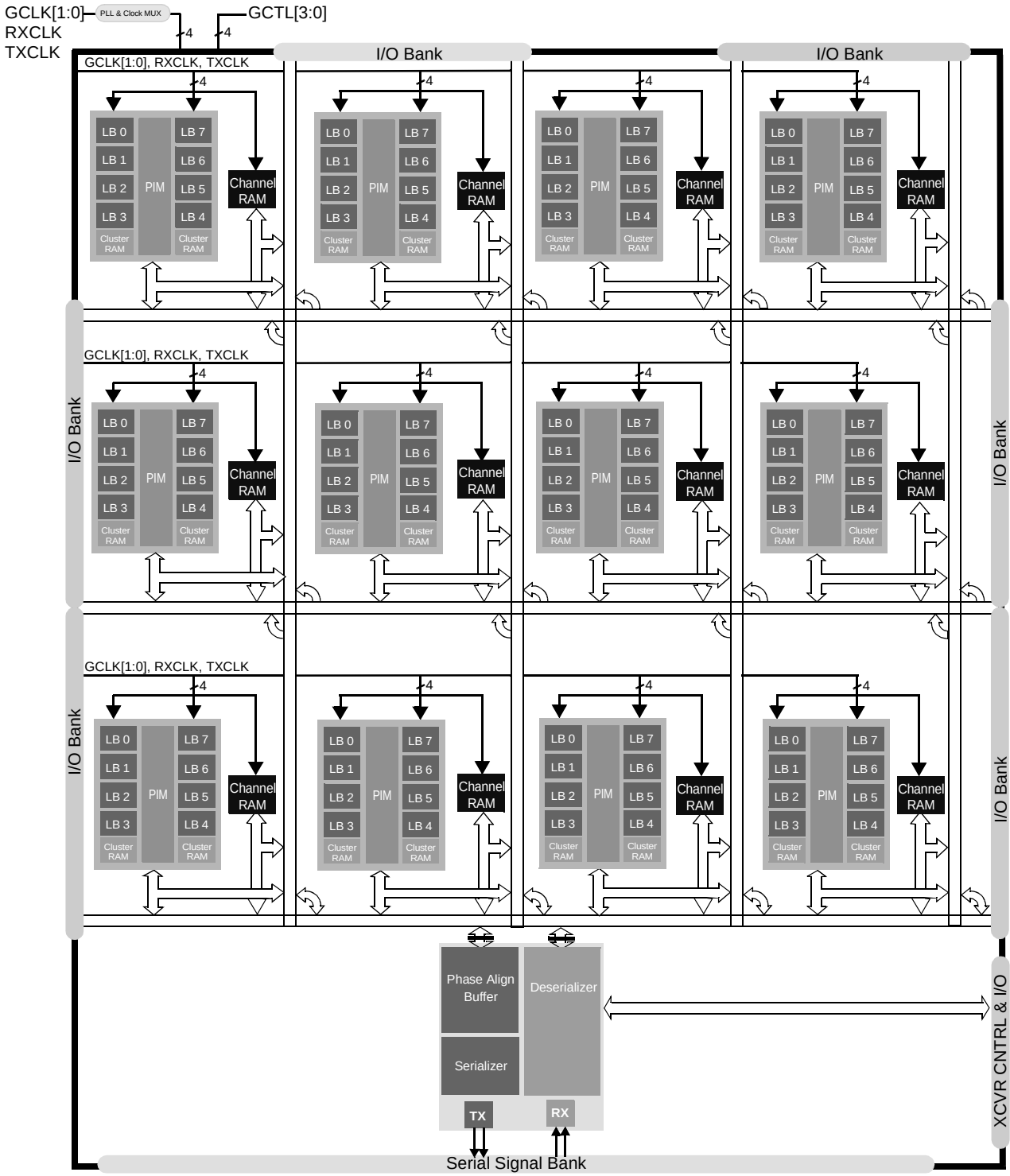


Figure 1. High-speed PSI™ Block Diagram (25G01K100) with I/O Bank Structure

Functional Description

The 2.5-Gbps PSI is a point-to-point or point-to-multipoint programmable communications building block allowing the manipulation and transfer of data over high-speed serial links at 2.5 Gbps per serial link. The 2.5-Gbps PSI is designed to combine the high speed, predictable timing, high density, low power, and ease of use of complex programmable logic devices (CPLD) with the serializing/deserializing (SERDES) capability of high-speed serial transceivers.

The architecture of the device is based on logic block clusters (LBC) and serial transceiver blocks that are connected by horizontal and vertical routing channels. Each LBC features eight individual logic blocks (LB) of 16 macrocells and two cluster memory blocks. Adjacent to each LBC is a channel memory block which is externally accessible through the I/O interface. Each transmit channel of the transceiver accepts 16 bit parallel characters, and converts it to serial data. Each receive channel accepts serial data and converts it to 16-bit parallel data, and presents these characters to the routing channels of the Programmable Logic.

High-speed Transceiver

The transceiver operation of the high-speed programmable serial interface devices is self-contained in a single block. It has a separate Transmit PLL (TXPLL) and a Receive Clock and Data Recovery PLL (RX CDR PLL) and a phase align buffer for flexible clocking. The transmit channel accepts a 16-bit input character from the routing channels and passes the character to the phase align buffer. This character is then serialized and output to differential CML output drivers at 2.5 Gbps. The receive channel accepts a serial bit-stream from the differential CML receiver. This bit-stream is deserialized and a 16-bit character is presented to the routing channels in the PSI device. The block also features loop-back and loop-through modes for simplified design debugging.

The transceiver block interfaces to the routing channels of the PSI device through highly configurable datapath cells. For specific architecture and operation of the transceiver blocks please refer to the Serial Transceiver Operation section (page 14).

The internal interfacing to the transceiver blocks of the high-speed device occur through the port definition of the high-speed transceiver block. The internal signals and their definition are described in the “Pin and Signal Description” section (page 38). These internal signals can be routed to the programmable logic by instantiation and port mapping them through hardware description using Warp Software.

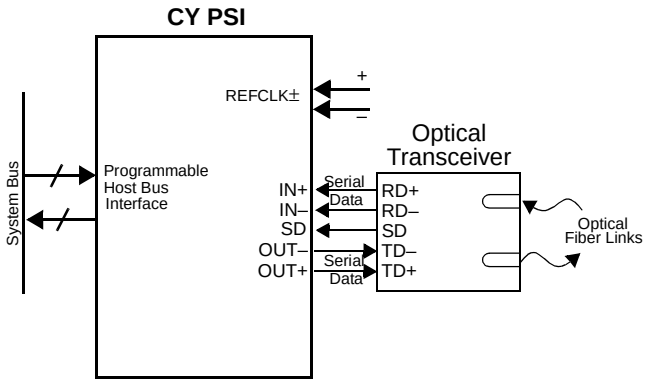


Figure 2. High-speed PSI System Connections with an Optical Interface

Standard Datapath Cell

Figure 3 is a block diagram of the PSI datapath cell. The datapath cell contains a three-state transmit buffer, a receive buffer, and a register that can be configured as a transmit or receive register.

The Transceiver Enable (TE) can be selected from one of the four global control signals(GCTL[0:3]) or from one of two Output Control Channel (OCC) signals. The transmit enable can be configured as always enabled or always disabled or it can be controlled by one of the remaining inputs to the mux. The selection is done via a mux that includes V_{CC} and GND as inputs.

One of the global clocks(GCLK[1:0], TXCLK or RXCLK) can be selected as the clock for the datapath cell register. The clock mux output is an input to a clock polarity mux that allows the transmit/receive register to be clocked on either edge of the clock.

Global Routing Description

The routing architecture in the PLD block of a PSI device is made up of horizontal and vertical (H&V) routing channels. These routing channels allow signals to move among I/Os, logic blocks and memories. In addition to the horizontal and vertical routing channels that interconnect the I/O banks, channel memory blocks, transceiver blocks and logic block clusters, each LBC contains a Programmable Interconnect Matrix™ (PIM™), which is used to route signals among the logic blocks and the cluster memory blocks in the LBC.

Figure 4 is a block diagram of the routing channels that interface within the PSI architecture.

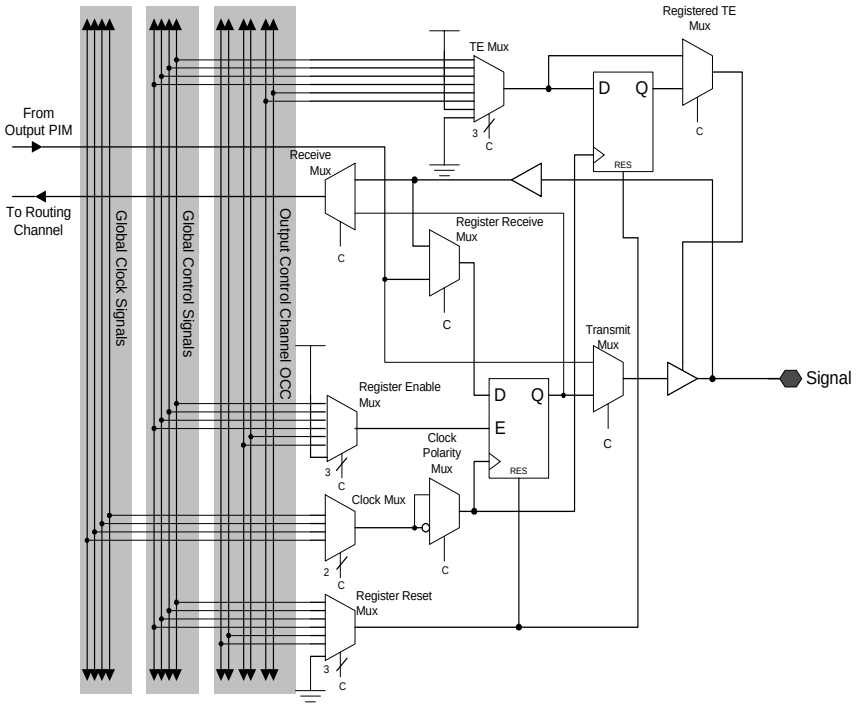


Figure 3. Block Diagram of a Standard Datapath Cell

Logic Block Cluster (LBC)

The PSI architecture consists of several logic block clusters, each of which have eight Logic Blocks (LBs) and two cluster memory blocks connected via a PIM, as shown in *Figure 5*. Each cluster memory block consists of 8-Kbit single-port RAM, which is configurable as synchronous or asynchronous. The cluster memory blocks can be cascaded with other cluster memory blocks within the same LBC as well as other LBCs to implement larger memory functions. If a cluster memory block is not specifically utilized by the designer, Cypress's *Warp* software can automatically use it to implement large blocks of logic.

All LBCs interface with each other via horizontal and vertical routing channels.

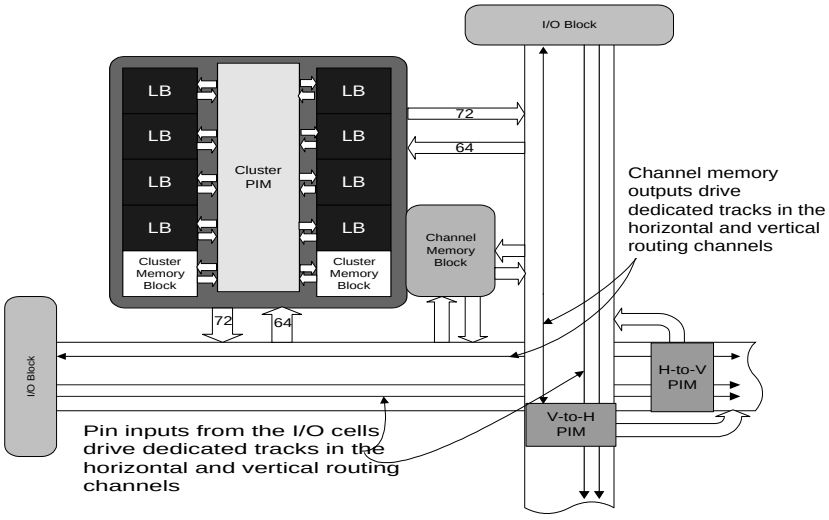


Figure 4. PSI Routing Interface

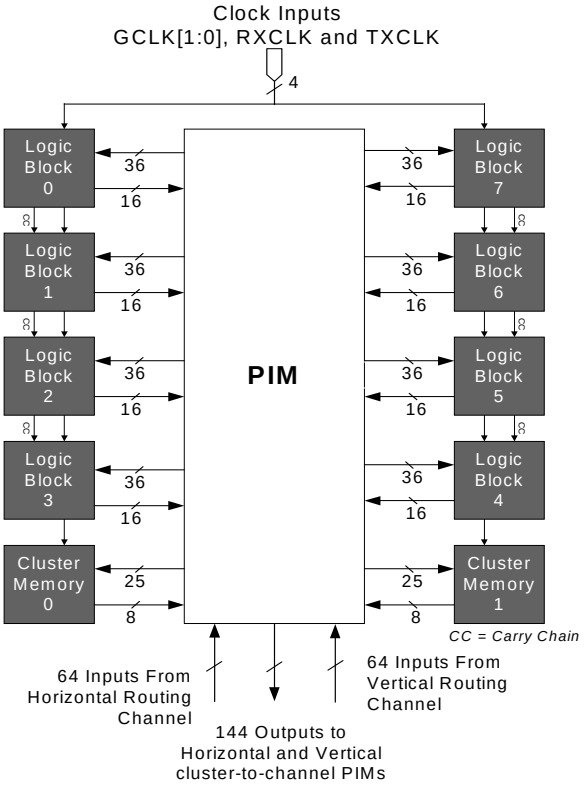


Figure 5. PSI Logic Block Cluster Diagram

Logic Block

The LB is the basic building block of the programmable logic block of the PSI architecture. It consists of a product term array, an intelligent product-term allocator, and 16 macrocells.

Product Term Array

Each LB features a 72 × 83 programmable product term array. This array accepts 36 inputs from the PIM. These inputs originate from device pins and macrocell feedbacks as well as cluster memory and channel memory feedbacks. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 83 product terms in the array can be created from any of the 72 inputs.

Of the 83 product terms, 80 are for general-purpose use for the 16 macrocells in the LB. Two of the remaining three product terms in the LB are used as asynchronous set and asynchronous reset product terms. The final product term is the Product Term clock (PTCLK) and is shared by all 16 macrocells within an LB.

Product Term Allocator

Through the product term allocator, *Warp* software automatically distributes the 80 product terms as needed among the 16 macrocells in the LB. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On PSI devices, product terms are steered on an individual basis. Any number between 1and 16 product terms can be steered to any macrocell.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one function has one or more product terms in its equation that are common to other functions, those product terms are only created once. The PSI product term allocator allows sharing across groups of four macrocells in a variable fashion. The software automatically takes advantage of this capability so that the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All steering and sharing configurations have been incorporated in the timing specifications for the PSI devices.

Macrocell

Within each LB there are 16 macrocells. Each macrocell accepts a sum of up to 16 product terms from the product term array. The sum of these 16 product terms can be output in either registered or combinatorial mode. *Figure 6* displays the block diagram of the macrocell. The register can be asynchronously preset or asynchronously reset at the macrocell level with the separate preset and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be preset or reset based on an AND expression or an OR expression.

An XOR gate in the PSI macrocell allows for many different types of equations to be realized. It can be used as a polarity mux to implement the true or complement form of an equation in the product term array or as a toggle to turn the D flip-flop into a T flip-flop. The carry-chain input mux allows additional flexibility for the implementation of different types of logic. The macrocell can utilize the carry chain logic to implement adders, subtractors, magnitude comparators, parity tree, or even generic XOR logic. The output of the macrocell is either registered or combinatorial.

Carry Chain Logic

The PSI macrocell features carry chain logic which is used for fast and efficient implementation of arithmetic operations. The carry logic connects macrocells in up to four LBs for a total of 64 macrocells. Effective data path operations are implemented through the use of carry-in arithmetic, which drives through the circuit quickly. *Figure 6* shows that the carry chain logic within the macrocell consists of two product terms (CPT0 and CPT1) from the PTA and an input carry-in for carry logic. The inputs to the carry chain mux are connected directly to the product terms in the PTA. The output of the carry chain mux generates the carry-out for the next macrocell in the LB as well as the local carry input that is connected to an input of the XOR input mux. Carry-in and a configuration bit are inputs to an AND gate. This AND gate provides a method of segmenting the carry chain in any macrocell in the LB.

Macrocell Clocks

Clocking of the register is highly flexible. Four global synchronous clocks (GCLK[1:0], RXCLK and TXCLK) and a Product Term clock (PTCLK) are available at each macrocell register. Furthermore, a clock polarity mux within each macrocell allows the register to be clocked on the rising or the falling edge (see macrocell diagram in *Figure 6*).

PRESET/RESET Configurations

The macrocell register can be asynchronously preset and reset using the PRESET and RESET mux. Both signals are active high and can be controlled by either of two Preset/Reset product terms (PRC[1:0] in *Figure 6*) or GND. In situations where the PRESET and RESET are active at the same time, RESET takes priority over PRESET.

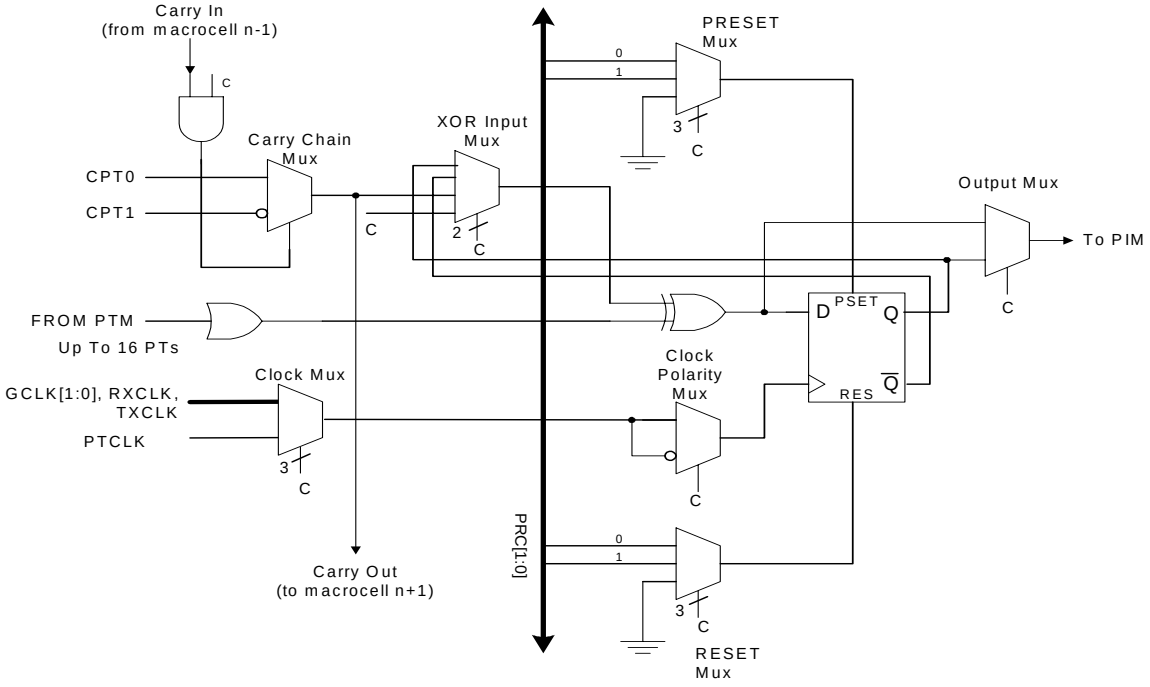


Figure 6. PSI Macrocell

Embedded Memory

The 2.5-Gbps PSI family contains two types of embedded memory blocks. The channel memory block is placed at the intersection of horizontal and vertical routing channels. Each channel memory block is 4096 bits in size and can be configured as asynchronous or synchronous Dual-Port RAM, Single-Port RAM, Read-Only memory (ROM), or synchronous FIFO memory. The memory organization is configurable as 4K × 1, 2K × 2, 1K × 4 and 512 × 8. The second type of memory block is located within each LBC and is referred to as a cluster memory block. Each LBC contains two cluster memory blocks that are 8192 bits in size. Similar to the channel memory blocks, the cluster memory blocks can be configured as 8K × 1, 4K × 2, 2K × 4 and 1K × 8 and can be configured as either asynchronous or synchronous Single-Port RAM or ROM.

Cluster Memory

Each LB cluster of the PSI device contains two 8192-bit cluster memory blocks. *Figure 7* is a block diagram of the cluster memory block and the interface of the cluster memory block to the cluster PIM.

The output of the cluster memory block can be optionally registered to perform synchronous pipelining or to register asynchronous read and write operations. The output registers contain an asynchronous RESET which can be used in any type of sequential logic circuits (e.g., state machines).

There are four global clocks and one local clock available for the input and the output registers. The local clock for the input registers is independent of the one used for the output registers. The local clock is generated in the user-design in a macrocell or comes from an I/O pin.

Cluster Memory Initialization

The cluster memory powers up in an undefined state, but is set to a user-defined known state during configuration. To facilitate the use of look-up-table (LUT) logic and ROM applications, the cluster memory blocks can be initialized with a given set of data when the device is configured at power up. For LUT and ROM applications, the user cannot write to memory blocks.

Channel Memory

The PSI architecture includes an embedded memory block at each crossing point of horizontal and vertical routing channels. The channel memory is a 4096-bit embedded memory block that can be configured as asynchronous or synchronous Single-Port RAM, Dual-Port RAM, ROM, or synchronous FIFO memory.

Data, address, and control inputs to the channel memory are driven from horizontal and vertical routing channels. All data and FIFO logic outputs drive dedicated tracks in the horizontal and vertical routing channels. The clocks for the channel memory block are selected from four global clocks and pin inputs from the horizontal and vertical channels. The clock muxes also include a polarity mux for each clock so that the user can choose an inverted clock.

Dual-Port (Channel Memory) Configuration

Each port has distinct address inputs, as well as separate data and control inputs that can be accessed simultaneously. The inputs to the Dual-Port memory are driven from the horizontal and vertical routing channels. The data outputs drive dedicated tracks in the routing channels. The interface to the routing is such that Port A of the Dual-Port interfaces primarily with the horizontal routing channel and Port B interfaces primarily with the vertical routing channel.

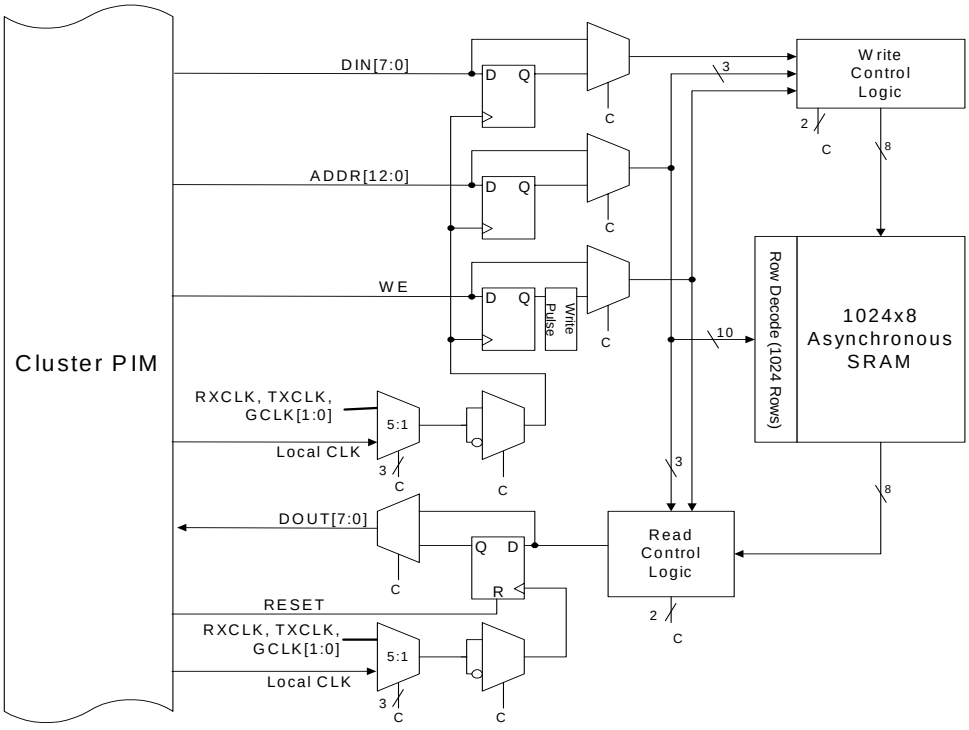


Figure 7. Block Diagram of Cluster Memory Block

The clocks for each port of the Dual-Port configuration are selected from four global clocks and two local clocks. One local clock is sourced from the horizontal channel and the other from the vertical channel. The data outputs of the dual-port memory can also be registered. Clocks for the output registers are also selected from four global clocks and two local clocks. One clock polarity mux per port allows the use of true or complement polarity for input and output clocking purposes.

Arbitration

The Dual-Port configuration of the Channel Memory Block provides arbitration when both ports access the same address at the same time. Depending on the memory operation being attempted, one port always gets priority. See *Table 1* for details on which port gets priority for read and write operations. An active-LOW 'Address Match' signal is generated when an address collision occurs.

Table 1. Arbitration Result: Address Match Signal Becomes Active

Port A	Port B	Result of Arbitration	Comment
Read	Read	No arbitration required	Both ports read at the same time
Write	Read	Port A gets priority	If Port B requests first then it will read the current data. The output will then change to the newly written data by Port A
Read	Write	Port B gets priority	If Port A requests first then it will read the current data. The output will then change to the newly written data by Port B
Write	Write	Port A gets priority	Port B is blocked until Port A is finished writing

FIFO (Channel Memory) Configuration

The channel memory blocks are also configurable as synchronous FIFO RAM. In the FIFO mode of operation, the channel memory block supports all normal FIFO operations without the use of any general-purpose logic resources in the device.

The FIFO block contains all of the necessary FIFO flag logic, including the read and write address pointers. The FIFO flags include an empty/full flag (EF), half-full flag (HF), and programmable almost-empty/full (PAEF) flag output. The FIFO configuration has the ability to perform simultaneous read and write operations using two separate clocks. These clocks may be tied together for a single operation or may run independently for asynchronous read/write (with reference to . each other) applications. The data and control inputs to the FIFO block are driven from the horizontal or vertical routing channels. The data and flag outputs are driven onto dedicated routing tracks in both the horizontal and vertical routing channels. This allows the FIFO blocks to be expanded by using multiple FIFO blocks on the same horizontal or vertical routing channel without any speed penalty.

In FIFO mode, the write and read ports are controlled by separate clock and enable signals. The clocks for each port are selected from four global clocks and two local clocks.

One local clock is sourced from the horizontal channel and the other from the vertical channel. The data outputs from the read port of the FIFO can also be registered. One clock polarity mux per port allows using true or complement polarity for read and write operations. The write operation is controlled by the clock and the write enable pin. The read operation is controlled by the clock and the read enable pin. The enable pins can be sourced from horizontal or vertical channels.

Channel Memory Initialization

The channel memory powers up in an undefined state, but is set to a user-defined known state during configuration. To facilitate the use LUT logic and ROM applications, the channel memory blocks can be initialized with a given set of data when the device is configured at power up. For LUT and ROM applications, the user cannot write to memory blocks.

Channel Memory Routing Interface

Similar to LBC outputs, the channel memory blocks feature dedicated tracks in the horizontal and vertical routing channels for the data outputs and the flag outputs, as shown in *Figure 8*. This allows the channel memory blocks to be expanded easily. These dedicated lines can be routed to I/O pins as chip outputs or to other LB clusters to be used in logic equations.

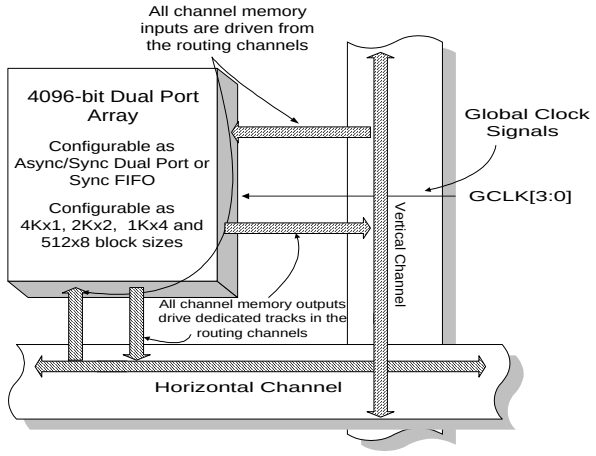


Figure 8. Block Diagram of Channel Memory Block

I/O Banks

The PSI interfaces the horizontal and vertical routing channels to the pins through I/O banks. There are several I/O banks per device as shown in *Figure 9* and all I/Os from an I/O bank are located in the same section of a package for PCB layout convenience. There exist two kinds of I/O banks; fixed-signal I/O banks and user programmable I/O banks.

The first fixed signal bank is the Serial Signal Bank. This bank includes all differential serial data transmission and receive signals. The second bank is the Transceiver Control Bank. This bank includes all static signal pins required for the configuration and operation of the transceiver blocks in each of the PSI devices.

Each PSI device has several types of user programmable I/O banks. The table in the next column (PSI programmable I/O Banks) indicates the availability of each type of programmable bank. Supported I/O standards for each bank are addressed by the appropriate V_{REF} and V_{CCIO} voltages. All the V_{REF} and V_{CCIO} pins in an I/O bank must be connected to the same V_{REF} and V_{CCIO} voltage respectively. This requirement restricts the number of I/O standards supported by an I/O bank at any given

time. It also dictates the I/O standard used for the GCTL[3:0] pins.

The architecture defining each programmable I/O bank consists of several I/O cells, where each I/O cell contains an input/output register, an output enable register, programmable slew rate control and programmable bus hold control logic. Each I/O cell drives a pin output of the device; the cell also supplies an input to the device that connects to a dedicated track in the associated routing channel.

There are four dedicated inputs (GCTL[3:0]) that are used as Global Control Signals available to every I/O cell. These global control signals may be used as output enables, register resets and register clock enables as shown in *Figure 10*. Each global control originates from a particular bank though they can be used to control any I/O cell in the device. The input signalling standard for a particular global control signal is same as the I/O standard for bank from which it originates.

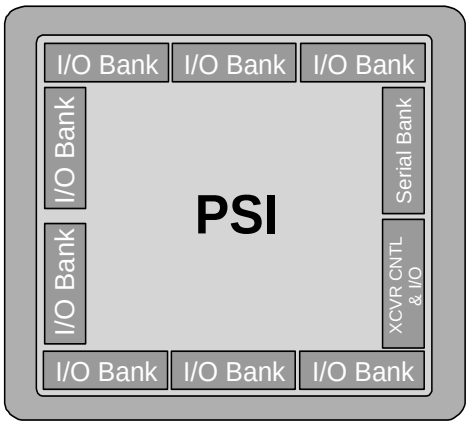


Figure 9. PSI I/O Bank Block Diagram

PSI Programmable I/O Banks

Device	Flexible	Semi-Flexible	Specific	
			V_{CCIO}	V_{REF}
25G01K100	Bank[0:3, 5]	Bank[4] V_{CCIO}=3.3V	Bank[6:7]	
			1.5V	0.68-0.90V

Table 2.

IO Standards

I/O Standard	V_{REF} (V)		V_{CCIO}	Termination Voltage (V_{TT})
	Min	Max		
LVTTL	N/A		3.3 V	N/A
LVCMOS			3.3 V	N/A
LVCMOS3			3.0 V	N/A
LVCMOS2			2.5 V	N/A
LVCMOS18			1.8 V	N/A
3.3V PCI			3.3 V	N/A
GTL+	0.9	1.1	N/A	1.5
SSTL3 I	1.3	1.7	3.3 V	1.5
SSTL3 II	1.3	1.7	3.3 V	1.5
SSTL2 I	1.15	1.35	2.5 V	1.25
SSTL2 II	1.15	1.35	2.5 V	1.25
HSTL I	0.68	0.9	1.5 V	0.75
HSTL II	0.68	0.9	1.5 V	0.75
HSTL III	0.68	0.9	1.5 V	1.5
HSTL IV	0.68	0.9	1.5 V	1.5

I/O Banks for Global Controls

	GCTL[0]	GCTL[1]	GCTL[2]	GCTL[3]
Bank	0	5	6	7

I/O Banks for Global CLKs

	GCLK[0]	GCLK[1]
Bank	0	5

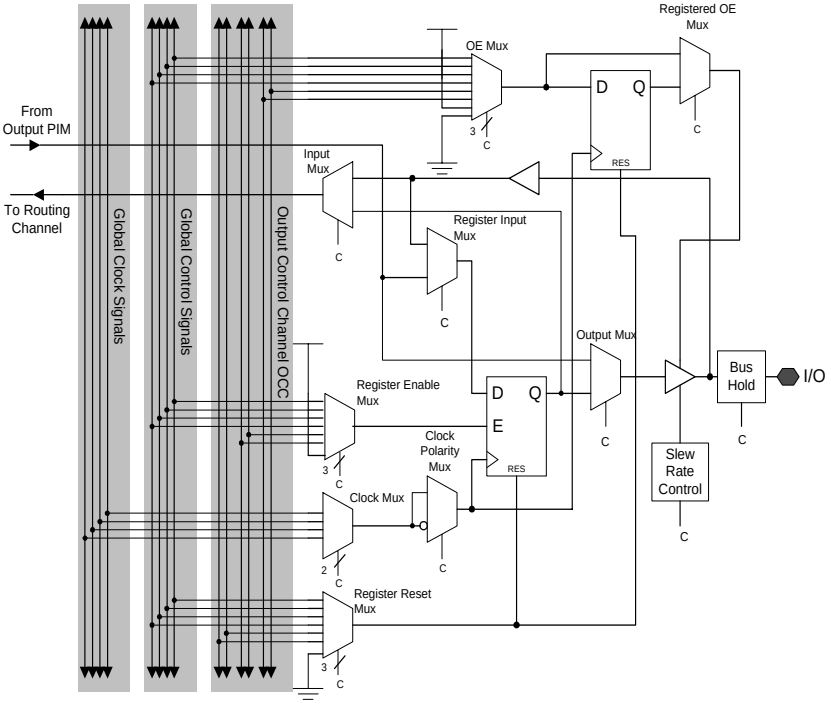


Figure 10. Block Diagram of I/O Cell

I/O Cell

Figure 10 is a block diagram of the PSI I/O cell. The I/O cell contains a three-state input buffer, an output buffer, and a register that can be configured as an input or output register. The output buffer has a slew rate control option that can be used to configure the output for a slower slew rate. The input of the device and the pin output can each be configured as registered or combinatorial, however only one path can be configured as registered in a given design.

The output enable can be selected from one of the four global control signals or from one of two OCC signals. The output enable can be configured as always enabled or always disabled or it can be controlled by one of the remaining inputs to the mux. The selection is done via a mux that includes V_{CC} and GND as inputs.

One of the global clocks can be selected as the clock for the I/O cell register. The clock mux output is an input to a clock polarity mux that allows the input/output register to be clocked on either edge of the clock.

Slew Rate Control

The output buffer has a slew rate control option. This allows the ouput buffer to slew at a fast rate (3 V/ns) or a slow rate (1 V/ns). All I/Os default to fast slew rate. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

Programmable Bus Hold

On each I/O pin, user-programmable bus-hold is included. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note "Understanding Bus-Hold – A Feature of Cypress CPLDs."

Clocks

PSI has four primary internal global clock trees in the CPLD portion of the device (INTCLK[3:0]). Each of these clock trees distributes a clock signal to every cluster, channel memory, and I/O cell in the CPLD. The global clock trees are designed such that the clock skew is minimized while maintaining an acceptable clock delay. Each of the internal global clocks can choose from two input sources for the clock signal: a PLL derived output or another one as shown in the table below.

Device	IN-TCLK[0]	IN-TCLK[1]	IN-TCLK[2]	IN-TCLK[3]
25G01K100	GCLK[0]	GCLK[1]	TXCLK	RXCLK

GCLK[0] and GCLK[1] are accessible through pins on the device package. TXCLK and RXCLK are provided internally to the device. TXCLK (transmit clock) is intended for data transfer from the CPLD block to the transmit channel of the transceiver block. RXCLK (receive clock) is intended for data transfer from the receive channel of the transceiver block to the CPLD block. The TXCLK and RXCLK can also be used for logic inside the CPLD block, e.g., for data processing.

Clock Tree Distribution

The global clock tree performs two primary functions. First, the clock tree generates the four internal global clocks by multiplexing four reference clocks derived from the Transceiver Blocks and from the package pins and four PLL driven clocks. Second, the clock tree distributes the four global clocks to every cluster, channel memory, I/O block, and datapath cell on the die. The global clock tree is designed such that the clock skew is minimized while maintaining an acceptable clock delay.

Spread Aware™ PLL

The 2.5-Gbps PSI device features an on-chip PLL designed using Spread Aware™ technology for low EMI applications. In general, PLLs are used to implement time-division-multiplex circuits to achieve higher performance with fewer device resources.

For example, a system that operates on a 32-bit data path that runs at 40 MHz can be implemented with 16-bit circuitry that runs internally at 80 MHz. PLLs can also be used to take advantage of the positioning of the internally generated clock edges to shift performance towards improved setup, hold or clock-to-out times.

There are several frequency multiply (X1, X2, X3, X4, X5, X6, X8, X16) and divide (/1, /2, /3, /4, /5, /6, /8, /16) options available to create a wide range of clock frequencies from a single clock input (GCLK[0]). For increased flexibility, there are seven phase shifting options which allow clock skew/de-skew by 45°, 90°, 135°, 180°, 225°, 270°, or 315°.

The Spread Aware feature refers to the ability of the PLL to track a spread-spectrum input clock such that its spread is seen on the output clock with the PLL staying locked. The total amount of spread on the input clock should be limited to 0.6% of the fundamental frequency. Spread Aware feature is supported only with X1, X2 and X4 multiply options.

The Voltage Controlled Oscillator (VCO), the core of the PSI PLL is designed to operate within the frequency range of 100 MHz to 266 MHz. Hence, the multiply option combined with input (GCLK[0]) frequency should be selected such that this VCO operating frequency requirement is met. This is demonstrated in *Table 3* (columns 1, 2, and 3).

Another feature of this PLL is the ability to drive the output clock (INTCLK) off the PSI chip to clock other devices on the board, as shown in *Figure 11* below. This off-chip clock is half the frequency of the output clock as it has to go through a register (I/O register or a macrocell register).

This PLL can also be used for board deskewing purpose by driving a PLL output clock off-chip, routing it to the other devices on the board and feeding it back to the PLL's external feedback input (GCLK[1]). When this feature is used, only limited multiply, divide and phase shift options can be used. *Table 3* describes the valid multiply and divide options that can be used without an external feedback. *Table 4* describes the valid multiply and divide options that can be used with an external feedback.

Table 5 describes the valid phase shift options that can be used with or without an external feedback.

Table 6 is an example of the effect of all the available divide and phase shift options on a VCO output of 250 MHz. It also shows the effect of division on the duty cycle of the resultant clock. Note that the duty cycle is 50-50 when a VCO output is divided by an even number. Also note that the phase shift applies to VCO output and not to the divided output.

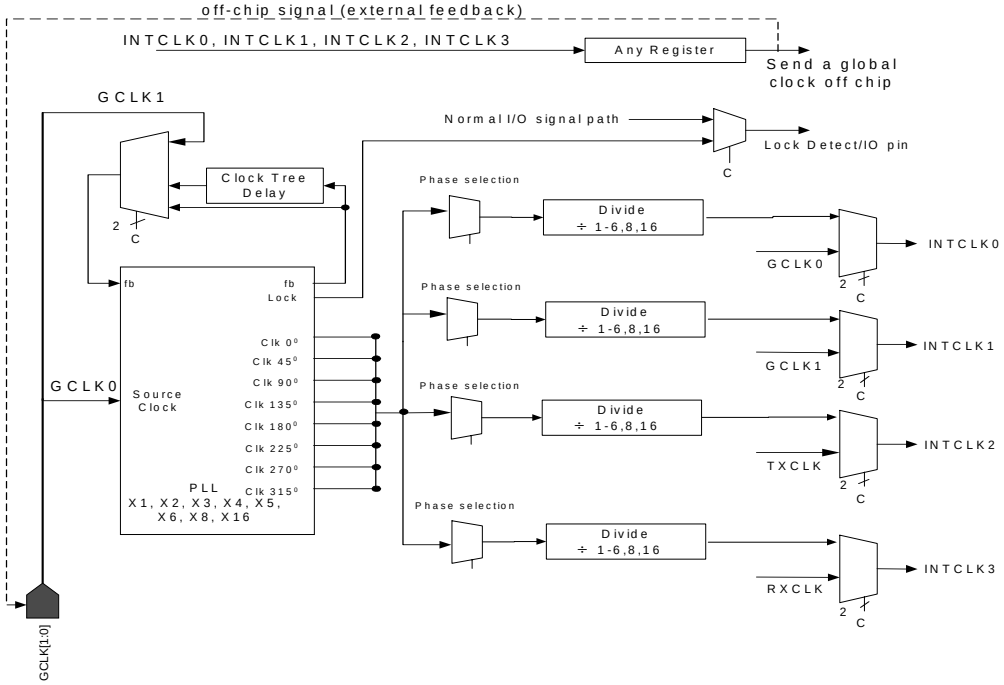


Figure 11. Block Diagram of Spread Aware PLL for CYP25G01K100

Table 3. PLL Multiply and Divide Options—without INTCLK1 Feedback

Input Frequency (GCLK[0]) f_{PLLI} (MHz)	Valid Multiply Options		Valid Divide Options		
	Value	VCO Output Frequency (MHz)	Value	Output Frequency (INTCLK[3:0]) f_{PLLO} (MHz)	Off-chip Clock Frequency
DC–12.5	N/A	N/A	N/A	DC–12.5	DC–6.25
100–133	1	100–133	1–6, 8, 16	6.25–133	3.125–66
50–133	2	100–266	1–6, 8, 16	6.25–266	3.125–133
33.3–88.7	3	100–266	1–6, 8, 16	6.25–266	3.1–266
25–66	4	100–266	1–6, 8, 16	6.25–266	3.125–133
20–53.2	5	100–266	1–6, 8, 16	6.25–266	3.1–133
16.6–44.3	6	100–266	1–6, 8, 16	6.25–266	3.1–133
12.5–33	8	100–266	1–6, 8, 16	6.25–266	3.125–133
12.5–16.625	16	200–266	1–6, 8, 16	6.25–266	3.125–133

Table 4. PLL Multiply and Divide Options—with External Feedback

Input (GCLK) Frequency f_{PLLI} (MHz)	Valid Multiply Options		Valid Divide Options		
	Value	VCO Output Frequency (MHz)	Value	Output (INTCLK) Frequency f_{PLLO} (MHz)	Off-chip Clock Frequency
50–133	1	100–266	1	100–266	50–133
25–66.5	1	100–266	2	50–133	25–66.5
16.67–44.33	1	100–266	3	33.33–88.66	16.67–44.33
12.5–33.25	1	100–266	4	25–66.5	12.5–33.25
12.5–26.6	1	125–266	5	25–53.2	12.5–26.6
12.5–22.17	1	150–266	6	25–44.34	12.5–22.17
12.5–16.63	1	200–266	8	25–33.25	12.5–16.63

Table 5. PLL Phase Shift Options with and without INTCLK1 Feedback

Without External Feedback	With External Feedback
0°,45°, 90°, 135°, 180°, 225°, 270°, 315°	0°

Table 6. Timing of Clock Phases for all Divide Options for a VCO Output Frequency of 250 MHz

Divide Factor	Period (ns)	Duty Cycle%	0° (ns)	45° (ns)	90° (ns)	135° (ns)	180° (ns)	225° (ns)	270° (ns)	315° (ns)
1	4	40–60	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
2	8	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
3	12	33–67	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
4	16	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
5	20	40–60	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
6	24	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
8	32	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
16	64	50	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5

Timing Model

One important feature of the 2.5-Gbps PSI is the simplicity of its timing. All combinatorial and registered/synchronous delays are worst case and system performance is static (as shown in the AC specs section) as long as data is routed through the same horizontal and vertical channels. *Figure 12* illustrates the true timing model for the programmable LB of the device. For synchronous clocking of macrocells, a delay is incurred from macrocell clock to macrocell clock of separate LBs within the same cluster, as well as separate LBs within different clusters. This is shown as t_{SCS} and t_{SCS2} in *Figure 12.* For combinatorial paths, any input to any output (from corner to corner on the device), incurs a worst-case delay in the 100K gate PSI regardless of the amount of logic or which horizontal and vertical channels are used. This is the t_{PD} shown in *Figure 12.* For synchronous systems, the input set-up time to the output macrocell register and the clock to output time are shown as the parameters t_{MCS} and t_{MCCO} shown in the

Figure 12. These measurements are for any output and synchronous clock, regardless of the logic placement.

PSI features:

- **no dedicated vs. I/O pin delays**
- **no penalty for using 0–16 product terms**
- **no added delay for steering product terms**
- **no added delay for sharing product terms**
- **no output bypass delays**.

The simple timing model of the 2.5-Gbps PSI eliminates unexpected performance penalties.

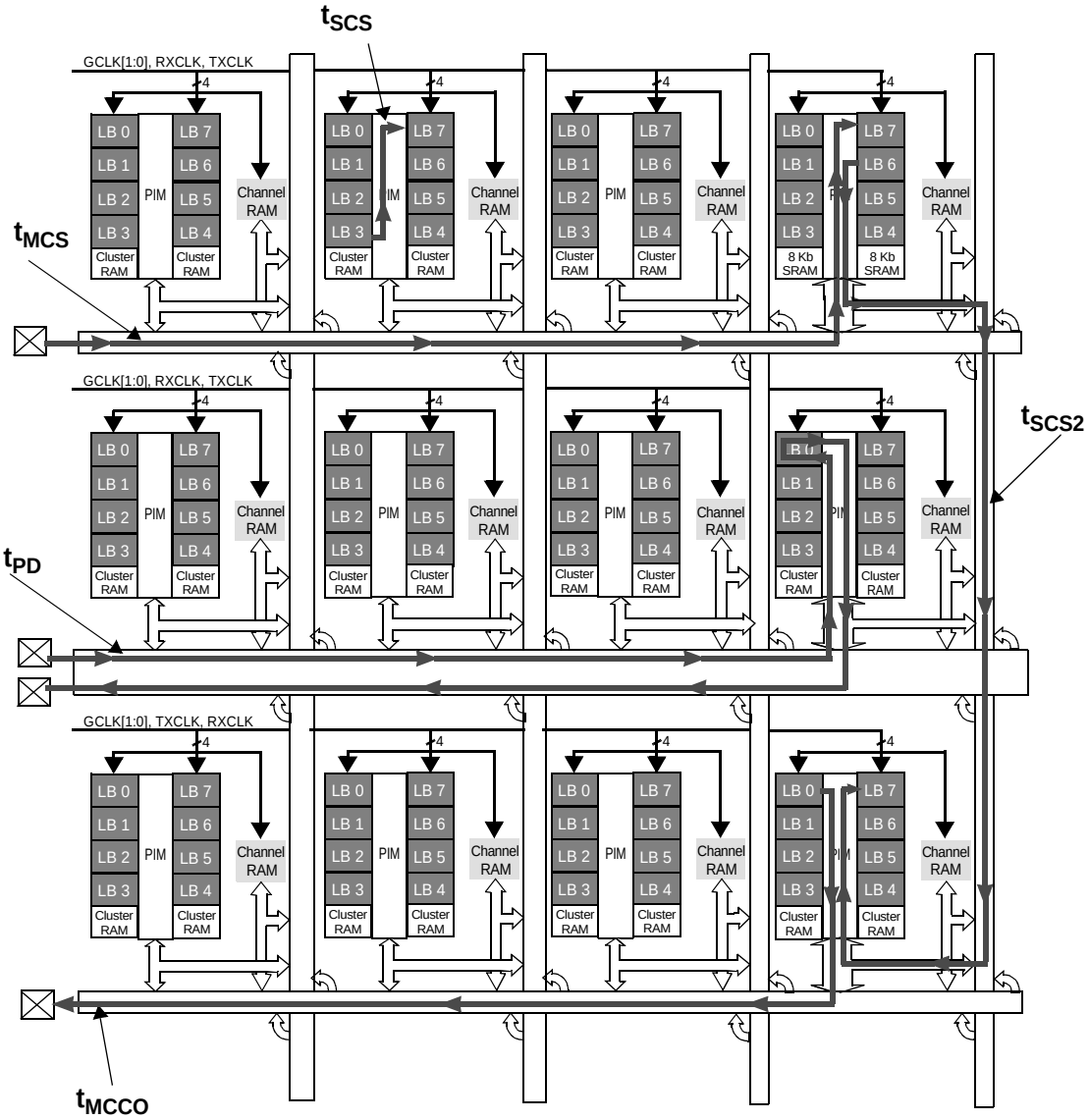


Figure 12. Timing Model for 100K gate PSI Devices

Serial Transceiver Operation

The PSI transceiver block is a highly configurable transceiver designed to support reliable transfer of large quantities of data, using high-speed serial links, from one or multiple sources to one or multiple destinations. This block supports serialization of a 16-bit dataword in the transmit side, and clock recovery and deserialization on the receive side. The interconnection between the serial transceiver block and the embedded programmable logic has to be specified using hardware description in Warp Software.

High-speed PSI Transceiver Operation

Registering TXD[15:0] Data Before it enters Serial Transceiver Block

Before the 16-bit parallel input data TXD[15:0] enters the serial transceiver block, it is required to register this data in a standard data path cell without any output enables. It is also required that these datapath cells are clocked on the rising edge of the global TXCLK.

Transmit Data Path

The registered 16-bit parallel TXD input data from the programmable LB of the device is input into the input register of the serial transceiver block. This input register is clocked using TXCLK, which is one of the four global clocks of the programmable logic.

Phase-Align Buffer

Data from the input register is passed to a phase-align buffer (FIFO). This buffer is used to absorb clock phase differences between the transmit input clock entering the serial transceiver and the internal character clock.

Initialization of the phase-align buffer takes place when the FIFO_RST signal is asserted LOW. When FIFO_RST is returned HIGH, the present input clock phase relative to TXCLK is set. Once set, the input clock is allowed to skew in time up to half a character period in either direction relative to REFCLK (i.e., ±180). This time shift allows the delay path of the character clock (relative to REFCLK) to change due to operating voltage and temperature while not effecting the desired operation. FIFO_RST is an asynchronous signal. FIFO_ERR is the transmit FIFO Error indicator. When HIGH, the transmit FIFO has either under or overflowed. The FIFO can be externally reset or logically reset by PSI logic to clear the error indication or if no action is taken, the internal clearing mechanism will clear the FIFO in nine clock cycles. When the FIFO is being reset, the output data is 1010.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts an external clock at the REFCLK input, and multiplies that clock by 16 to generate a bit-rate clock (2.5 Gbps) for use by the transmit shifter. The operating serial signaling rate and allowable range of REFCLK frequencies are listed in the High-speed PSI Transceiver Timing Parameter Values table under “REFCLK Timing Parameters” (see page 24). The REFCLK± input is a standard LVPECL input.

Serializer

The parallel data from the phase-align buffer is passed to the Serializer which converts the parallel data to serial data using the bit-rate clock generated by the Transmit PLL clock multiplier. TXD[15] is the most significant bit of the output word, and is transmitted first on the serial interface.

Serial Output Driver

The serial interface Output Driver makes use of high-performance differential CML (Current Mode Logic) to provide a source-matched driver for the transmission lines. This driver receives its data from the Transmit Shifters or the receive loopback data. The outputs have signal swings equivalent to that of standard LVPECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

Receive Data Path

Serial Line Receivers

A differential line receiver, IN±, is available for accepting the input serial data stream. The serial line receiver inputs can accommodate high wire interconnect and filtering losses or transmission line attenuation ($V_{SE} \geq$ 25 mV, or 50 mV peak-to-peak differential), and can be AC-coupled to +3.3V or +5V powered fiber-optic interface modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages.

Lock to Data Control

Line Receiver routed to the clock and data recovery PLL is monitored for

- **status of signal detect (SD) pin**
- **status of LOCKREF pin**
- **received data stream outside normal frequency range (±100 ppm)**.

This status is presented on the $\overline{\text{LFI}}$ (Line Fault Indicator) output signal, which changes asynchronously in the cases when SD or LOCKREF goes from HIGH to LOW. Otherwise, it changes synchronously to the REFCLK.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of data bits from received serial stream is performed by a Clock/Data Recovery (CDR) block. The clock extraction function is performed by high-performance embedded PLL that tracks the frequency of the incoming bit stream and aligns the phase of the internal bit-rate clock to the transitions in the selected serial data stream.

CDR accepts a character-rate (bit-rate ÷ 16) reference clock on the REFCLK input. This REFCLK input is used to ensure that the VCO (within the CDR) is operating at the correct frequency (rather than some harmonic of the bit-rate), to improve PLL acquisition time, and to limit unlocked frequency excursions of the CDR VCO when no data is present at the serial inputs.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits set by the range controls, the CDR PLL will track REFCLK instead of the data stream. When the frequency of the selected data stream returns to a valid frequency, the CDR PLL is allowed to track the received data stream. The frequency of REFCLK is required to be within ±100 ppm of the frequency of the clock that drives the REFCLK signal of the remote transmitter to ensure a lock to the incoming data stream.

External Filter

The CDR circuit uses external capacitors for the PLL filter. A 0.1-µF capacitor needs be connected between RXCN1 and RXCP1. Similarly a 0.1-µF capacitor needs to be connected between RXCN2 and RXCP2. The recommended packages and dielectric material for these capacitors are 0805 X7R or 0603 X7R. These capacitors should be surface mount packages and be placed as close as possible to the device.

Deserializer

The CDR circuit extracts bits from the serial data stream and clocks these bits into the Deserializer at the bit-clock rate. The Deserializer converts serial data into parallel data. RXD[15] is the most significant bit of the output word and is received first on the serial interface. This RXD[15:0] data is output registered and fed to the programmable LB of the device.

Registering RXD[15:0] Data Before It Enters Programmable LB

Before the RXD[15:0] enters the programmable LB it is required to register these signals in standard datapath cells without any output enables. It is also required to clock these standard datapath cells using the rising edge of the global RXCLK.

Loopback/Timing Modes

High-speed PSI supports various loopback modes as described below.

Facility Loopback (Line Loopback With Retiming)

When the LINELOOP signal is set HIGH, the Facility Loopback mode is activated and the high-speed serial receive data (IN±) is presented to the high-speed transmit output (OUT±) after retiming. In Facility Loopback mode, the high-speed receive data (IN±) is also converted to parallel data and presented to the low-speed receive data output pins (RXD[15:0]). The receive recovered clock is also divided down and presented to the low speed clock output (RXCLK).

Equipment Loopback (Diagnostic Loopback With Retiming)

When the DIAGLOOP signal is set HIGH, transmit data is looped back to the RX PLL, replacing IN±. Data is looped back from the parallel TX inputs to the parallel RX outputs. The data is looped back at the internal serial interface and goes through transmit shifter and the receive CDR. SD is ignored in this mode.

Line Loopback Mode (Non-retimed Data)

When the LOOPA signal is set HIGH, the RX serial data is directly buffered out to the transmit serial data. The data at the serial output is not retimed.

Loop Timing Mode

When the LOOPTIME signal is set HIGH, the TX PLL is bypassed and receive bit-rate clock is used for transmit side shifter.

Reset Modes for the serial transceiver

All logic circuits in the serial transceiver block can be reset using RESET and FIFO_RST signals. When RESET is set LOW, all logic circuits in the serial transceiver except FIFO are internally reset. When FIFO_RST is set LOW, the FIFO logic is reset.

Power-down Mode for serial transceiver

High-speed PSI transceiver block provide a power-down signal PWRDN. When LOW, this signal powers down the entire serial transceiver block to a minimal power dissipation state. RESET and FIFO_RST signals should be asserted LOW along with PWRDN signal to ensure low-power dissipation.

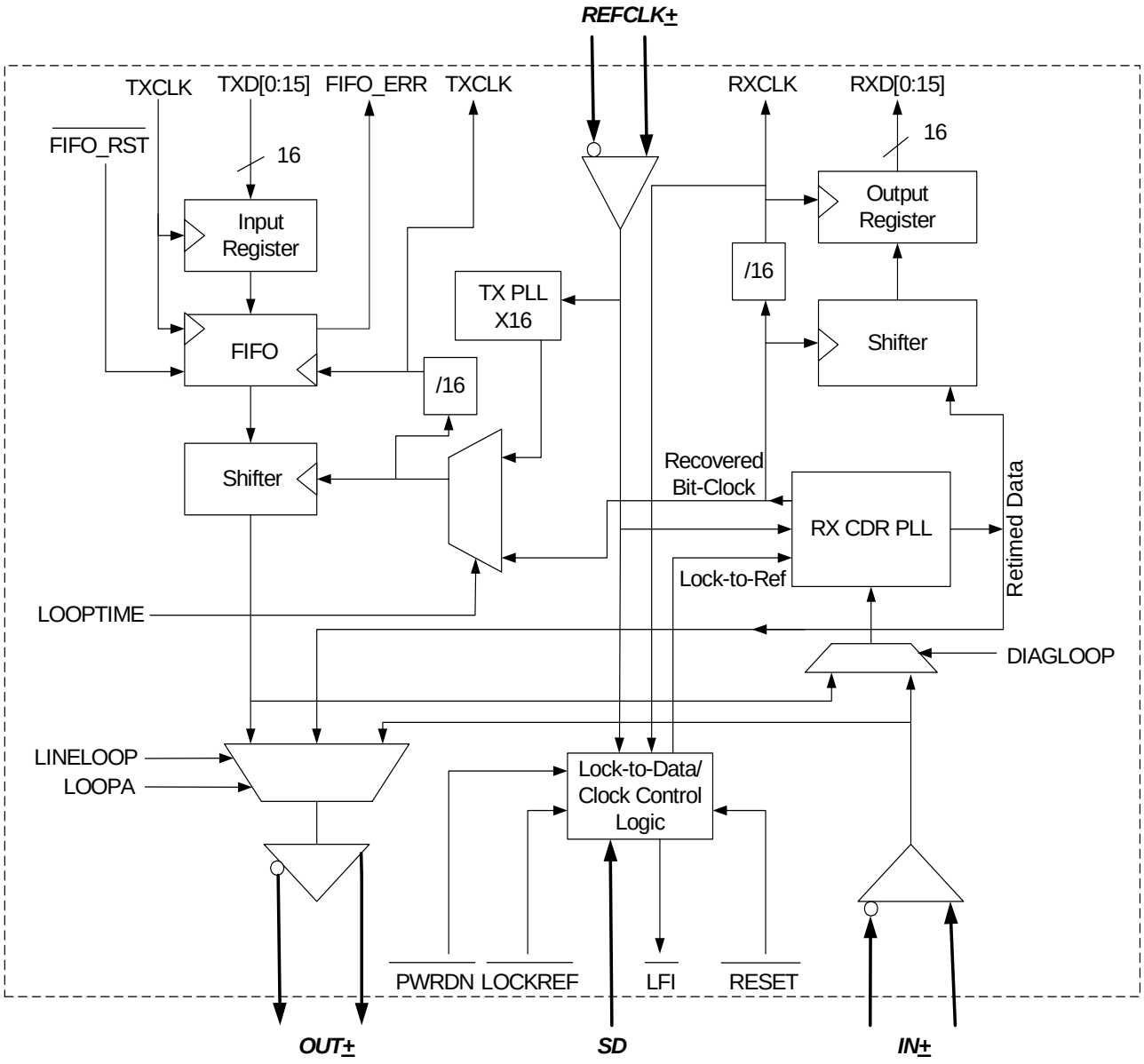


Figure 13. High-speed PSI Transceiver Logic Block Diagram[2]

Note:

2. All signal names outside the dotted box have dedicated pins in the package. Other signals are internal and must be port-mapped to programmable logic using hardware description in Warp software.

IEEE 1149.1-compliant JTAG Operation

The 2.5-Gbps PSI has an IEEE standard 1149.1 JTAG interface for both Boundary Scan and ISR operations.

Four dedicated pins are reserved on each device for use by the Test Access Port (TAP).

The serial transceiver block of this device does not support JTAG since most of the blocks in the serial transceiver block are analog. Hence the serial transceiver portion is not a part of the JTAG test chain.

Boundary Scan

The 2.5-Gbps PSI supports Bypass, Sample/Preload, Extest, Intest, Idcode and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 14*.

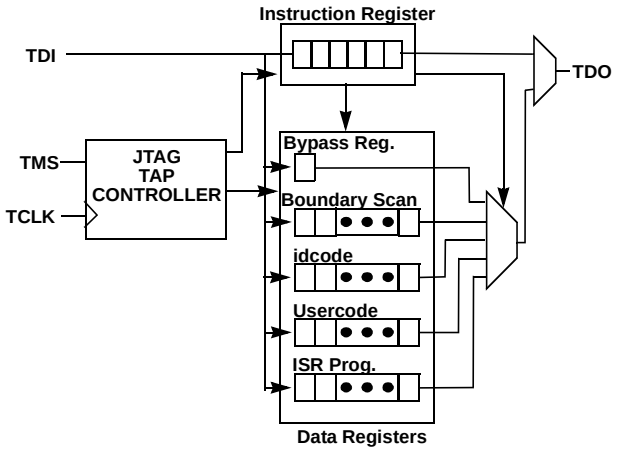


Figure 14. JTAG Interface

In-System Reprogramming™ (ISR™)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The 2.5-Gbps PSI implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Configuration

The CPLD block in the 2.5-Gbps PSI is designed with Self-Boot capability. An embedded on-chip EEPROM is used to store configuration data. For PSI devices, programming is defined as the loading of a user's design into the internal EEPROM. Configuration, on the other hand, is defined as the loading of a user's design into the volatile CPLD block.

Configuration can begin in two ways. It can be initiated by toggling the *Reconfig* pin from LOW to HIGH, or by issuing the appropriate IEEE std 1149.1 JTAG instruction to the PSI device via the JTAG interface. There are two IEEE std 1149.1 JTAG instructions that initiate configuration of the PSI. The *Self Config* instruction causes the PSI to (re)configure with data store in the internal EEPROM. The *Load Config* instruction causes the PSI to (re)configure with data provided by other sources such as a PC, Automatic Test Equipment (ATE), or an embedded micro-controller/processor via the JTAG port.

There are multiple configuration options available for issuing the IEEE std 1149.1 JTAG instructions to the PSI. The first method is to use a PC with the C3 ISR programming cable and software. With this method, the ISR pins of the PSI devices in the system are routed to a connector at the edge of the printed circuit board. The C3 ISR programming cable is then connected between the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on the PSI devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish configuration, reading, verifying, and other ISR functions.

For systems with embedded controllers/processors, a controller/processor may be used to configure the PSI. The PSI ISR software assists in this method by converting the device HEX file into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be configured. The controller/processor then simply directs this ISR stream to the chain of PSI devices to complete the desired reconfiguration or diagnostic operations. Contact your local sales office for information on availability of this option.

Programming

The on-chip EEPROM device of the CPLD block is programmed by issuing the appropriate IEEE std 1149.1 JTAG instruction. This can be done automatically using ISR/STAPL software. The configuration bits are sent from a PC through the JTAG port into the PSI via the C3 ISR programming cable. The data is then passed to the internal EEPROM through the Non-Volatile (NV) port of the CPLD block. For more information on how to program the PSI through ISR/STAPL, please refer to the ISR/STAPL User Guide.

Third-Party Programmers

Cypress support is available on a wide variety of third-party programmers. All major programmers (including BP Micro, System General, Hi-Lo) support the PSI family.

Development Software Support

Warp

Warp is a state-of-the-art design environment for designing with Cypress programmable logic. *Warp* utilizes a subset of IEEE 1076/1164 VHDL and IEEE 1364 as the Hardware Description Language (HDL) for design entry. *Warp* accepts VHDL or Verilog input, synthesizes and optimizes the entered design, and outputs a configuration bitstream for the desired PSI device. For simulation, *Warp* provides a graphical waveform simulator as well as VHDL and Verilog Timing Models.

VHDL and Verilog are open, powerful, non-proprietary Hardware Description Languages (HDLs) that are standards for behavioral design entry and simulation. HDL allows designers to learn a single language that is useful for all facets of the design process.

Third-party Software

Cypress products are supported in a number of third-party design entry and simulation tools. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third party vendors.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Soldering Temperature.....220°C

Ambient Temperature with Power Applied.....–40°C to +85°C

Junction Temperature .....135°C

V_{CC} relative to Ground Potential..... –0.5V to 4.2V

V_{CCIO} relative to Ground Potential..... –0.5V to 4.6V

DC Voltage Applied to Outputs in High-Z State –0.5V to 4.5V

Output Current into LVCMOS Outputs (LOW)..... 30 mA

DC Input voltage..... .....–0.5V to 4.5V

DC Current into Outputs..... .....± 20 mA[3]

Static Discharge Voltage..... > 1100V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

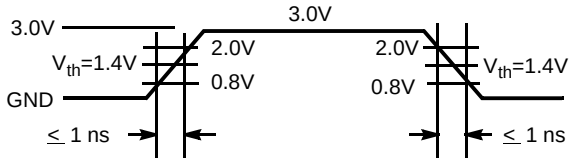
Operating Range

Range	Ambient Temperature	V_{CC}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 10%	1.4V to 1.6V

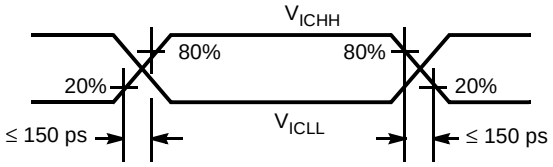
Operating Range

Range	Ambient Temperature	Junction Temperature	Output Condition	V_{CCIO}	V_{CC}	V_{CCJTAG}/ V_{CCCNFG}	V_{CCPLL}	V_{CEP}
Commercial	0°C to +70°C	0°C to +85°C	3.3V	3.3V ± 0.3V	3.3V ± 0.3V	Same as V_{CCIO}	Same as V_{CC}	3.3V ± 0.3V
			2.5V	2.5V ± 0.2V				
			1.8V	1.8V ± 0.15V				
			1.5V	1.5V ± 0.1V				

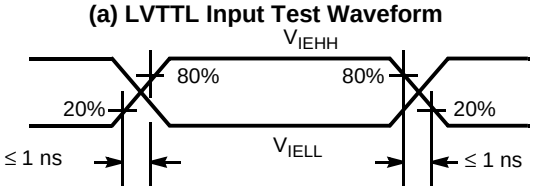
Test Waveforms to High-speed PSI Transceiver Block



(a) LVTTL Input Test Waveform

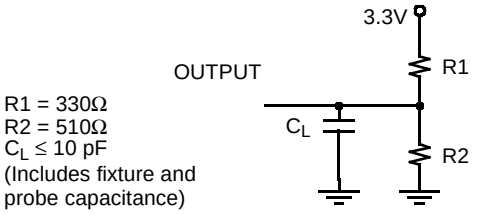


(b) CML Input Test Waveform

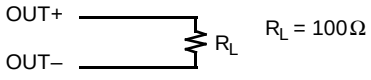


(c) LVPECL Input Test Waveform

AC Test Loads to High-speed Transceiver Block



(a) TTL AC Test Load



(b) CML AC Test Load

Note:

3. DC current into outputs is 36 mA with HSTL III and 48 mA with HSTL IV.

Electrical Characteristics Over the Operating Range

DC Characteristics

Parameter	Description	Test Conditions	V_{CCIO} = 3.3V		V_{CCIO} = 2.5V		V_{CCIO} = 1.8V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{DRINT}	Data Retention V_{CC} Voltage (config data may be lost below this)		1.5		1.5		1.5		V
V_{DRIO}	Data Retention V_{CCIO} Voltage (config data may be lost below this)		1.2		1.2		1.2		V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ 3.6V	–10	10	–10	10	–10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CCIO}	–10	10	–10	10	–10	10	µA
I_{OS}[4]	Output Short Circuit Current	V_{CCIO} = Max., V_{OUT} = 0.5V		–160		–160		–160	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., V_{PIN} = V_{IL}	+40		+30		+25		µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., V_{PIN} = V_{IH}	–40		–30		–25		µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.		+250		+200		+150	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.		–250		–200		–150	µA

Capacitance

Parameter	Description	Test Conditions	Min.	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{in} = V_{CCIO} @ f = 1 MHz 25°C		10	pF
C_{PCI}	PCI compliant I/O Capacitance	V_{in} = V_{CCIO} @ f = 1 MHz 25°C		8	pF
C_{CLK}	Clock Signal Capacitance	V_{in} = V_{CCIO} @ f = 1 MHz 25°C	5	12	pF
C_{INPECL}	PECL Input Capacitance	V_{CC} = 3.3V @ f = 1 MHz 25°C		4	pF
C_{SD1}	SD Pin Input Capacitance	V_{CC} = 3.3V @ f = 1 MHz 25°C		5	pF
C_{INC1}	CML Input Capacitance	V_{CC} = 3.3V @ f = 1 MHz 25°C		4	pF

DC Characteristics (I/O)

Input/Output Standard	V_{REF} (V)		V_{CCIO} (V)	V_{OH} (V)		V_{OL} (V)		V_{IH} (V)		V_{IL} (V)	
				@ I_{OH} =	V_{OH} (Min.)	@ I_{OL} =	V_{OL} (Max.)	Min.	Max.	Min.	Max.
LVTTL –2 mA	N/A		3.3	–2 mA	2.4	2 mA	0.4	2.0 V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –4 mA			3.3	–4 mA	2.4	4 mA	0.4	2.0 V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –6 mA			3.3	–6 mA	2.4	6 mA	0.4	2.0 V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –8 mA			3.3	–8 mA	2.4	8 mA	0.4	2.0 V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –12 mA			3.3	–12 mA	2.4	12 mA	0.4	2.0 V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –16 mA			3.3	–16 mA	2.4	16 mA	0.4	2.0 V	V_{CCIO} + 0.3	–0.3V	0.8V
LVTTL –24 mA			3.3	–24 mA	2.4	24 mA	0.4	2.0 V	V_{CCIO} + 0.3	–0.3V	0.8V
LVCMOS			3.3	–0.1 mA	V_{CCIO} – 0.2V	0.1 mA	0.2	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVCMOS3			3.0	–0.1 mA	V_{CCIO} – 0.2V	0.1 mA	0.2	2.0V	V_{CCIO} + 0.3	–0.3V	0.8V
LVCMOS2			2.5	–0.1 mA	2.1	0.1 mA	0.2	1.7V	V_{CCIO} + 0.3	–0.3V	0.7V
				–1.0 mA	2.0	1.0 mA	0.4				
				–2.0 mA	1.7	2.0 mA	0.7				
LVCMOS18			1.8	– 2 mA	V_{CCIO}–0.45V	2.0 mA	0.45	0.65V_{CCIO}	V_{CCIO}+0.3	–0.3V	0.35V_{CCIO}
3.3V PCI			3.3	–0.5 mA	0.9V_{CCIO}	1.5 mA	0.1V_{CCIO}	0.5V_{CCIO}	V_{CCIO}+0.5	–0.5V	0.3V_{CCIO}

Note:

4. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT}=0.5V has been chosen to avoid test problems caused by tester ground degradation. Tested initially and after any design or process changes that may affect these parameters.

DC Characteristics (I/O)

Input/Output Standard	V_{REF} (V)		V_{CCIO} (V)	V_{OH} (V)		V_{OL} (V)		V_{IH} (V)		V_{IL} (V)	
				@ I_{OH} =	V_{OH} (Min.)	@ I_{OL} =	V_{OL} (Max.)	Min.	Max.	Min.	Max.
GTL+	0.9	1.1	Note 5			36 mA[6]	0.6	V_{REF}+ 0.2			V_{REF}– 0.2
SSTL3 I	1.3	1.7	3.3	–8 mA	V_{CCIO}–1.1V	8 mA	0.7	V_{REF}+ 0.2	V_{CCIO}+0.3	–0.3V	V_{REF}– 0.2
SSTL3 II	1.3	1.7	3.3	–16 mA	V_{CCIO}–0.9V	16 mA	0.5	V_{REF}+ 0.2	V_{CCIO}+0.3	–0.3V	V_{REF}– 0.2
SSTL2 I	1.15	1.35	2.5	–7.6 mA	V_{CCIO}–0.62V	7.6 mA	0.54	V_{REF}+ 0.18	V_{CCIO}+0.3	–0.3V	V_{REF}– 0.18
SSTL2 II	1.15	1.35	2.5	–15.2 mA	V_{CCIO}–0.43V	15.2 mA	0.35	V_{REF}+ 0.18	V_{CCIO}+0.3	–0.3V	V_{REF}– 0.18
HSTL I	0.68	0.9	1.5	–8 mA	V_{CCIO}–0.4V	8 mA	0.4	V_{REF}+ 0.1	V_{CCIO}+0.3	–0.3V	V_{REF}– 0.1
HSTL II	0.68	0.9	1.5	–16 mA	V_{CCIO}–0.4V	16 mA	0.4	V_{REF}+ 0.1	V_{CCIO}+0.3	–0.3V	V_{REF}– 0.1
HSTL III	0.68	0.9	1.5	–8 mA	V_{CCIO}–0.4V	24 mA	0.4	V_{REF}+ 0.1	V_{CCIO}+0.3	–0.3V	V_{REF}– 0.1
HSTL IV	0.68	0.9	1.5	–8 mA	V_{CCIO}–0.4V	48 mA	0.4	V_{REF}+ 0.1	V_{CCIO}+0.3	–0.3V	V_{REF}– 0.1

Parameter	Description	Test Conditions	Min.	Max.	Unit
SD Pin LVTTL Inputs					
V_{IHT}	Input HIGH Voltage	Low = 2.0V, High = V_{CC} + 0.5V	2.0	V_{CC} – 0.3	V
V_{ILT}	Input LOW Voltage	Low = –3.0V, High = 0.8V	–0.3	0.8	V
I_{IHT}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		50	µA
I_{ILT}	Input LOW Current	V_{CC} = Max., V_{IN} = 0V		–50	µA
REFCLK LVPECL-compatible Inputs					
V_{INSGLE}	Input Single-ended Swing		200	600	mV
V_{DIFFE}	Input Differential Voltage		400	1200	mV
V_{IEHH}	Highest Input HIGH Voltage		V_{CC} – 1.2	V_{CC} – 0.3	V
V_{IELL}	Lowest Input LOW Voltage		V_{CC} – 2.0	V_{CC} – 1.45	V
I_{IEH}	Input HIGH Current	V_{IN} = V_{IEHH} Max.		750	µA
I_{IEL}	Input LOW Current	V_{IN} = V_{IELL} Min.	–200		µA
Transmitter Differential CML-compatible Outputs					
V_{OHC}	Output HIGH Voltage (V_{CC} Referenced)	100Ω differential load	V_{CC} – 0.5	V_{CC} – 0.15	V
V_{OLC}	Output LOW Voltage (V_{CC} Referenced)	100Ω differential load	V_{CC} – 1.2	V_{CC} – 0.7	V
I_{ACCM}	AC Common Mode Current			5	µA
V_{ACCM}	AC Common Mode Voltage			25	mV
Z_D	Differential Output Impedance		75	125	Ω
Z_{SE}	Single Ended Output Impedance		30	75	Ω
Z_{MSE}	Single Ended Output Impedance Matching Within a Single Lane			10	%
I_{DSHORT}	Short Circuit Current		–100	100	mA
V_{DIFFOC}	Output Differential Swing	100Ω differential load	1000	1600	mV
V_{SGLOC}	Output Single Ended Swing	100Ω differential load	500	800	mV

Notes:

5. See “Power-up Sequence Requirements” for V_{CCIO} requirement.
6. 25Ω resistor terminated to termination voltage of 1.5V.

Parameter	Description	Test Conditions	Min.	Max.	Unit
Receiver Differential CML Compatible Inputs					
V_{ICHH}	Highest Input HIGH Voltage			V_{CC}	V
V_{ICLL}	Lowest Input LOW Voltage		1.2		V
Z_{VTT}	V_{TT} Impedance			30	Ω
L_{DR}	Differential Return Loss		10		dB
L_{CMR}	Common Mode Return Loss		6		dB
V_{RSD}	Voltage Threshold		20		mV
V_{RMAX}	Maximum Input Voltage (p-p)			1.6	V
V_{DIFFC}	Input Differential Voltage		50	2000	mV
V_{INSGLC}	Input Single-ended Swing		25	1000	mV

Configuration Parameters

Parameter	Description	Min.	Unit
$t_{RECONFIG}$	*Reconfig* pin LOW time before it goes HIGH	200	ns

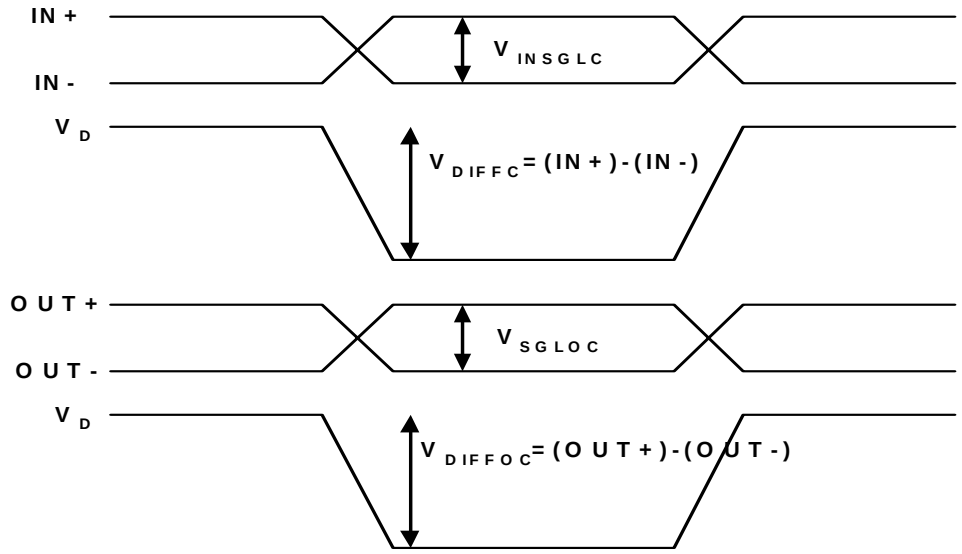


Figure 15. Differential Parameters Waveforms

Power-up Sequence Requirements

- Upon power-up, all the outputs remain three-stated until all the V_{CC} pins have powered up to the nominal voltage and the part has completed configuration.
- The part will not start configuration until V_{CC}, V_{DDQ}, V_{CCIO}, V_{CCJTAG}, V_{CCCNFG}, V_{CCPLL} and VCEP have reached nominal voltage.
- V_{CC} pins can be powered up in any order. This includes V_{CC}, V_{DDQ}, V_{CCIO}, V_{CCJTAG}, V_{CCCNFG}, V_{CCPLL} and VCEP.
- All V_{CCIO}s on a bank should be tied to the same potential and powered up together.
- All V_{CCIO}s (even the unused banks) need to be powered up to at least 1.5V before configuration has completed.
- Maximum ramp time for all V_{CC}s should be 0V to nominal voltage in 100 ms.

Switching Characteristics

Timing Parameter Values [7]

Parameter	Description	Min.	Max.	Unit
Combinatorial Mode Parameters				
t_{PD}	Delay from any pin input, through any cluster on the channel associated with that pin input, to any pin output on the horizontal or vertical channel associated with that cluster		7.5	ns
t_{EA}	Global control to output enable		5.0	ns
t_{ER}	Global control to output disable		5.0	ns
t_{PRR}	Asynchronous macrocell RESET or PRESET recovery time from any pin input on the horizontal or vertical channel associated with the cluster the macrocell is in	6.0		ns
t_{PRO}	Asynchronous macrocell RESET or PRESET from any pin input on the horizontal or vertical channel associated with the cluster that the macrocell is in to any pin output on those same channels	10		ns
t_{PRW}	Asynchronous macrocell RESET or PRESET minimum pulse width, from any pin input to a macrocell in the farthest cluster on the horizontal or vertical channel the pin is associated with	3.6		ns
Synchronous Clocking Parameters				
t_{MCS}	Set-up time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock	3.0		ns
t_{MCH}	Hold time of any input pin to a macrocell in any cluster on the channel associated with that input pin, relative to a global clock	0.0		ns
t_{MCCO}	Global clock to output of any macrocell to any output pin on the horizontal or vertical channel associated with the cluster that macrocell is in		6.0	ns
t_{IOS}	Set-up time of any input pin to the I/O cell register associated with that pin, relative to a global clock	1.0		ns
t_{IOH}	Hold time of any input pin to the I/O cell register associated with that pin, relative to a global clock	1.0		ns
t_{IOCO}	Clock to output of an I/O cell register to the output pin associated with that register		4.0	ns
t_{SCS}	Macrocell clock to macrocell clock through array logic within the same cluster	3.5		ns
t_{SCS2}	Macrocell clock to macrocell clock through array logic in different clusters on the same channel	4.5		ns
t_{ICS}	I/O register clock to any macrocell clock in a cluster on the channel the I/O register is associated with	5.0		ns
t_{OCS}	Macrocell clock to any I/O register clock on the horizontal or vertical channel associated with the cluster that the macrocell is in	5.0		ns
t_{CHZ}	Clock to output disable (high-impedance)		3.5	ns
t_{CLZ}	Clock to output enable (low-impedance)	1.5		ns
f_{MAX}	Maximum frequency with internal feedback—within the same cluster		286	MHz
f_{MAX2}	Maximum frequency with internal feedback—within different clusters at the opposite ends of a horizontal or vertical channel		222	MHz
Product Term Clocking Parameters				
t_{MCSPT}	Set-up time for macrocell used as input register, from input to product term clock	3.0		ns
t_{MCHPT}	Hold time of macrocell used as an input register	1.0		ns
t_{MCCOPT}	Product term clock to output delay from input pin		8.0	ns
t_{SCS2PT}	Register to register delay through array logic in different clusters on the same channel using a product term clock	6.5		ns
Channel Interconnect Parameters				
t_{CHSW}	Adder for a signal to switch from a horizontal to vertical channel and vice-versa		1.0	ns
t_{CL2CL}	Cluster to Cluster delay adder (through channels and channel PIM)		2.0	ns

Note:

7. Add t_{CHSW} to signals making a horizontal to vertical channel switch or vice versa.

Switching Characteristics

Timing Parameter Values [7] (continued)

Parameter	Description	Min.	Max.	Unit
Miscellaneous Parameters				
t_{CPLD}	Delay from the input of a cluster PIM, through a macrocell in the cluster, back to a cluster PIM input. This parameter can be added to the t_{PD} and t_{SCS} parameters for each extra pass through the AND/OR array required by a given signal path		3.0	ns
t_{MCCD}	Adder for carry chain logic per macrocell		0.25	ns
PLL Parameters				
t_{MCCJ}	Maximum cycle to cycle jitter time	–150	150	ps
t_{DWSA}	PLL delay with skew adjustment	–1.35	–0.85	ns
t_{DWOSA}	PLL delay without any skew adjustment	–150	150	ps
t_{LOCK}	Lock time for the PLL		250	µs
f_{PLLO}	Output frequency of the PLL	6.2	266	MHz
f_{PLLI}	Input frequency of the PLL	12.5	133	MHz

Cluster Memory Timing Parameter Values

Parameter	Description	200		Unit
		Min.	Max.	
Asynchronous Mode Parameters				
t_{CLMAA}	Cluster memory access time. Delay from address change to read data out		11	ns
t_{CLMPWE}	Write enable pulse width	6.0		ns
t_{CLMSA}	Address set-up to the beginning of write enable	2.0		ns
t_{CLMHA}	Address hold after the end of write enable with both signals from the same I/O block	1.0		ns
t_{CLMSD}	Data set-up to the end of write enable	6.0		ns
t_{CLMHD}	Data hold after the end of write enable	0.5		ns
Synchronous Mode Parameters				
$t_{CLMCYC1}$	Clock cycle time for flow-through read and write operations (from macrocell register through cluster memory back to a macrocell register in the same cluster)	10		ns
$t_{CLMCYC2}$	Clock cycle time for pipelined read and write operations (from cluster memory input register through the memory to cluster memory output register)	5.0		ns
t_{CLMS}	Address, data, and WE set-up time of pin inputs, relative to a global clock	3.0		ns
t_{CLMH}	Address, data, and WE hold time of pin inputs, relative to a global clock	0.0		ns
t_{CLMDV1}	Global clock to data valid on output pins for flow through data		11	ns
t_{CLMDV2}	Global clock to data valid on output pins for pipelined data		7.5	ns
$t_{CLMMACS1}$	Cluster memory input clock to macrocell clock in the same cluster	8.0		ns
$t_{CLMMACS2}$	Cluster memory output clock to macrocell clock in the same cluster	5.0		ns
$t_{MACCLMS1}$	Macrocell clock to cluster memory input clock in the same cluster	4.0		ns
$t_{MACCLMS2}$	Macrocell clock to cluster memory output clock in the same cluster	6.5		ns
Internal Parameters				
$t_{CLMCLAA}$	Asynchronous cluster memory access time from input of cluster to output of cluster	6.0		ns

Channel Memory Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
Dual-Port Asynchronous Mode Parameters				
t_{CHMAA}	Channel memory access time. Delay from address change to read data out		11	ns
t_{CHMPWE}	Write enable pulse width	6.0		ns
t_{CHMSA}	Address set-up to the beginning of write enable	2.0		ns

Channel Memory Timing Parameter Values (continued)

t_{CHMHA}	Address hold after the end of write enable with both signals from the same I/O block	1.0		ns
t_{CHMSD}	Data set-up to the end of write enable	6.0		ns
t_{CHMHD}	Data hold after the end of write enable	0.5		ns
t_{CHMBA}	Channel memory asynchronous dual port address match (busy access time)		9.0	ns
Dual-Port Synchronous Mode Parameters				
$t_{CHMCYC1}$	Clock cycle time for flow through read and write operations (from macrocell register through channel memory back to a macrocell register in the same cluster)	10		ns
$t_{CHMCYC2}$	Clock cycle time for pipelined read and write operations (from channel memory input register through the memory to channel memory output register)	5.3		ns
t_{CHMS}	Address, data, and WE set-up time of pin inputs, relative to a global clock	3.3		ns
t_{CHMH}	Address, data, and WE hold time of pin inputs, relative to a global clock	0.0		ns
t_{CHMDV1}	Global clock to data valid on output pins for flow through data		11	ns
t_{CHMDV2}	Global clock to data valid on output pins for pipelined data		7.5	ns
t_{CHMBDV}	Channel memory synchronous dual-port address match (busy, clock to data valid)		9.0	ns
$t_{CHMMACS1}$	Channel memory input clock to macrocell clock in the same cluster	9.0		ns
$t_{CHMMACS2}$	Channel memory output clock to macrocell clock in the same cluster	5.0		ns
$t_{MACCHMS1}$	Macrocell clock to channel memory input clock in the same cluster	5.0		ns
$t_{MACCHMS2}$	Macrocell clock to channel memory output clock in the same cluster	7.3		ns
Synchronous FIFO Data Parameters				
t_{CHMCLK}	Read and write minimum clock cycle time	5.0		ns
t_{CHMFS}	Data, read enable, and write enable set-up time relative to pin inputs	4.0		ns
t_{CHMFH}	Data, read enable, and write enable hold time relative to pin inputs	0.0		ns
$t_{CHMFRDV}$	Data access time to output pins from rising edge of read clock (read clock to data valid)		7.0	
$t_{CHMMACS}$	Channel memory FIFO read clock to macrocell clock for read data	5.0		ns
$t_{MACCHMS}$	Macrocell clock to channel memory FIFO write clock for write data	5.0		ns
Synchronous FIFO Flag Parameters				
t_{CHMFO}	Read or write clock to respective flag output at output pins		11	ns
$t_{CHMMACF}$	Read or write clock to macrocell clock with FIFO flag	9		ns
t_{CHMFRS}	Master Reset Pulse Width	5.0		ns
$t_{CHMFRSR}$	Master Reset Recovery Time		4.0	ns
$t_{CHMFRSF}$	Master Reset to Flag and Data Output Time		10.0	ns
$t_{CHMSKEW1}$	Read/Write Clock Skew Time for Full Flag		2.0	ns
$t_{CHMSKEW2}$	Read/Write Clock Skew Time for Empty Flag		2.0	ns
$t_{CHMSKEW3}$	Read/Write Clock Skew Time for Boundary Flags		5.0	ns
Internal Parameters				
$t_{CHMCHAA}$	Asynchronous channel memory access time from input of channel memory to output of channel memory	7.0		ns

High-speed PSI Transceiver Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
Transceiver Interfacing Timing Parameters				
t_{TS}	**TXCLK** Frequency (must be frequency coherent to REFCLK)	154.5	156.5	MHz
t_{TXCLK}	**TXCLK** Period	6.38	6.47	ns
t_{RS}	**RXCLK** Frequency	154.5	156.5	MHz
t_{RXCLK}	**RXCLK** Period	6.38	6.47	ns

High-speed PSI Transceiver Timing Parameter Values

Parameter	Description	Min.	Max.	Unit
REFCLK Timing Parameters				
t_{REF}	REFCLK Input Frequency	154.5	156.5	MHz
t_{REFP}	REFCLK Period	6.38	6.47	ns
t_{REFD}	REFCLK Duty Cycle	35	65	%
t_{REFT}	REFCLK Frequency Tolerance (relative to received serial data)[8]	–100	+100	ppm
t_{REFR}	REFCLK Rise Time	0.3	1.5	ns
t_{REFF}	REFCLK Fall Time	0.3	1.5	ns
t_{REFJ}	REFCLK Jitter	See *Figure 16* for phase noise requirements		
CML Serial Outputs				
t_{DRF}	Driver Rise/Fall Time (20–80% rise, 80–20% fall, 100Ω balanced load)	100		ps
t_{UID}[9]	Unit Interval	400	400	ps
CML Serial Outputs				
t_{RISE}	CML Output Rise Time (20–80%, 100Ω balanced load)	60	170	ps
t_{FALL}	CML Output Fall Time (80–20%, 100Ω balanced load)	60	170	ps

Jitter Specifications for CYP25G01K100 (Non-SONET)

t_{EYE}	Eye opening at CML serial inputs	140		ps
t_{JDR}	Deterministic Jitter allowed at CML serial inputs		0.41	UI
t_{JTR}	Total Jitter allowed at CML serial inputs		0.65	UI
t_{JD}	Deterministic Jitter at CML serial outputs		0.17	UI
t_{JT}	Total Jitter at CML serial outputs		0.35	UI

Jitter Specifications for CYS25G01K100 (SONET)

Parameter	Description	Min.	Typical[11]	Max.[11]	Unit
$t_{TJ\text{-}TXPLL}$	Total Output Jitter for TX PLL (p-p)[10]		0.03	0.04	UI
	Total Output Jitter for TX PLL (rms)[10]		0.007	0.008	UI
$t_{TJ\text{-}RXPLL}$	Total Output Jitter for RX CDR PLL (p-p)[10]		0.035	0.05	UI
	Total Output Jitter for RX CDR PLL (rms)[10]		0.008	0.01	UI

Note:

8. ± 20 ppm is required to meet SONET output frequency specification.
9. Measured with serial bit rate of 2.5 Gbps.
10. The RMS and P-to-P jitter values are measured using a 12 KHz to 20 MHz SONET filter.
11. Typical at room temperature, Max. at 0^{o} deg C.

Phase Noise Limits for CYS25G01K100(SONET) REFCLK Source

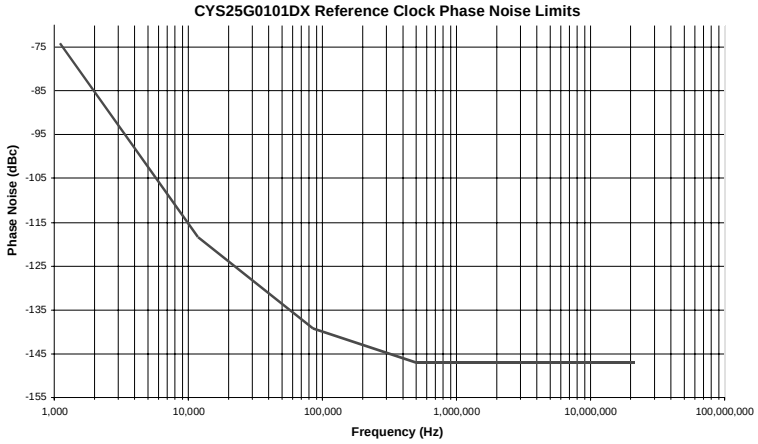


Figure 16. Phase Noise Limits for REFCLK Inputs of CYS25G01K100

Jitter Transfer for CYS25G01K100 (SONET) RXPLL

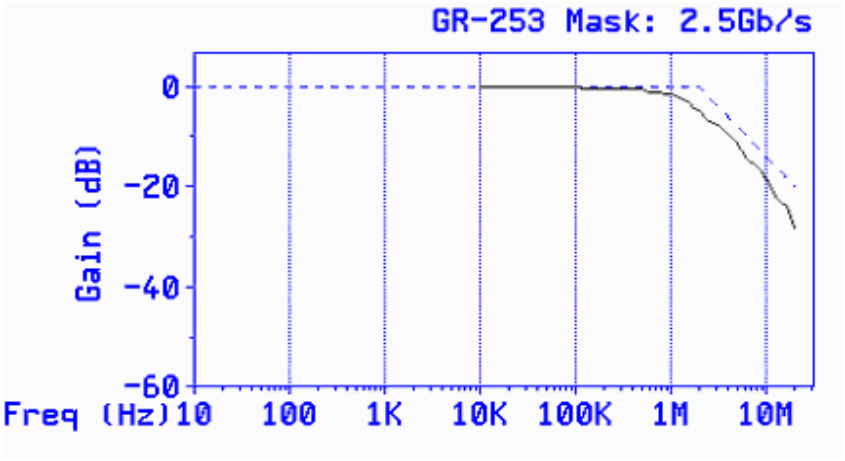


Figure 17. Jitter Transfer for CYS25G01K100

Jitter Tolerance for CYS25G01K100 (SONET)

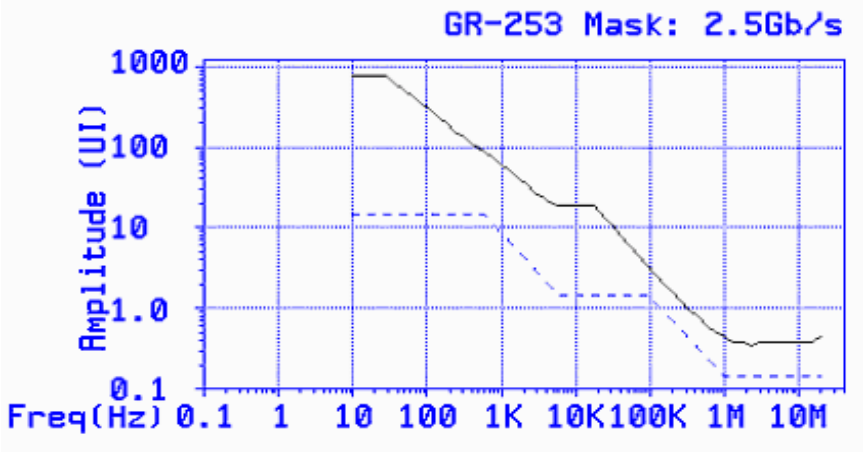


Figure 18. Jitter Tolerance for CYS25G01K100

Input and Output Standard Timing Delay Adjustments

All the timing specifications in this data sheet are specified based on 3.3V PCI compliant inputs and outputs (fast slew rates[12]). Apply following adjustments if the inputs and outputs are configured to operate at other standards.

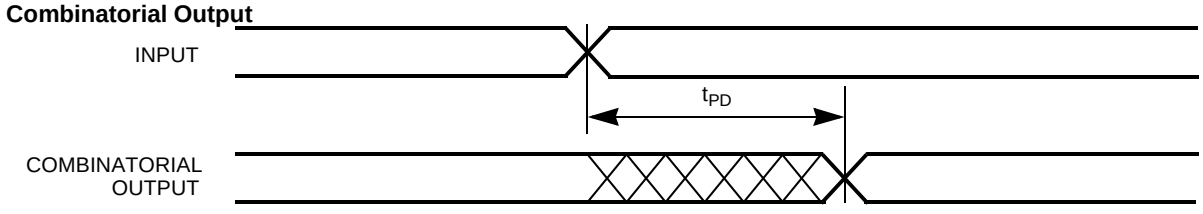
Input/Output Standard	Output Delay Adjustments (ns)			Input Delay Adjustments(ns)		
	t_{IOD}	t_{EA}	t_{ER}	t_{IOIN}	t_{CKIN}	$t_{IOREGPIN}$
LVTTL – 2 mA	2.75	0	0	0	0	0
LVTTL – 4 mA	1.8	0	0	0	0	0
LVTTL – 6 mA	1.8	0	0	0	0	0
LVTTL – 8 mA	1.2	0	0	0	0	0
LVTTL – 12 mA	0.6	0	0	0	0	0
LVTTL – 16 mA	0.16	0	0	0	0	0
LVTTL – 24 mA	0	0	0	0	0	0
LVCMOS	0	0	0	0	0	0
LVCMOS3	0.14	0.05	0	0.1	0.1	0.2
LVCMOS2	0.41	0.1	0	0.2	0.2	0.4
LVCMOS18	1.6	0.7	0.1	0.5	0.4	0.3
3.3V PCI	–0.14	0	0	0	0	0
GTL+	0.02[13]	0.6[13]	0.9[13]	0.5	0.4	0.2
SSTL3 I	–0.15	0.3	0.1	0.5	0.3	0.3
SSTL3 II	–0.4	0.2	0	0.5	0.3	0.3
SSTL2 I	–0.02	0.4	0	0.9	0.5	0.6
SSTL2 II	–0.22	0.2	0	0.9	0.5	0.6
HSTL I	0.94	0.9	0.5	0.5	0.5	0.3
HSTL II	0.79	0.8	0.5	0.5	0.5	0.3
HSTL III	0.77	0.5	0.1	0.5	0.5	0.3
HSTL IV	0.44	0.6	0	0.5	0.5	0.3

Notes:
12. For “slow slew rate” output delay adjustments, refer to *Warp* software’s static timing analyzer results.
13. These delays are based on falling edge output. The rising edge delay depends on the size of pull up resistor and termination voltage.

Switching Waveforms

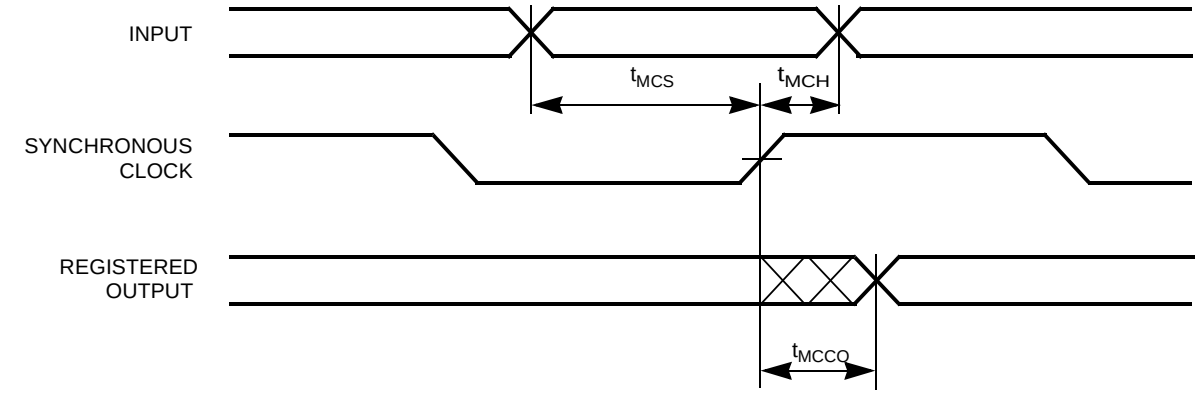
General Switching Waveforms

Combinatorial Output

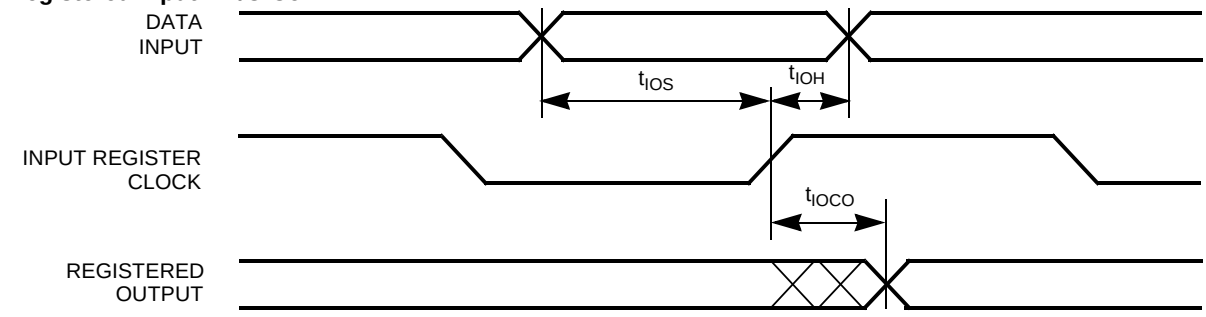


Switching Waveforms (continued)

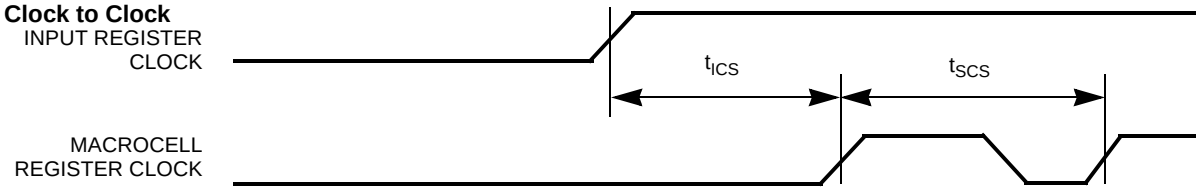
Registered Output with Synchronous Clocking (Macrocell)



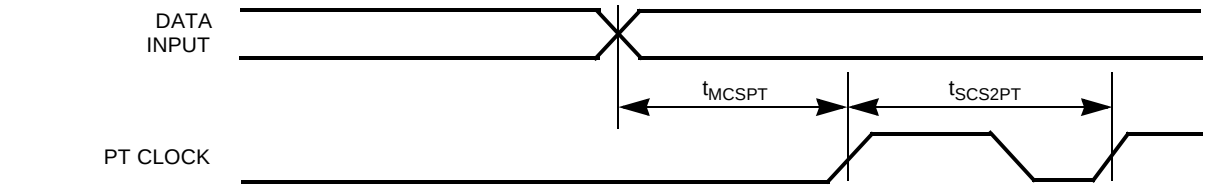
Registered Input in I/O Cell



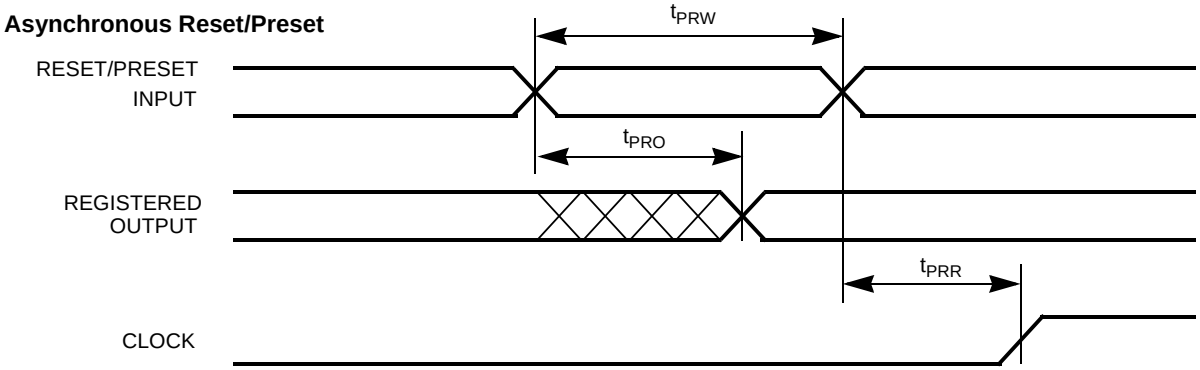
Clock to Clock



PT Clock to PT Clock

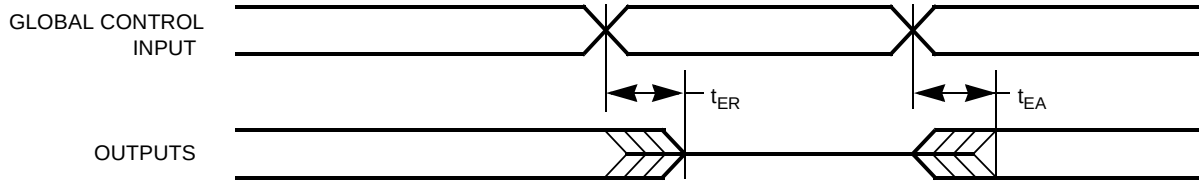


Asynchronous Reset/Preset

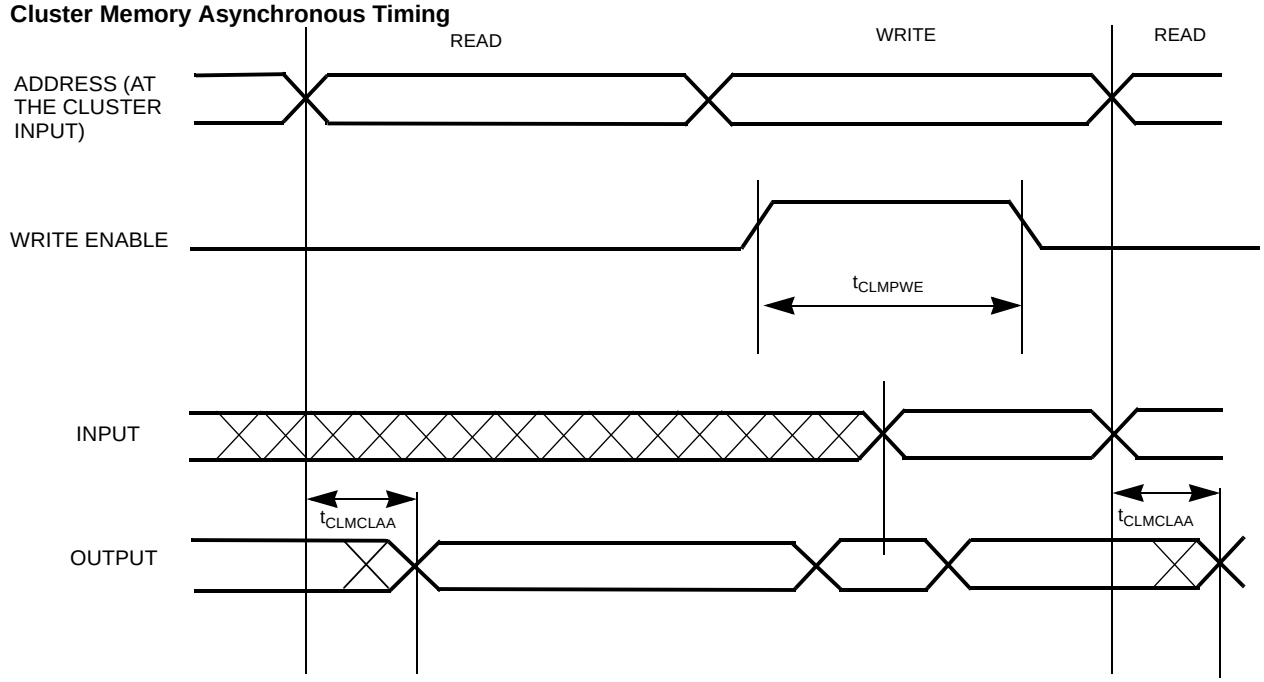


Switching Waveforms (continued)

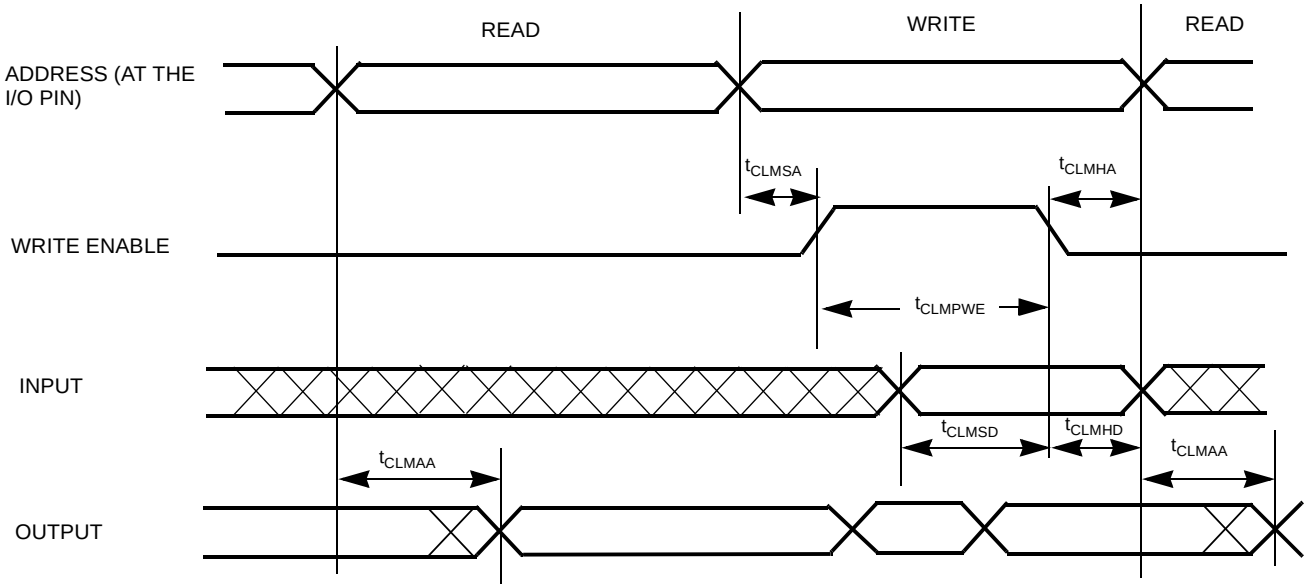
Output Enable/Disable



Cluster Memory Asynchronous Timing

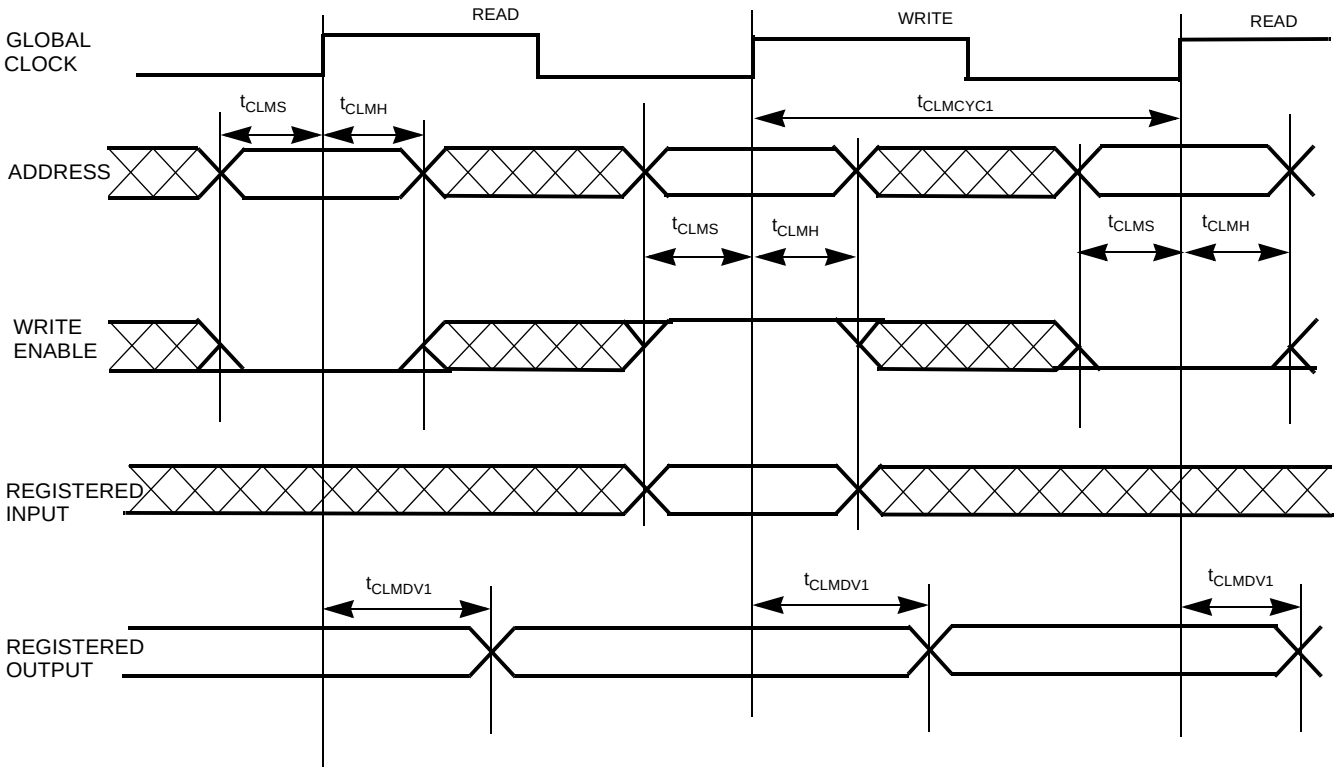


Cluster Memory Asynchronous Timing 2

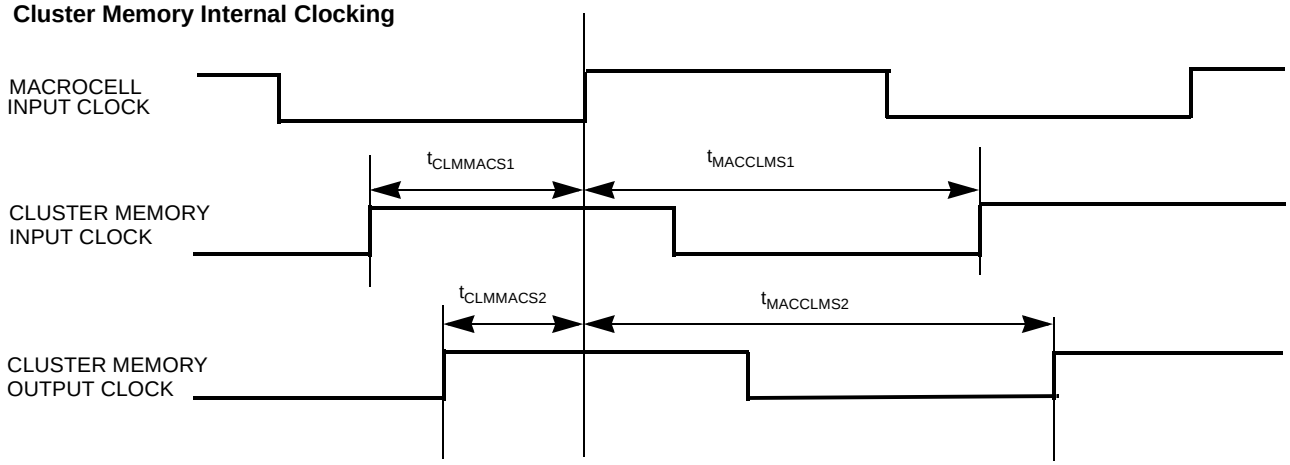


Switching Waveforms (continued)

Cluster Memory Synchronous Timing

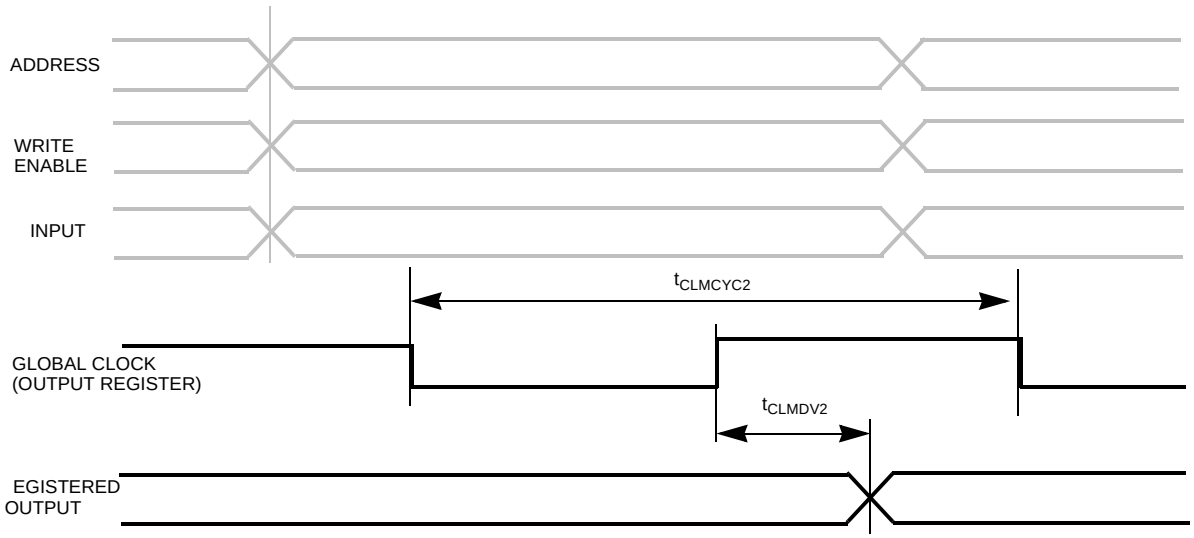


Cluster Memory Internal Clocking

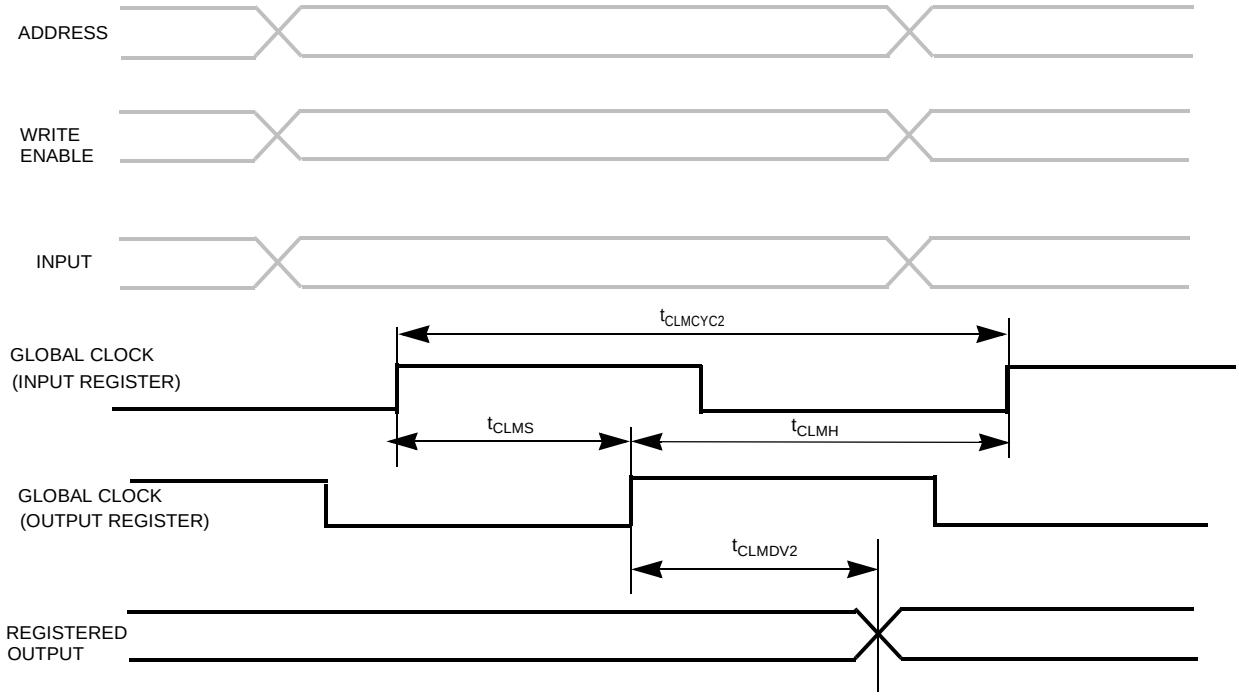


Switching Waveforms (continued)

Cluster Memory Output Register Timing (Asynchronous Inputs)

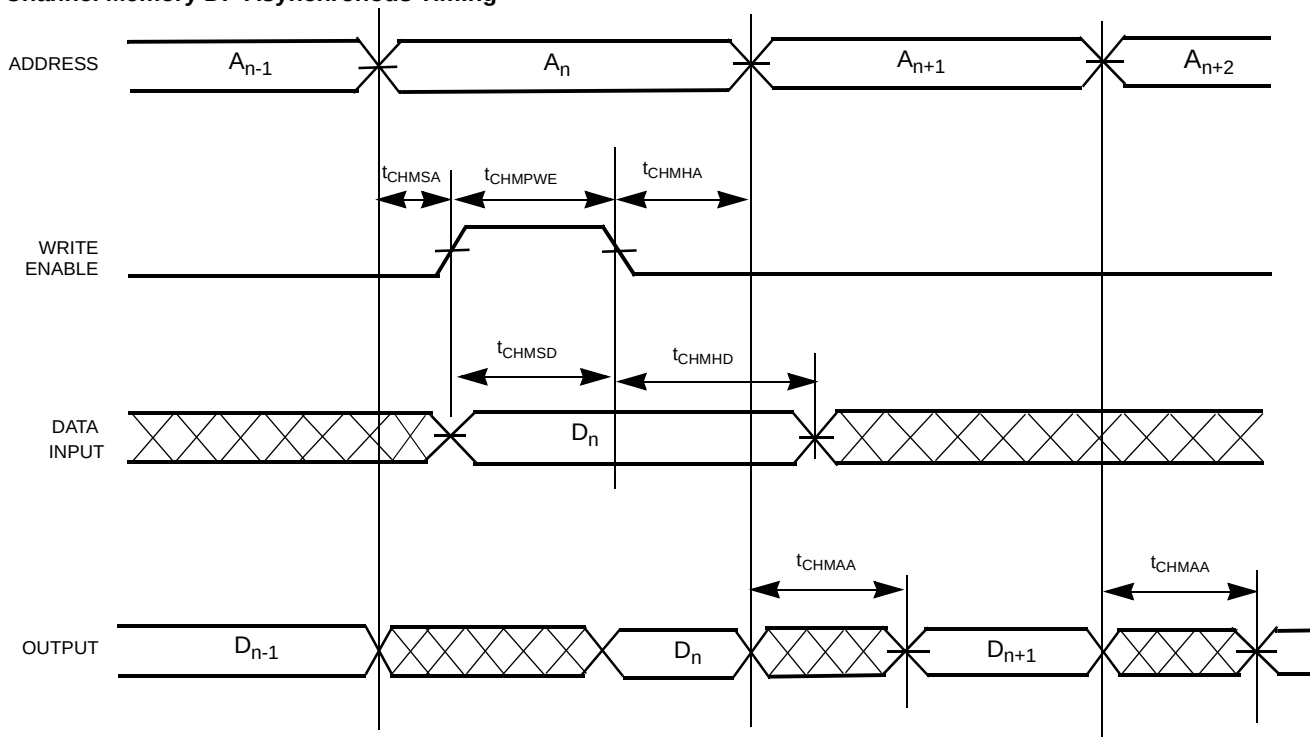


Cluster Memory Output Register Timing (Synchronous Inputs)

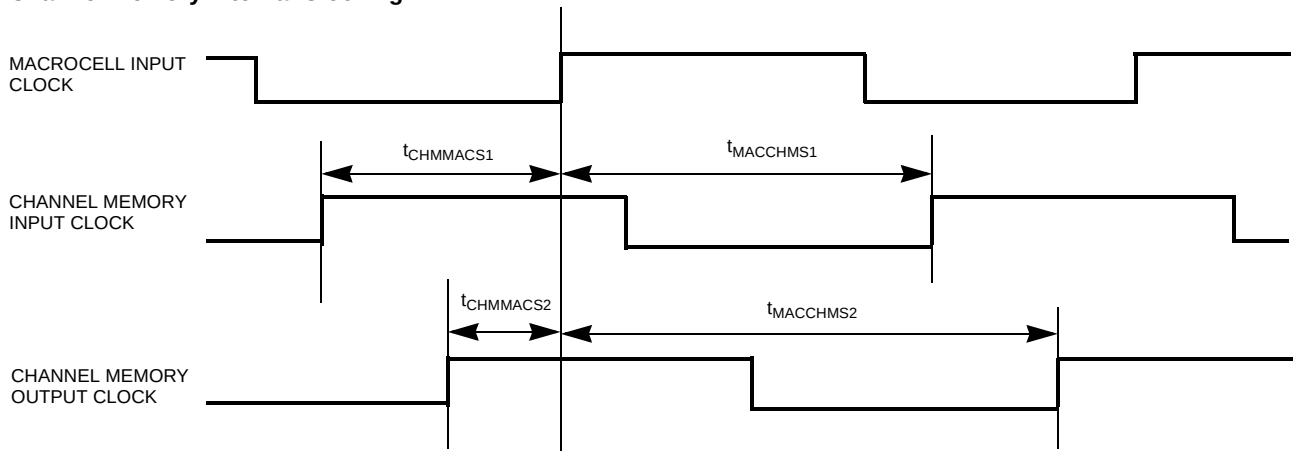


Switching Waveforms (continued)

Channel Memory DP Asynchronous Timing

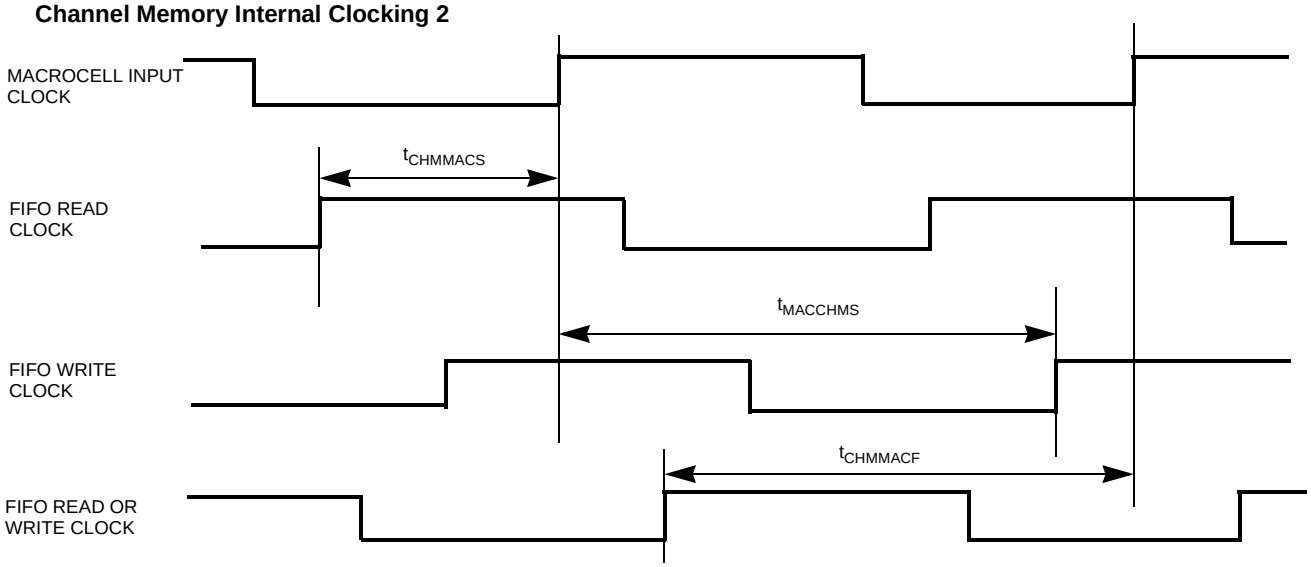


Channel Memory Internal Clocking

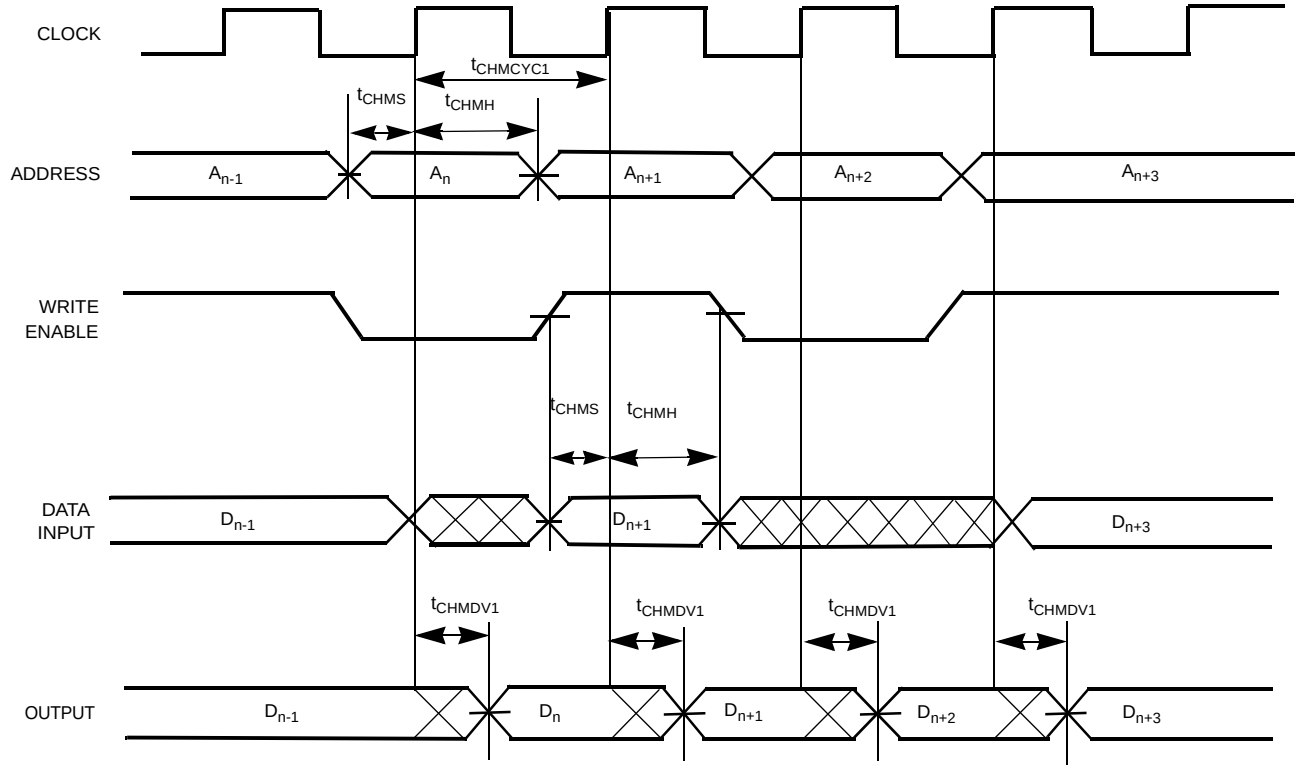


Switching Waveforms (continued)

Channel Memory Internal Clocking 2

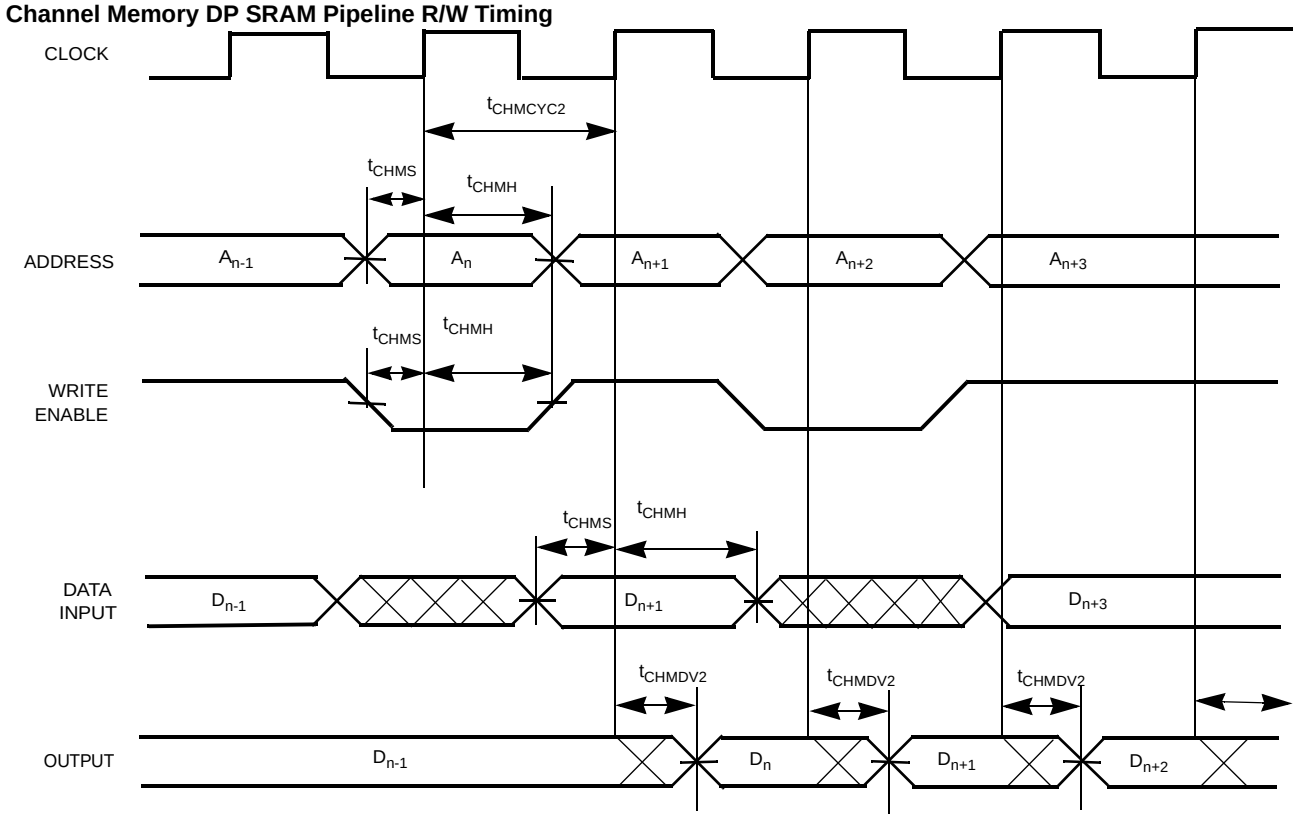


Channel Memory DP SRAM Flow Through R/W Timing

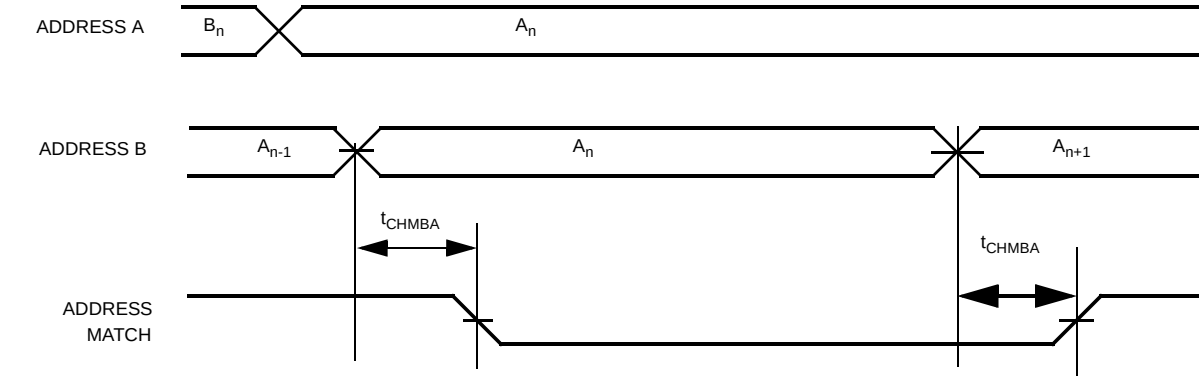


Switching Waveforms (continued)

Channel Memory DP SRAM Pipeline R/W Timing

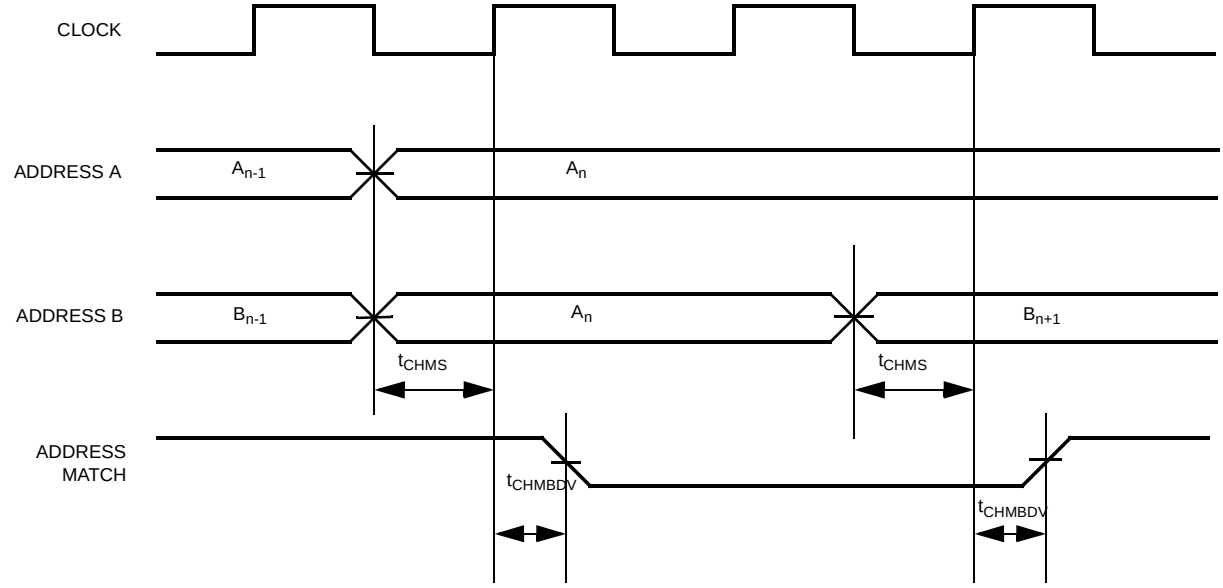


Dual-Port Asynchronous Address Match Busy Signal

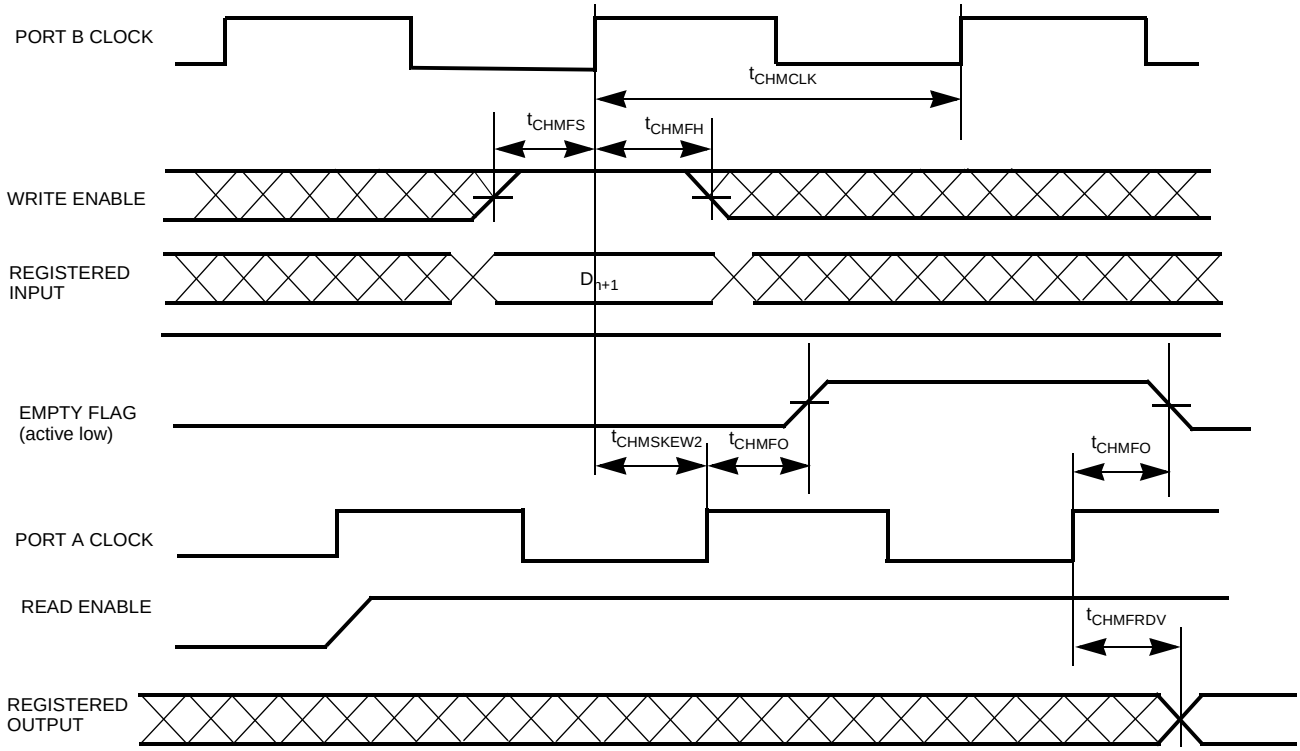


Switching Waveforms (continued)

Dual-Port Synchronous Address Match Busy Signal

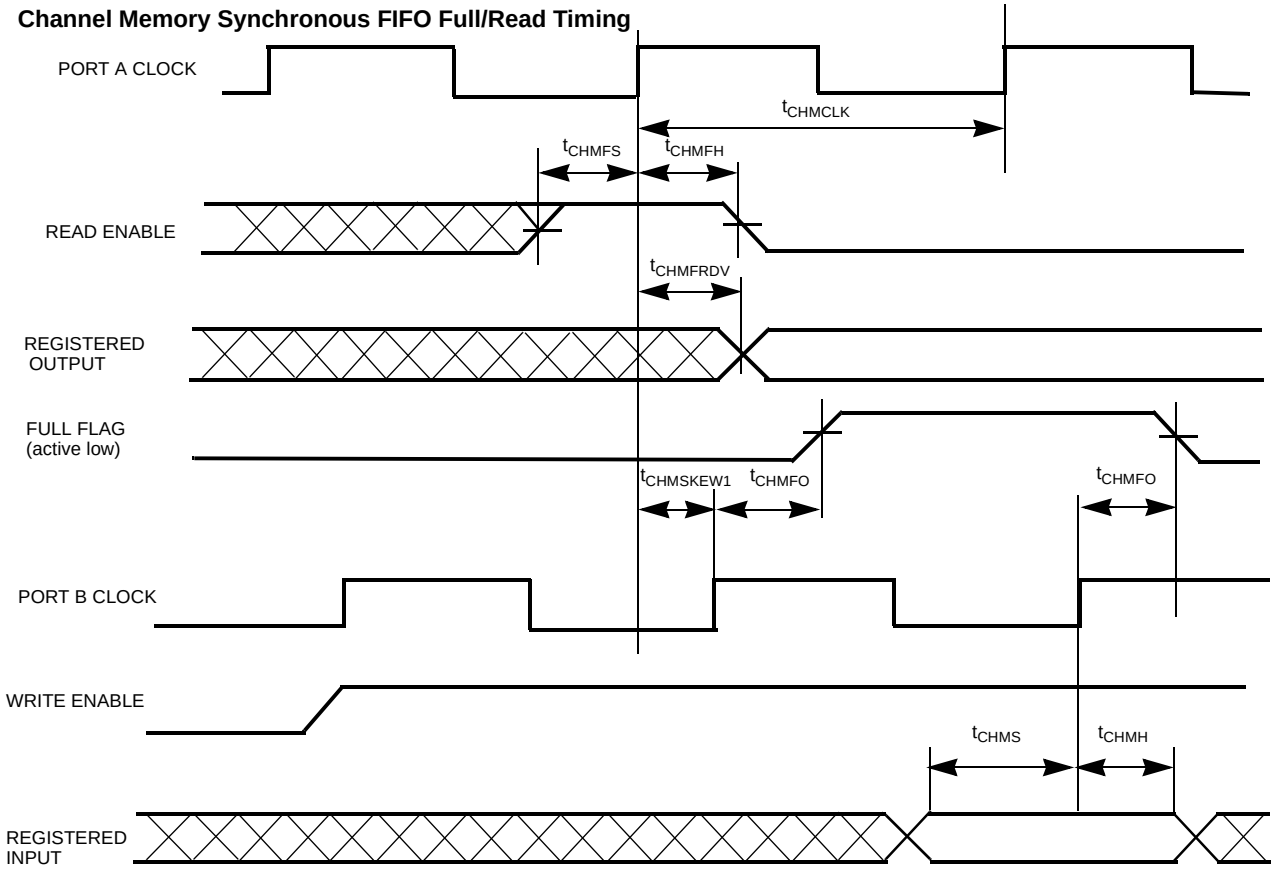


Channel Memory Synchronous FIFO Empty/Write Timing

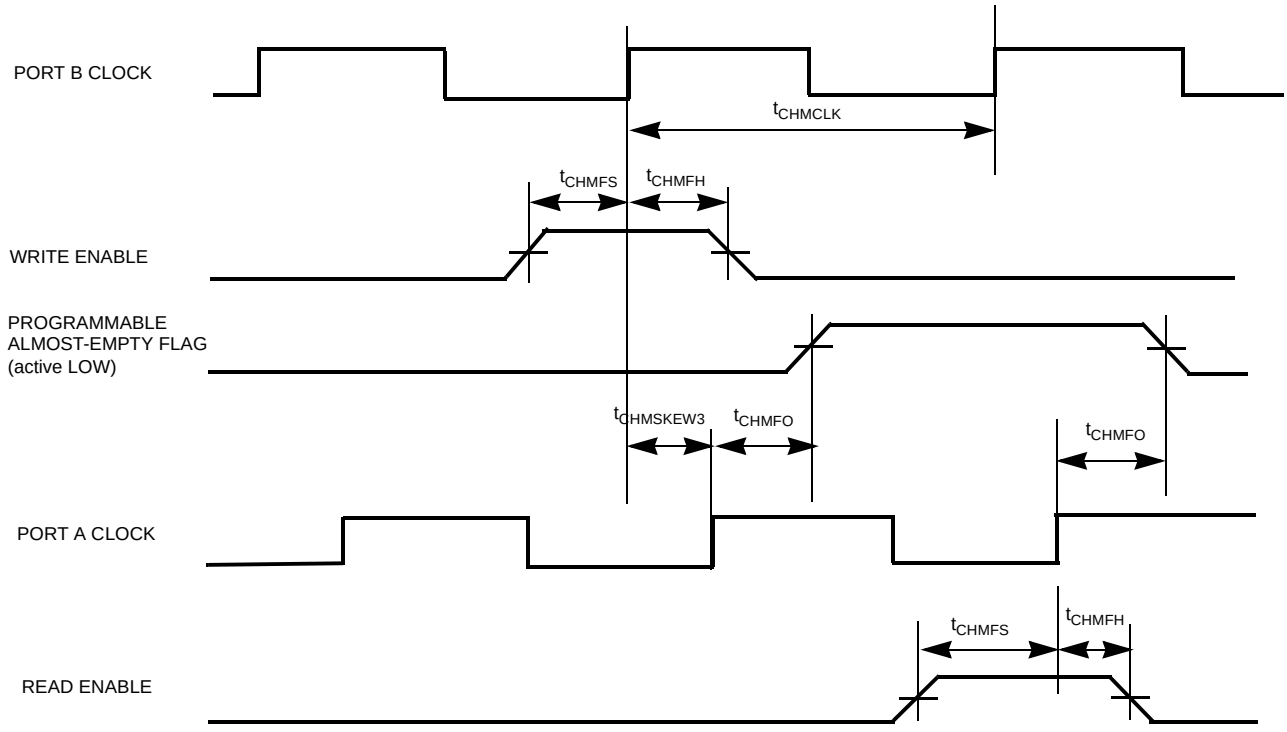


Switching Waveforms (continued)

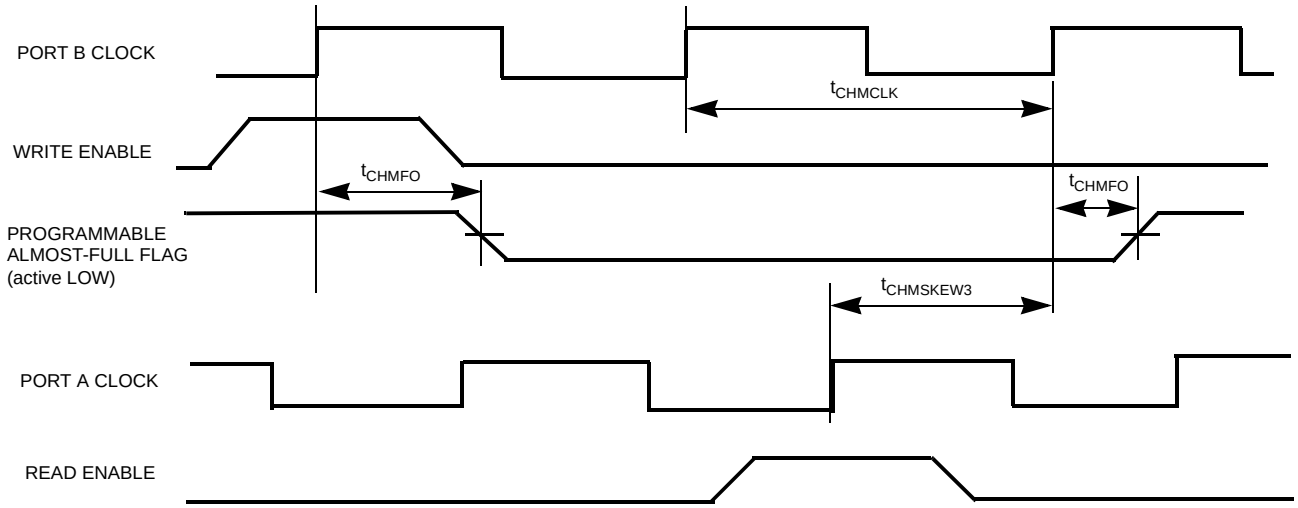
Channel Memory Synchronous FIFO Full/Read Timing



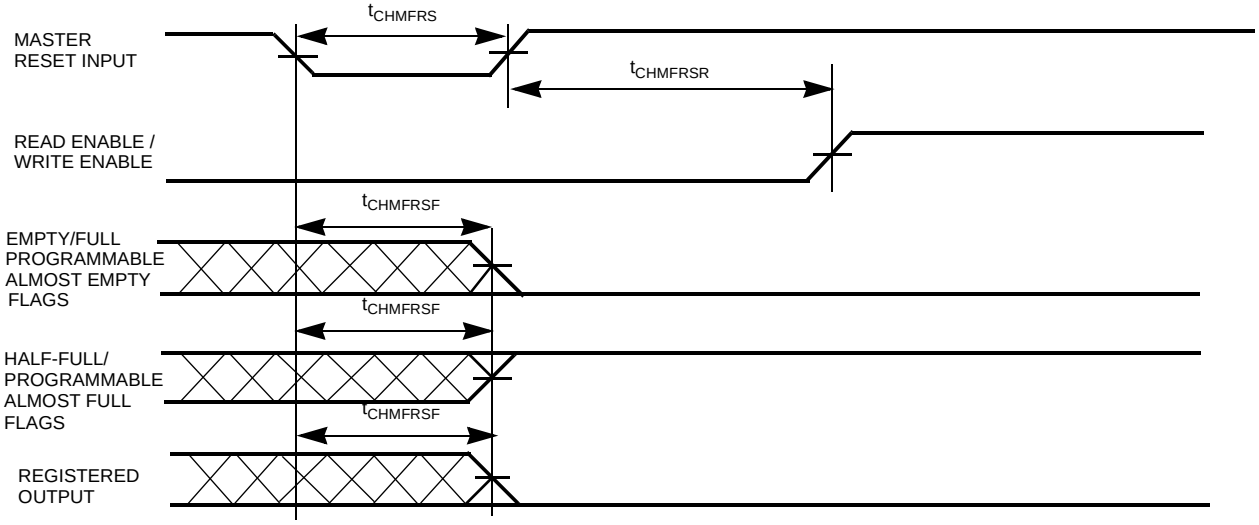
Channel Memory Synchronous FIFO Programmable Flag Timing



Switching Waveforms (continued)



Channel Memory Synchronous FIFO Master Reset Timing



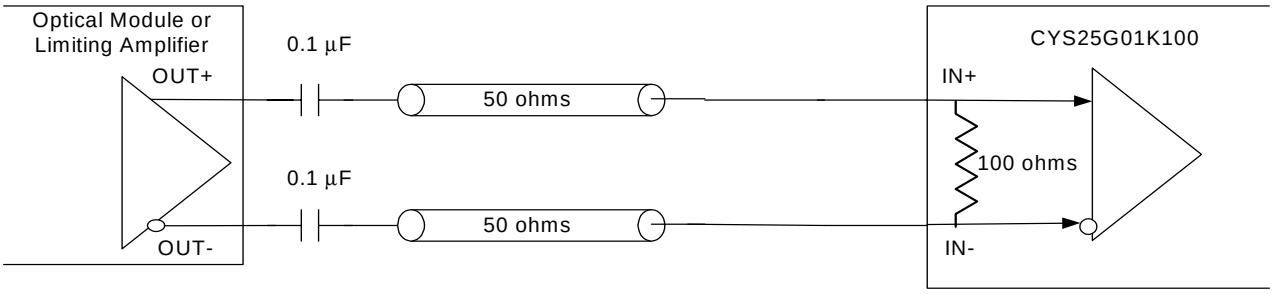


Figure 19. Serial Input Termination

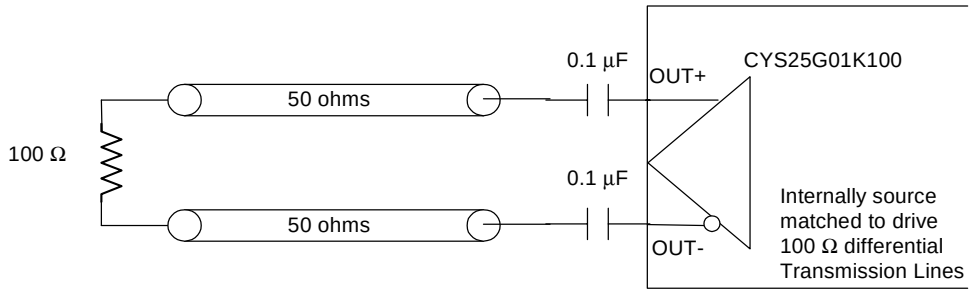


Figure 20. Serial Output Termination

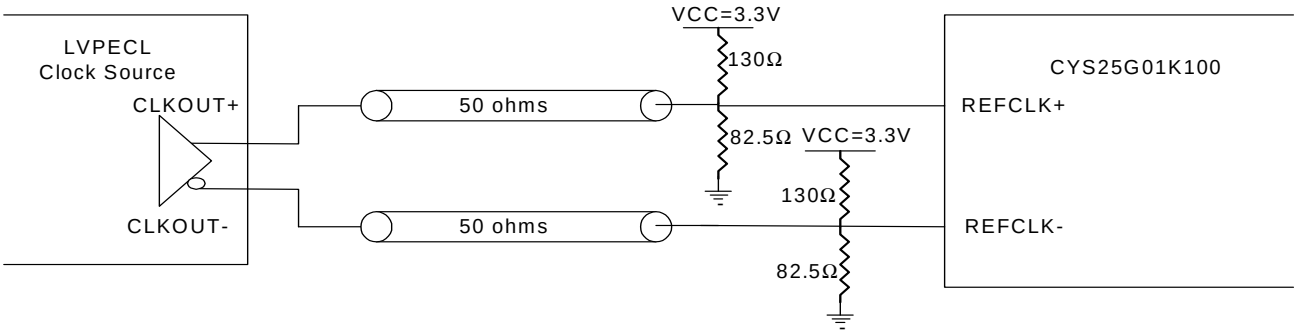


Figure 21. REFCLK Oscillator Termination

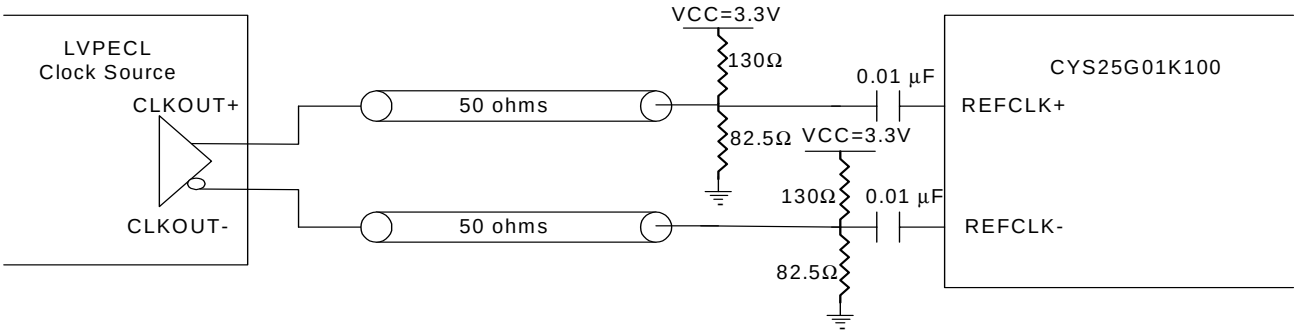


Figure 22. AC-Coupled REFCLK Oscillator Termination

Pin and Signal Description

Name	Function	Signal Description
Standard Device Signals		
CCLK	Output	Configuration Clock for serial interface with the external boot PROM
CDONE	Output	Flag indicating that configuration is complete
CDATA	Input	Pin to receive configuration data from the external boot PROM
GCLK0-1	Input	Global Input Clock signals 0 through 1. Other global clocks are TXCLK and RXCLK.
CCE	Output	Chip select for the external boot PROM
GCTL0-3	Input	Global Control signals 0 through 3
IO/V_{REF0}	Input/Output	Dual function pin: I/O or Reference Voltage for Bank 0
IO/V_{REF1}	Input/Output	Dual function pin: I/O or Reference Voltage for Bank 1
IO/V_{REF2}	Input/Output	Dual function pin: I/O or Reference Voltage for Bank 2
IO/V_{REF3}	Input/Output	Dual function pin: I/O or Reference Voltage for Bank 3
IO/V_{REF4}	Input/Output	Dual function pin: I/O or Reference Voltage for Bank 4
IO/V_{REF5}	Input/Output	Dual function pin: I/O or Reference Voltage for Bank 5

Pin and Signal Description (continued)

Name	Function	Signal Description
IO	Input/Output	Input or Output pin
IO6/Lock	Input/Output	Dual function pin: I/O in Bank 6 or PLL lock output signal
HSTLREF	Input	Reference Voltage for HSTL Specific IO Banks
MSEL	Input	Mode Select Pin
Reconfig	Input	Pin to start configuration of PSI
CRST	Output	Reset signal to interface with the external boot PROM
TCK	Input	JTAG Test Clock
TDI	Input	JTAG Test Data In
TDO	Output	JTAG Test Data Out
TMS	Input	JTAG Test Mode Select
Transmit Path Signals		
TXD[15:0]	Internal	Parallel Transmit Data Inputs to the serial transceiver block. A 16-bit word, sampled by TXCLK↑. TXD[15] is the most significant bit (the first bit transmitted)
TXCLK	Internal	Parallel Transmit Data Input Clock to the serial transceiver block. Divide by 16 of the selected transmit bit-rate clock. One of the four global clocks in the programmable logic.
Receive Path Signals		
RXD[15:0]	Internal	Parallel Receive Data Output from the serial transceiver block. These outputs change following RXCLK↓. RXD[15] is the most significant bit of the output word, and is received first on the serial interface
RXCLK	Internal	Receive Clock Output from the serial transceiver block. Divide by 16 of the bit-rate clock extracted from the received serial stream. One of the four global clocks in the programmable.
CMSER	Analog	Common Mode Termination. Capacitor (0.1 µF) shunt to V_{SS} for common mode noise
RXCN1	Analog	Receive Loop Filter Capacitor (Negative)
RXCN2	Analog	Receive Loop Filter Capacitor (Negative)
RXCP1	Analog	Receive Loop Filter Capacitor (Positive)
RXCP2	Analog	Receive Loop Filter Capacitor (Positive)
Transceiver Control and Status Signals		
REFCLK±	Differential LVPECL input	Reference Clock. This clock input is used as the timing reference for the transmit and receive PLLs. A derivative of this input clock may also be used to clock the transmit parallel interface
$\overline{\text{LFI}}$	Internal	Line Fault Indicator Output Signal. When LOW, this signal indicates that the selected receive data stream has been detected as invalid by either a LOW input on SD, or by the receive VCO being operated outside its specified limits
$\overline{\text{RESET}}$	Internal	Reset for all logic functions in the serial transceiver block except the transmit FIFO
$\overline{\text{LOCKREF}}$	Internal	Receive PLL Lock to Reference Input Signal. When LOW, the receive PLL locks to REFCLK instead of the received serial data stream
SD	LVTTL input	Signal Detect. When LOW, the receive PLL locks to REFCLK instead of the received serial data stream
FIFO_ERR	Internal	Transmit FIFO Error Output Signal. When HIGH the transmit FIFO has either under or overflowed. The FIFO must be reset to clear the error indication
$\overline{\text{FIFO\_RST}}$	Internal	Transmit FIFO Reset Input Signal. When LOW, the in and out pointers of the transmit FIFO are set to maximum separation
$\overline{\text{PWRDN}}$	Internal	Device Power Down Input Signal. When LOW, the logic and drivers are all disabled and placed into a standby condition where only minimal power is dissipated

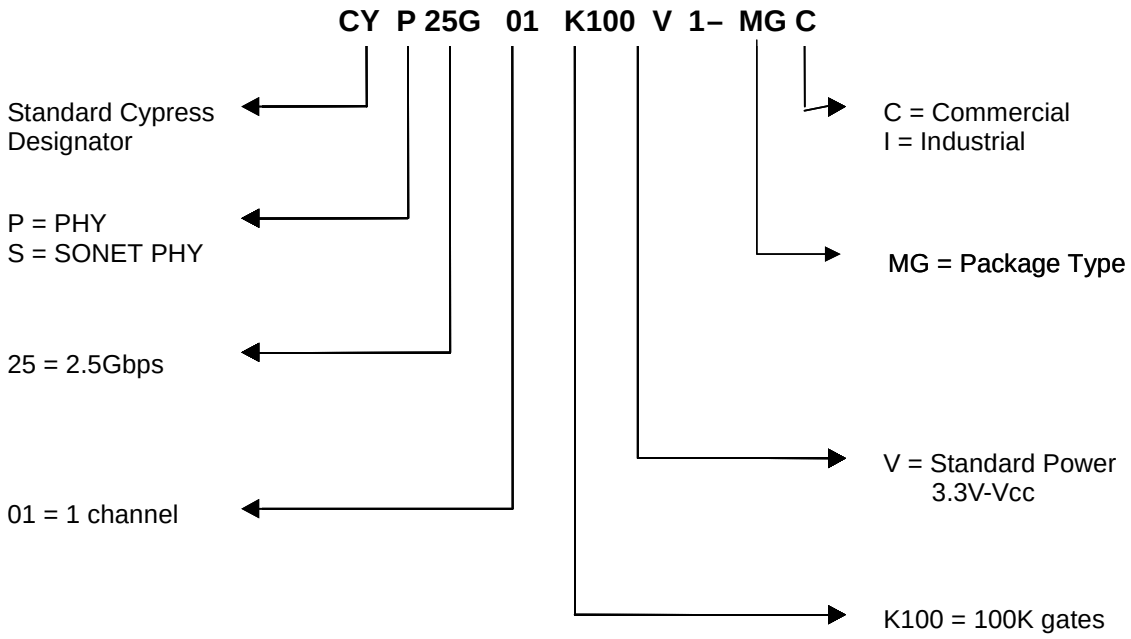
Pin and Signal Description (continued)

Name	Function	Signal Description
Transceiver Loop Control Signals		
DIAGLOOP	Internal	Diagnostic Loopback Control Input Signal. When HIGH, transmit data is routed through the receive clock and data recovery and presented at the RXD[15:0] outputs. When LOW, received serial data is routed through the receive clock and data recovery and presented at the RXD[15:0] outputs
LINELOOP	Internal	Line Loopback Control Input Signal. When HIGH, received serial data is looped back from receive to transmit after being reclocked by a recovered clock. When LINELOOP is LOW, the data passed to the OUT± line driver is controlled by LOOPA. When both LINELOOP and LOOPA are LOW, the data passed to the OUT± line driver is generated in the transmit shifter
LOOPA	Internal	Analog Line Loopback Input Signal. When LINELOOP is LOW and LOOPA is HIGH, received serial data is looped back from receive input buffer to transmit output buffer, but is not routed through the clock and data recovery PLL. When LOOPA is LOW, the data passed to the OUT± line driver is controlled by LINELOOP
LOOPTIME	Internal	Loop Time Mode Input Signal. When HIGH, the extracted receive bit-clock replaces transmit bit-clock. When LOW, the REFCLK input is multiplied by 16 to generate the transmit bit clock
Serial I/O		
OUT±	Differential CML output	Differential Serial Data Output. This differential CML output (+3.3V referenced) is capable of driving terminated 50Ω transmission lines or commercial fiberoptic transmitter modules
IN±	Differential CML input	Differential Serial Data Input. This differential input accept the serial data stream for deserialization and clock extraction
Power		
V_{CC}	Power	+3.3V Supply (operating voltage)
GND	Ground	Signal and Power Ground
V_{CCQ}		+3.3V Quiet Power
V_{SSQ}		Quiet Ground
V_{DDQ}		+1.5V Supply for HSTL Outputs
V_{CCIO0}	Power	V_{CC} for I/O bank 0
V_{CCIO1}	Power	V_{CC} for I/O bank 1
V_{CCIO2}	Power	V_{CC} for I/O bank 2
V_{CCIO3}	Power	V_{CC} for I/O bank 3
V_{CCIO4}	Power	V_{CC} for I/O bank 4
V_{CCIO5}	Power	V_{CC} for I/O bank 5
V_{CCJTAG}	Power	V_{CC} for JTAG pins
V_{CCCFG}	Power	V_{CC} for Configuration port
V_{CCPLL}	Power	V_{CC} for logic PLL
GNPLL	Ground	Ground for logic PLL
V_{CEP}	Power	V_{CC} for the Self-Boot™ solution embedded boot PROM

Pin Configurations

456-ball BGA (25G01K100): Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	GND	HSTL-REF	IO7	IO7	IO7	IO7	HSTL-REF	IO7	IO7	IO7	HSTL-REF	HSTL-REF	IO6	IO6	IO6	HSTL-REF	IO5	IO5	IO5	IO/VREF5	IO5	IO5	IO5	IO/VREF5	IO5	GND	A
B	HSTL-REF	HSTL-REF	IO7	HSTL-REF	IO7	IO7	IO7	VDDQ	IO7	HSTL-REF	IO6	IO6	IO6	IO6	IO6	IO6	IO5	IO5	IO5	IO5	IO5	IO/VREF5	IO5	IO5	IO5	IO5	B
C	IO0	IO7	IO7	IO7	VDDQ	VCC	VCC	IO7	GCTL3	IO7	VDDQ	VDDQ	VDDQ	HSTL-REF	IO6	IO6	IO5	IO5	IO5	GCTL2	GCTL1	IO5	IO5	IO5	TDO	TCK	C
D	IO0	IO0	IO0	IO7	VDDQ	VDDQ	VDDQ	GND	HSTL-REF	IO7	NC	VDDQ	VCC	IO6	IO6	IO6	VCCPLL	VDDQ	VDDQ	VDDQ	VCC	NC	GCLK1	IO5	TMS	TDI	D
E	IO0	IO0	IO0	GCTL0	GND	GND	IO7	GND	GND	HSTL-REF	IO6	IO6	IO6	IO6/Lock	IO6	IO6	IO/VREF5	IO5	IO5	IO5	IO5	IO5	VCCIO5	VCCIO5	VCCIO5	VCCJTAG	E
F	IO/VREF0	IO0	IO0	VCC	GND																	NC	NC	NC	NC	NC	F
G	IO0	IO/VREF0	VCC	VCCIO0	GCLK0																	NC	NC	NC	NC	NC	G
H	IO0	IO0	VCC	VCCIO0	GND																	NC	VSSQ	VSSQ	NC	NC	H
J	IO0	IO0	VCC	VCCIO0	GND																	NC	VSSQ	VSSQ	VSSQ	NC	J
K	IO0	IO0	IO0	IO0	VCC																	VSSQ	VSSQ	VSSQ	NC	NC	K
L	IO0	IO0	IO0	GND	IO0						GND	GND	GND	GND	GND	GNPLL						NC	NC	NC	NC	NC	L
M	IO0	IO/VREF0	IO0	GND	IO0						GND	GND	GND	GND	GND	GND						SD	RXCN1	RXCP1	RXCN2	RXCP2	M
N	VCC	IO0	IO0	GND	IO/VREF0						GND	GND	GND	GND	GND	GND						NC	VCCQ	VCCQ	VCCQ	VCCQ	N
P	IO1	IO1	IO1	IO1	IO0						GND	GND	GND	GND	GND	GND						NC	VSSQ	VSSQ	IN+	IN-	P
R	IO1	IO1	IO1	VCCIO1	GND						GND	GND	GND	GND	GND	GND						NC	VSSQ	VSSQ	VSSQ	CMSER	R
T	IO/VREF1	IO/VREF1	IO1	IO1	IO1						GND	GND	GND	GND	GND	GND						VSSQ	VSSQ	VSSQ	OUT+	OUT-	T
U	IO1	IO1	IO1	GND	GND																	NC	VCCQ	VCCQ	VCCQ	VCCQ	U
V	IO1	IO1	IO/VREF1	IO1	GND																	REF-CLK+	VCCIO4	IO4	IO4	VCCIO4	V
W	IO1	IO1	IO1	IO1	GND																	REF-CLK-	VCCIO4	IO4	IO4	IO4	W
Y	IO1	IO1	VCEP	IO1	IO1																	IO4	VCEP	IO4	IO4	IO/VREF4	Y
AA	IO1	IO1	VCCIO1	IO/VREF1	GND																	IO4	NC	IO4	IO4	IO4	AA
AB	GND	CDONE	VCCIO1	IO1	IO2	GND	GND	GND	IO2	IO/VREF2	IO2	IO2	IO3	IO3	GND	IO3	GND	GND	GND	IO3	IO3	IO3	IO4	IO4	IO4	IO4	AB
AC	CDATA	RECONFIG	IO2	IO2	VCCCFG	VCCIO2	VCCIO2	VCCIO2	VCCIO2	NC	IO2	IO2	IO2	VDDQ	VCCIO3	VCCIO3	IO3	IO3	IO/VREF3	NC	NC	VCCIO4	IO/VREF4	IO/VREF4	IO4	IO4	AC
AD	CRST	CCLK	IO2	IO2	IO2	IO2	IO2	NC	VDDQ	VDDQ	IO2	IO2	IO/VREF2	IO2	IO3	IO3	IO3	IO3	IO3	VCC	VCCIO3	VCCIO3	IO/VREF3	IO3	IO3	IO3	AD
AE	CCE	MSEL	IO/VREF2	IO2	IO/VREF2	IO2	IO2	IO2	IO2	IO2	IO/VREF2	IO2	IO2	IO2	IO3	IO3	IO3	IO3	IO3	IO3	IO/VREF3	IO3	IO3	IO3	IO/VREF3	IO3	AE
AF	GND	IO2	IO2	IO2	IO2	IO2	IO/VREF2	IO2	IO2	IO2	IO2	IO2	VCC	IO/VREF3	IO3	IO3	IO/VREF3	IO3	IO3	IO3	IO3	IO3	IO3	IO3	IO3	GND	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

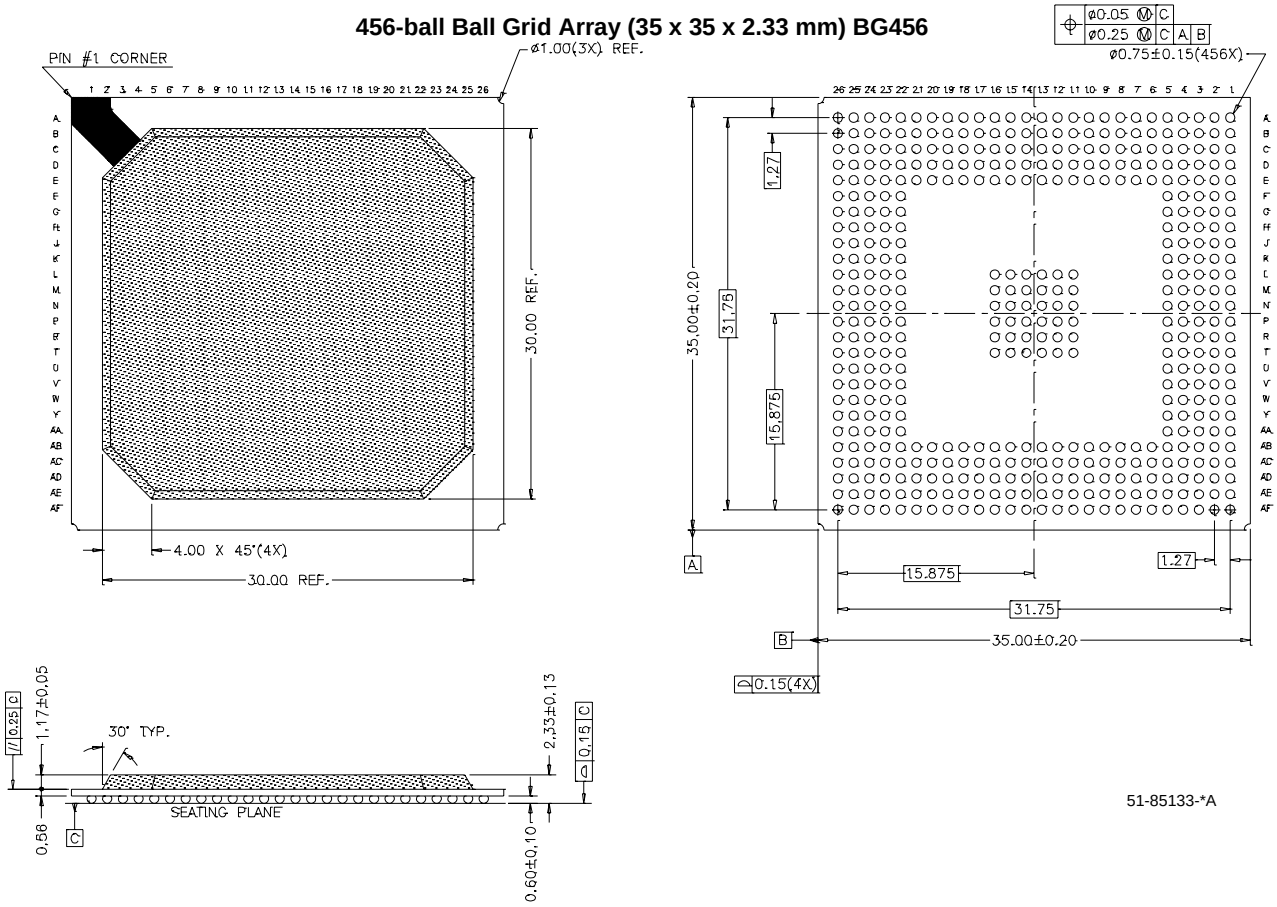


Ordering Information

Device	Channels and Link Speed	Ordering Code	Package Name	Package Type	Operating Range
25G01K100	1 x 2.5 Gbps	CYP25G01K100V1-MGC	456MGC	456-ball Ball Grid Array	Commercial
	1 x 2.5 Gbps	CYS25G01K100V1-MGC	456MGC	456-ball Ball Grid Array	

Package Diagram

456-ball Ball Grid Array (35 x 35 x 2.33 mm) BG456



Document History Page

Document Title: 2.5-Gbps Programmable Serial Interface Document Number: 38-02021				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106745	05/25/01	SZV	Change from Spec #38-01093 to 38-02021
*A	107726	06/04/01	MHW	Updated Marketing Part Numbers
*B	109064	09/07/01	MHW	Added x8 feature in PLL and CHAR data
*C	120882	12/13/02	PDS	Revised data sheet to reflect only 2.5-Gbps single channel 100K programmable logic PSI data. Added SONET jitter specs and jitter performance data for CYS25G01K100. Added REFCLK phase noise limits plot for CYS25G01K100. Changed title. Updated logic PLL data with additional multiplication factors available. Added sections titled “Registering TXD[15:0] Data Before it enters Serial Transceiver Block” and “Registering RXD[15:0] Data before it enters Programmable LB” under the major section called “Serial Transceiver Operation.” Updated some Timing Parameter Values. Updated Output Differential Swing and Input Differential Voltage.