

January 1994

## Dual FIR Filter

### Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Two Independent 8-Tap FIR Filters Configurable as a Single 16-Tap FIR
- 10-Bit Data & Coefficients
- On-Board Storage for 32 Programmable Coefficient Sets
- Up To: 256 FIR Taps, 16 x 16 2-D Kernels, or 10 x 20-Bit Data and Coefficients
- Programmable Decimation to 16
- Programmable Rounding on Output
- Standard Microprocessor Interface
- 33MHz, 25.6MHz Versions

### Applications

- Quadrature, Complex Filtering
- Correlation
- Image Processing
- PolyPhase Filtering
- Adaptive Filtering

### Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43168GM-25/883	-55°C to +125°C	84 Lead PGA
HSP43168GM-33/883	-55°C to +125°C	84 Lead PGA

### Description

The HSP43168 Dual FIR Filter consists of two independent 8-tap FIR filters. Each filter supports decimation from 1 to 16 and provides on-board storage for 32 sets of coefficients. The Block Diagram shows two FIR cells each fed by a separate coefficient bank and one of two separate inputs. The outputs of the FIR cells are either summed or multiplexed by the MUX/Adder. The compute power in the FIR Cells can be configured to provide quadrature filtering, complex filtering, 2-D convolution, 1-D/2-D correlations, and interpolating/decimating filters.

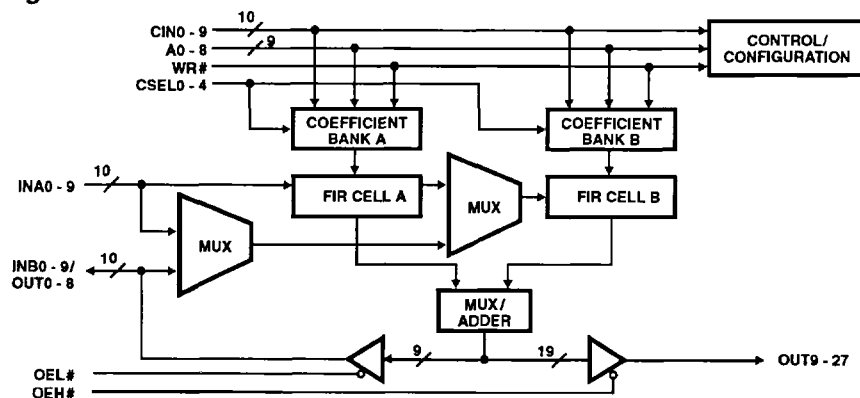
The FIR cells take advantage of symmetry in FIR coefficients by pre-adding data samples prior to multiplication. This allows an 8-tap FIR to be implemented using only 4 multipliers per filter cell. These cells can be configured as either a single 16-tap FIR filter or dual 8-tap FIR filters. Asymmetric filtering is also supported.

Decimation of up to 16 is provided to boost the effective number of filter taps from 2 to 16 times. Further, the decimation registers provide the delay necessary for fractional data conversion and 2-D filtering with kernels to 16x16.

The flexibility of the Dual is further enhanced by 32 sets of user programmable coefficients. Coefficient selection may be changed asynchronously from clock to clock. The ability to toggle between coefficient sets further simplifies applications such as polyphase or adaptive filtering.

The HSP43168 is a low power fully static design implemented in an advanced CMOS process. The configuration of the device is controlled through a standard microprocessor interface.

### Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.  
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File Number 3177.2

Pinouts

84 PIN PGA  
TOP VIEW

	11	10	9	8	7	6	5	4	3	2	1	
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
K	OUT18	V <sub>CC</sub>	OUT16	OUT13	V <sub>CC</sub>	INB0	INB2	GND	INB7	INB8	INA1	K
J	OUT19	OUT17			OUT9	OEL#	INB3			INA0	INA2	J
H	OUT21	OUT20								INA3	INA4	H
G	OUT24	OUT23	OUT25						INA7	INA5	INA6	G
F	OUT27	OUT22	OUT26						INA8	INA9	V <sub>CC</sub>	F
E	OE#	GND	CLK						CIN2	CIN1	CIN0	E
D	V <sub>CC</sub>	ACCEN								GND	CIN3	D
C	TXFR#	FWRD#			A5	A6	CSEL0			CIN6	CIN4	C
B	SHFT EN#	MUX0	MUX1	A0	A3	A2	V <sub>CC</sub>	CSEL2	CIN9	CIN7	CIN5	B
A	RVRS#	WR#	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A PIN 'A1' ID
	11	10	9	8	7	6	5	4	3	2	1	

84 PIN PGA  
BOTTOM VIEW

	11	10	9	8	7	6	5	4	3	2	1	
A	RVRS#	WR#	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A PIN 'A1' ID
B	SHFT EN#	MUX0	MUX1	A0	A3	A2	V <sub>CC</sub>	CSEL2	CIN9	CIN7	CIN5	B
C	TXFR#	FWRD#			A5	A6	CSEL0			CIN6	CIN4	C
D	V <sub>CC</sub>	ACCEN								GND	CIN3	D
E	OE#	GND	CLK							CIN2	CIN1	E
F	OUT27	OUT22	OUT26							INA8	INA9	V <sub>CC</sub>
G	OUT24	OUT23	OUT25							INA7	INA5	INA6
H	OUT21	OUT20								INA3	INA4	H
J	OUT19	OUT17			OUT9	OEL#	INB3			INA0	INA2	J
K	OUT18	V <sub>CC</sub>	OUT16	OUT13	V <sub>CC</sub>	INB0	INB2	GND	INB7	INB8	INA1	K
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
	11	10	9	8	7	6	5	4	3	2	1	

## Specifications HSP43168/883

### Absolute Maximum Ratings

Supply Voltage .....	+8.0V
Input, Output or I/O Voltage .....	GND-0.5V to $V_{CC}+0.5V$
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	+175°C
Lead Temperature (Soldering 10s) .....	+300°C
ESD Classification .....	Class 1

### Reliability Information

Thermal Resistance	$\theta_{JA}$	$\theta_{JC}$
Ceramic PGA Package .....	33.5°C/W	7.5°C/W
Maximum Package Power Dissipation at +125°C		
Ceramic PGA Packazge .....	1.49 W	
Gate Count .....	32529 Gates	

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### Operating Conditions

Operating Voltage Range .....	+4.5V to +5.5V	Operating Temperature Range .....	-55°C to +125°C
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**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Logical One Input Voltage	$V_{IH}$	$V_{CC} = 5.5V$	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	2.2	-	V
Logical Zero Input Voltage	$V_{IL}$	$V_{CC} = 4.5V$	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	-	0.8	V
Logical One Input Voltage Clock	$V_{IHC}$	$V_{CC} = 5.5V$	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	3.0	-	V
Logical Zero Input Voltage Clock	$V_{ILC}$	$V_{CC} = 4.5V$	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	-	0.8	V
Output HIGH Voltage	$V_{OH}$	$I_{OH} = -400\mu A$ $V_{CC} = 4.5V$ (Note 1)	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	2.6	-	V
Output LOW Voltage	$V_{OL}$	$I_{OL} = +2.0mA$ $V_{CC} = 4.5V$ (Note 1)	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	-	0.4	V
Input Leakage Current	$I_I$	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	-10	+10	$\mu A$
Output Leakage Current	$I_O$	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	-10	+10	$\mu A$
Standby Power Supply Current	$I_{CCSB}$	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$ , Outputs Open	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	-	500	$\mu A$
Operating Power Supply Current	$I_{CCOP}$	$f = 25.6MHz$ , $V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5V$ (Note 2)	1, 2, 3	$-55^\circ \leq T_A \leq +125^\circ C$	-	281.6	mA
Functional Test	FT	(Note 3)	7, 8	$-55^\circ \leq T_A \leq +125^\circ C$	-	-	-

**NOTES:**

1. Interchanging of force and sense conditions is permitted.
2. Operating Supply Current is proportional to frequency, typical rating is 11mA/MHz.
3. Tested as follows:  $f = 1MHz$ ,  $V_{IH}(\text{clock inputs}) = 3.4V$ ,  $V_{IH}$  (all other inputs) = 2.6V,  $V_{IL} = 0.4V$ ,  $V_{OH} \geq 1.5V$ , and  $V_{OL} \leq 1.5V$ .

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1D FILTERS

**Specifications HSP43168/883**

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	(-33MHz)		(-25MHz)		UNITS
					MIN	MAX	MIN	MAX	
CLK Period	T <sub>CP</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	30	-	39	-	ns
CLK High	T <sub>CH</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	12	-	15	-	ns
CLK Low	T <sub>CL</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	12	-	15	-	ns
WR# Period	T <sub>WP</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	30	-	39	-	ns
WR# High	T <sub>WH</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	12	-	15	-	ns
WR# Low	T <sub>WL</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	12	-	15	-	ns
Set-up Time; A0-8 to WR# Low	T <sub>AWs</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	10	-	10	-	ns
Hold Time; A0-8 to WR# High	T <sub>AWH</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	1	-	1	-	ns
Set-up Time; CIN0-9 to WR# High	T <sub>CWS</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	12	-	15	-	ns
Hold Time; CIN0-9 to WR# High	T <sub>CWH</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	1.5	-	1.5	-	ns
Set-up Time; WR# Low to CLK Low	T <sub>WLCL</sub>	Note 3	9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	5	-	8	-	ns
Set-up Time; CIN0-9 to CLK Low	T <sub>CVCL</sub>	Note 3	9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	8	-	8	-	ns
Set-up Time; CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, MUX0-1 to CLK High	T <sub>ECS</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	15	-	17	-	ns
Hold Time; CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, MUX0-1 to CLK High	T <sub>ECH</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	0	-	0	-	ns
CLK to Output Delay OUT0-27	T <sub>DO</sub>		9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	-	15	-	17	ns
Output Enable Time	T <sub>OE</sub>	Note 2	9, 10, 11	-55° ≤ T <sub>A</sub> ≤ +125°C	-	12	-	12	ns

**NOTES:**

- AC testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 3.0V and 0V; Timing reference levels (CLK) 2.0V; All others 1.5V. V<sub>CC</sub> = 4.5V and 5.5V. Output load per test load circuit with C<sub>L</sub> = 40 pF. Output transition is measured at V<sub>OH</sub> > 1.5V and V<sub>OL</sub> < 1.5V.
- Transition is measured at ±200mV from steady state voltage, Output loading per test load circuit, C<sub>L</sub> = 40pF.
- Set-up time requirements for loading of data on CIN0-9 to guarantee recognition on the following clock.

**Specifications HSP43168/883**

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	(-33MHz)		(-25MHz)		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	$C_{IN}$	$V_{CC}$ = Open, $f=1$ MHz All measurements are referenced to device GND.	1	$T_A = +25^{\circ}C$	-	12	-	12	pF
Output Capacitance	$C_{OUT}$		1	$T_A = +25^{\circ}C$	-	12	-	12	pF
Output Disable Time	$T_{OD}$		1, 2	$-55^{\circ} \leq T_A \leq +125^{\circ}C$	-	12	-	12	ns
Output Rise Time	$T_R$	From 0.8V to 2.0V	1, 2	$-55^{\circ} \leq T_A \leq +125^{\circ}C$	-	8	-	8	ns
Output Fall Time	$T_F$	From 2.0V to 0.8V	1, 2	$-55^{\circ} \leq T_A \leq +125^{\circ}C$	-	8	-	8	ns

NOTE:

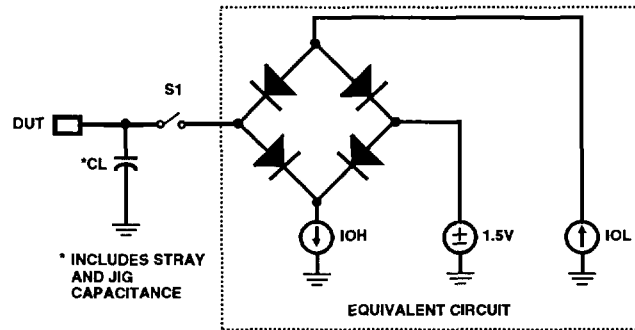
1. The parameters in Table 3 are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with  $C_L = 40pF$ .

**TABLE 4. APPLICABLE SUBGROUPS**

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

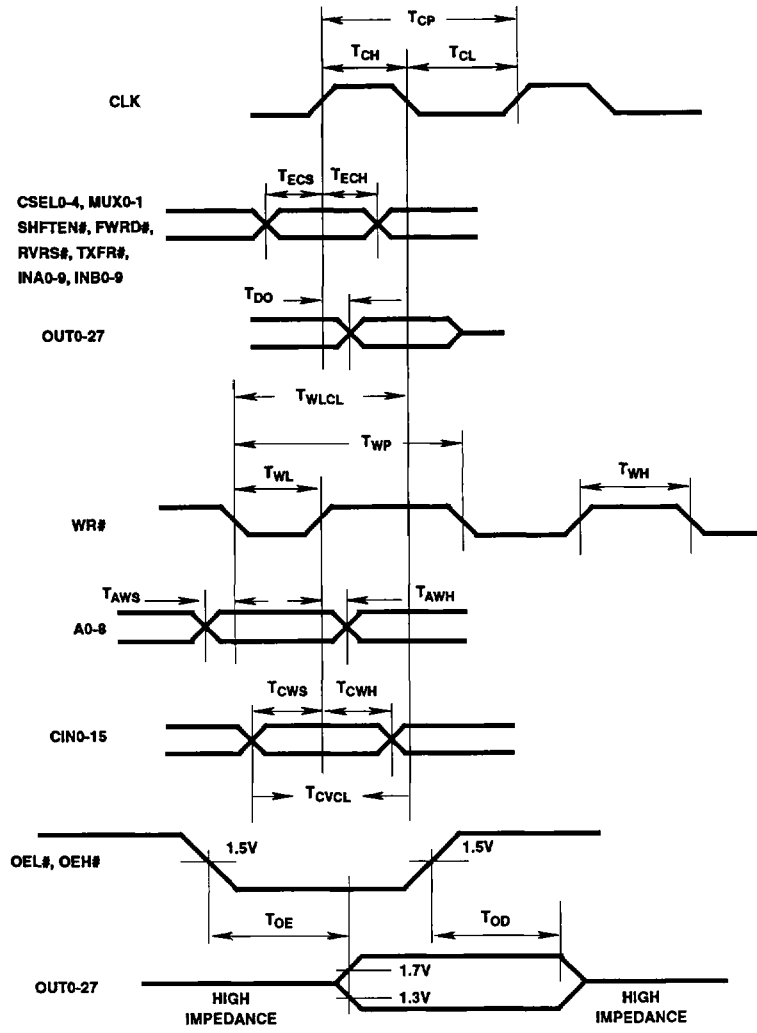
**3**  
**1D FILTERS**

**AC Test Load Circuit**

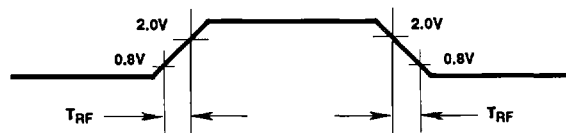


SWITCH S1 OPEN FOR  $I_{CCSB}$  AND  $I_{CCOP}$  TEST

Waveforms



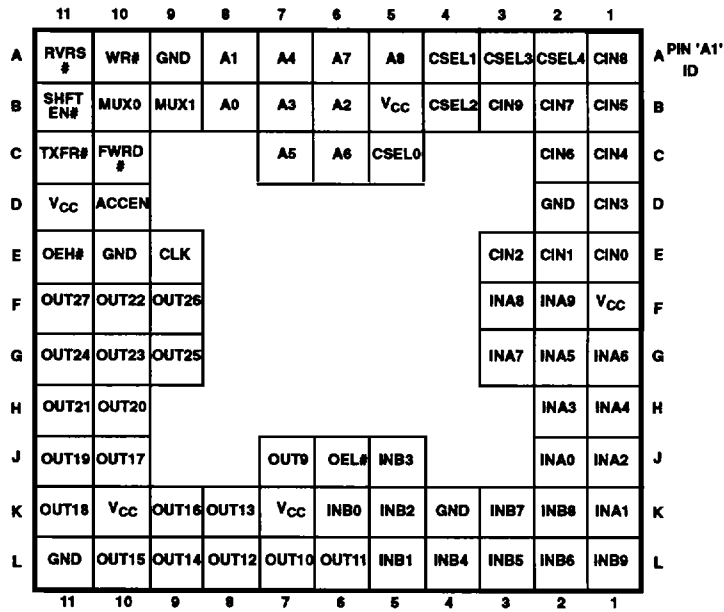
OUTPUT ENABLE, DISABLE TIMING



OUTPUT RISE AND FALL TIMES

**Burn-In Circuit**

84 PIN PGA  
BOTTOM VIEW



NOTES:

1. V<sub>CC</sub>/2 (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V<sub>CC</sub> and GND
3. V<sub>CC</sub> = 5.5 ±0.5V.
4. 0.1µf (Min) capacitor between V<sub>CC</sub> and GND per position.
5. F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2 . . . , F16 = F15/2, 40 to 60% duty cycle.
6. Input voltage limits:  
V<sub>IL</sub> = 0.8V Max, V<sub>IH</sub> = 4.5 ±10%

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	CIN8	F9	B11	SHFTEN	F14	F9	SUM26	V <sub>CC</sub> /2	K2	INB8	F9
A2	CSEL4	F12	C1	CIN4	F7	F10	SUM22	V <sub>CC</sub> /2	K3	INB7	F8
A3	CSEL3	F11	C2	CIN6	F9	F11	SUM27	V <sub>CC</sub> /2	K4	GND	GND
A4	CSEL1	F9	C5	CSEL0	F8	G1	INA6	F7	K5	INB2	F3
A5	A8	F12	C6	A6	F11	G2	INA5	F6	K6	INB0	F1
A6	A7	F10	C7	A5	F12	G3	INA7	F8	K7	V <sub>CC</sub>	V <sub>CC</sub>
A7	A4	F11	C10	FWRD	F13	G9	SUM25	V <sub>CC</sub> /2	K8	SUM13	V <sub>CC</sub> /2
A8	A1	F12	C11	TXFR	F11	G10	SUM23	V <sub>CC</sub> /2	K9	SUM16	V <sub>CC</sub> /2
A9	GND	GND	D1	CIN3	F10	G11	SUM24	V <sub>CC</sub> /2	K10	V <sub>CC</sub>	V <sub>CC</sub>
A10	WRB	F6	D2	GND	GND	H1	INA4	F5	K11	SUM18	V <sub>CC</sub> /2
A11	RVRs	F12	D10	ACCEN	F13	H2	INA3	F4	L1	INB9	F10
B1	CIN5	F8	D11	V <sub>CC</sub>	V <sub>CC</sub>	H10	SUM20	V <sub>CC</sub> /2	L2	INB6	F7
B2	CIN7	F10	E1	CIN0	F7	H11	SUM21	V <sub>CC</sub> /2	L3	INB5	F6
B3	CIN9	F10	E2	CIN1	F8	J1	INA2	F3	L4	INB4	F5
B4	CSEL2	F10	E3	CIN2	F9	J2	INA0	F1	L5	INB1	F2
B5	V <sub>CC</sub>	V <sub>CC</sub>	E9	CLK	F0	J5	INB3	F4	L6	SUM11	V <sub>CC</sub> /2
B6	A2	F11	E10	GND	GND	J6	OELB	F13	L7	SUM10	V <sub>CC</sub> /2
B7	A3	F10	E11	OE#	F14	J7	SUM9	V <sub>CC</sub> /2	L8	SUM12	V <sub>CC</sub> /2
B8	A0	F13	F1	V <sub>CC</sub>	V <sub>CC</sub>	J10	SUM17	V <sub>CC</sub> /2	L9	SUM14	V <sub>CC</sub> /2
B9	MUX1	F13	F2	INA9	F10	J11	SUM19	V <sub>CC</sub> /2	L10	SUM15	V <sub>CC</sub> /2
B10	MUX0	F12	F3	INA8	F9	K1	INA1	F2	L11	GND	GND

**Metallization Topology**

**DIE DIMENSIONS:**  
314 x 348 x 19 ± 1mils

**METALLIZATION:**  
Type: Si-Al or Si-Al-Cu  
Thickness: 8kÅ

**GLASSIVATION:**  
Type: Nitrox  
Thickness: 10kÅ

**WORST CASE CURRENT DENSITY:**  
 $1.93 \times 10^5 \text{ A/cm}^2$

**Metallization Mask Layout**

