HARRIS SEMICONDUCTOR

CDP1872C, CDP1874C, CDP1875C

March 1997

High-Speed 8-Bit Input and Output Ports

Features

- Parallel 8-Bit Input/Output Register with Buffered Outputs
- High-Speed Data-In to Data-Out 85ns (Max) at V_{DD} = 5V
- Flexible Applications In Microprocessor Systems as Buffers and Latches
- High Order Address-Latch Capability in CDP1800-Series Microprocessor Systems
- Output Sink Current = 5mA (Min) at V_{DD} = 5V
- Three-State Output - CDP1872C and CDP1874C

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1872CE	-40°C to +85°C	PDIP	E22.4
CDP1874CE	-40°C to +85°C	PDIP	E22.4
CDP1875CE	-40°C to +85°C	PDIP	E22.4

Description

The CDP1872C, CDP1874C and CDP1875C devices are high-speed 8-bit parallel input and output ports designed for use in the CDP1800 microprocessor system and for general use in other microprocessor systems. The CDP1872C and CDP1874C are 8-bit input ports; the CDP1875C is an 8-bit output port.

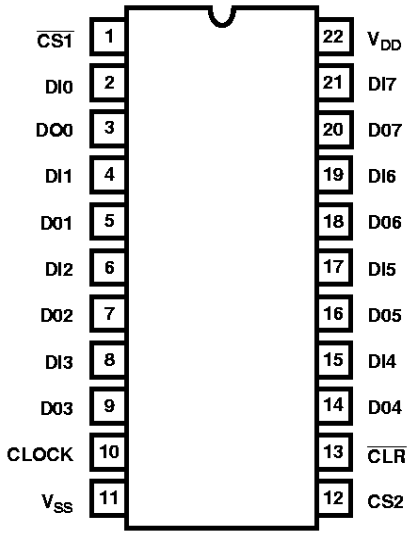
These devices have flexible capabilities as buffers and data latches and are reset by $\overline{CLR}$ input when the data strobe is not active.

The CDP1872C and CDP1874C are functionally identical except for device selects.The CDP1872C has one active low and one active high select; the CDP1874C has two active high device selects. These devices also feature Three-state outputs when deselected. Data is strobed into the register on the leading edge of the CLOCK and latched on the trailing edge of the CLOCK.

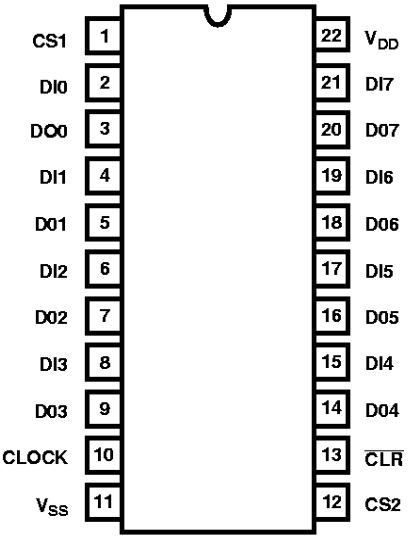
The CDP1875C is an output port with data latched into the registers when the device selects are active. There are two active high and one active low selects. The output buffers are enabled at all times.

Pinouts

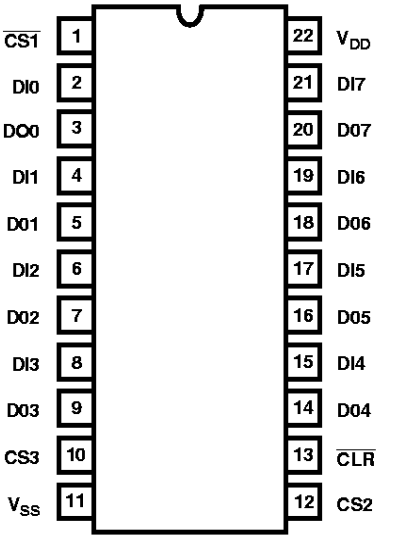
CDP1872C INPUT PORT (PDIP) TOP VIEW



CDP1874C INPUT PORT (PDIP) TOP VIEW



CDP1875C OUTPUT PORT (PDIP) TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1255.2**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}) . . . . . -0.5V to +7V
(Voltage referenced to V_{SS} Terminal)
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
PDIP Package 75
Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type E. . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At distance 1/16 ± 1/32 In. (1.59 ± 0.79mm)
from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

At T_A = -40 to +85°C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS ALL TYPES	UNITS
DC Operating-Voltage Range	4 to 6.5	V
Input Voltage Range	V_{SS} to V_{DD}	V

Static Electrical Specifications

At T_A = -40 to +85°C, V_{DD} ±5%, Unless Otherwise Specified.

PARAMETER		TEST CONDITIONS			LIMITS ALL TYPES			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	25	50	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	5	10	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-4	-7	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
Input Leakage Current	I_{IN}	-	0, 5	5	-	-	±1	µA
Three-State Output Leakage Current (Note 3)	I_{OUT}	0, 5	0, 5	5	-	-	±5	µA
Input Capacitance	C_{IN}	-	-	-	-	15	-	pF
Output Capacitance (Note 3)	C_{OUT}	-	-	-	-	15	-	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD} ±5%.
2. $I_{OL} = I_{OH}$ = 1µA
3. For CDP1872C and CDP1874C only.

Logic Diagrams

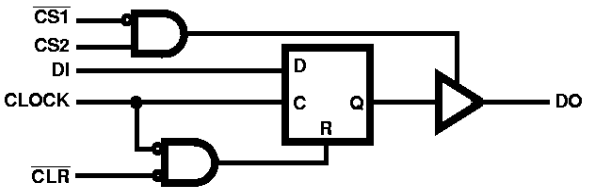


FIGURE 1. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) FOR CDP1872C

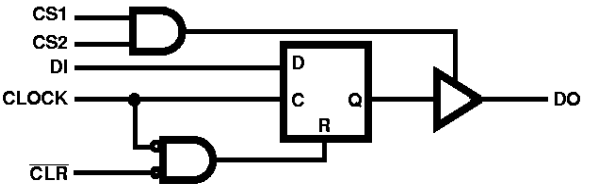


FIGURE 2. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) for CDP1874C

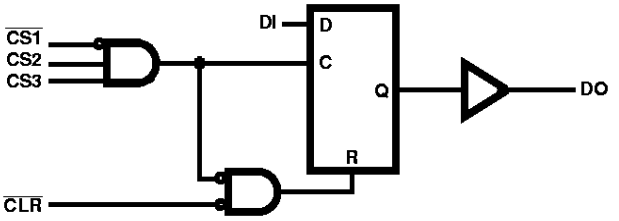


FIGURE 3. EQUIVALENT LOGIC DIAGRAM (1 OF 8 LATCHES SHOWN) FOR CDP1875C

Dynamic Electrical Specifications

At $T_A = 25^oC$, V_{DD} 5V, t_R, t_F = 10ns, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$, C_L = 150pF

PARAMETER		LIMITS CDP1872C, CDP1874C MIN	(NOTE 1) TYP	(NOTE 2) MAX	UNITS
INPUT PORT (FIGURE 4)					
Output Enable	t_{EN}	-	45	90	ns
Output Disable	t_{DIS}	-	45	90	ns
Clock to Data Out	t_{CLO}	-	45	90	ns
$\overline{\text{Clear}}$ to Output	t_{CRO}	-	80	160	ns
Data In to Data Out	t_{DIO}	-	50	85	ns
Minimum Data Setup Time	t_{DSU}	-	10	30	ns
Data Hold Time	t_{DH}	-	10	30	ns
Minimum Clock Pulse Width	t_{CL}	-	30	60	ns
Minimum $\overline{\text{Clear}}$ Pulse Width	t_{CR}	-	30	60	ns

NOTES:

1. Typical values are for $T_A = +25^oC$ and $V_{DD} \pm 5\%$.
2. Maximum values are for $T_A = +85^oC$ and $V_{DD} \pm 5\%$

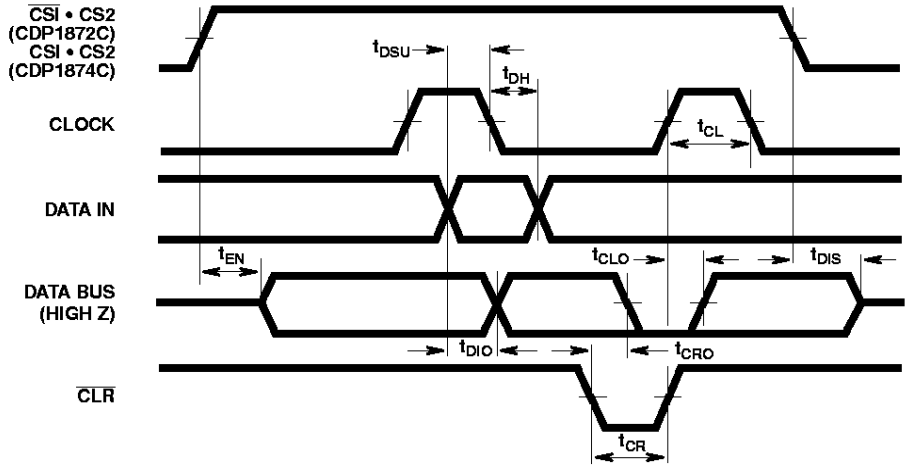


FIGURE 4. TIMING WAVEFORMS FOR CDP1872C AND CDP1874C (INPUT-PORT TYPES)

Dynamic Electrical Specifications At $T_A = 25^oC$, V_{DD} 5V, t_R, $t_F = 10ns$, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$, $C_L = 150pF$

PARAMETER		LIMITS CDP1875C MIN	(NOTE 1) TYP	(NOTE 2) MAX	UNITS
OUTPUT PORT (FIGURE 5)					
Clock to Data Out	t_{CLO}	-	50	100	ns
$\overline{\text{Clear}}$ to Output	t_{CRO}	-	80	160	ns
Data In to Data Out	t_{DIO}	-	50	85	ns
Minimum Data Setup Time	t_{DS}	-	10	30	ns
Data Hold Time	t_{DH}	-	10	30	ns
Minimum $\overline{\text{Clear}}$ Pulse Width	t_{CR}	-	30	60	ns

NOTES:

1. Typical values are for $T_A = +25^oC$ and $V_{DD} \pm 5\%$.
2. Maximum values are for $T_A = +85^oC$ and $V_{DD} \pm 5\%$

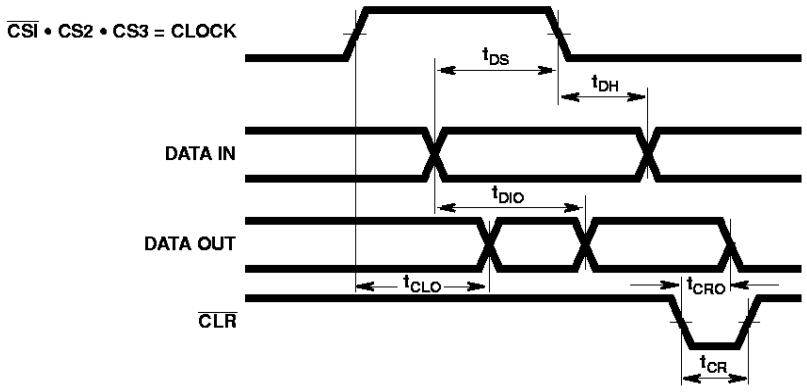


FIGURE 5. TIMING WAVEFORMS FOR CDP1875C (OUTPUT PORT)

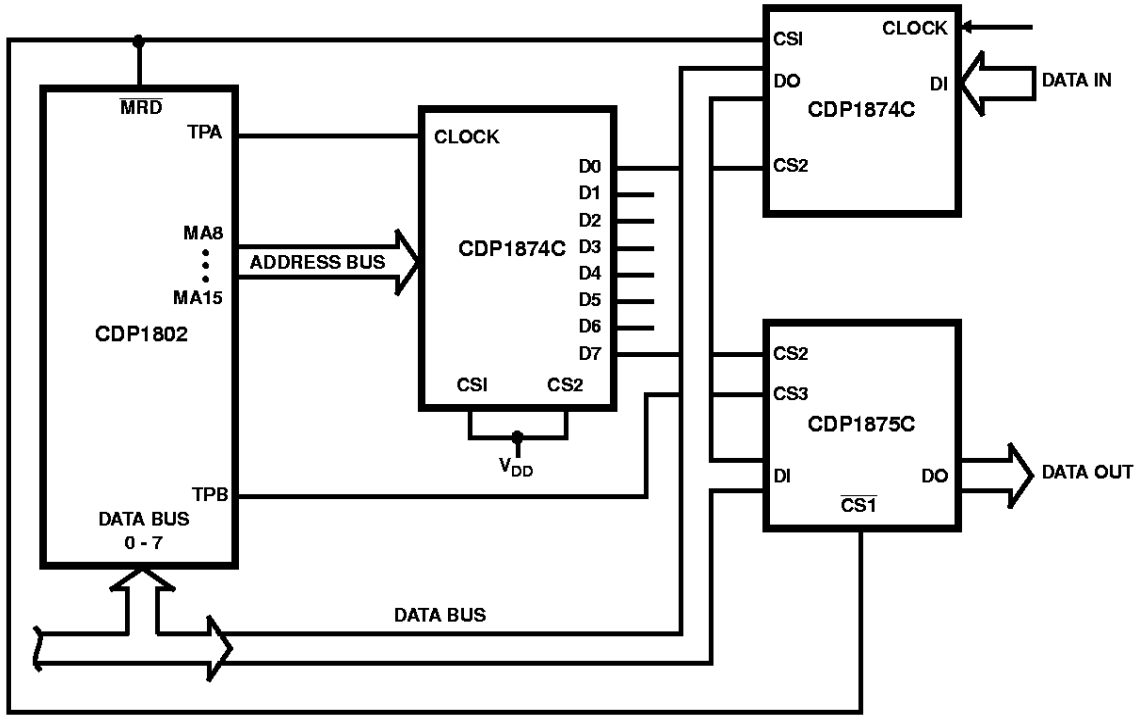


FIGURE 6. CDP1874C USED AS AN INPUT PORT AND ADDRESS LATCH WITH CDP1875C USED AS AN OUTPUT PORT

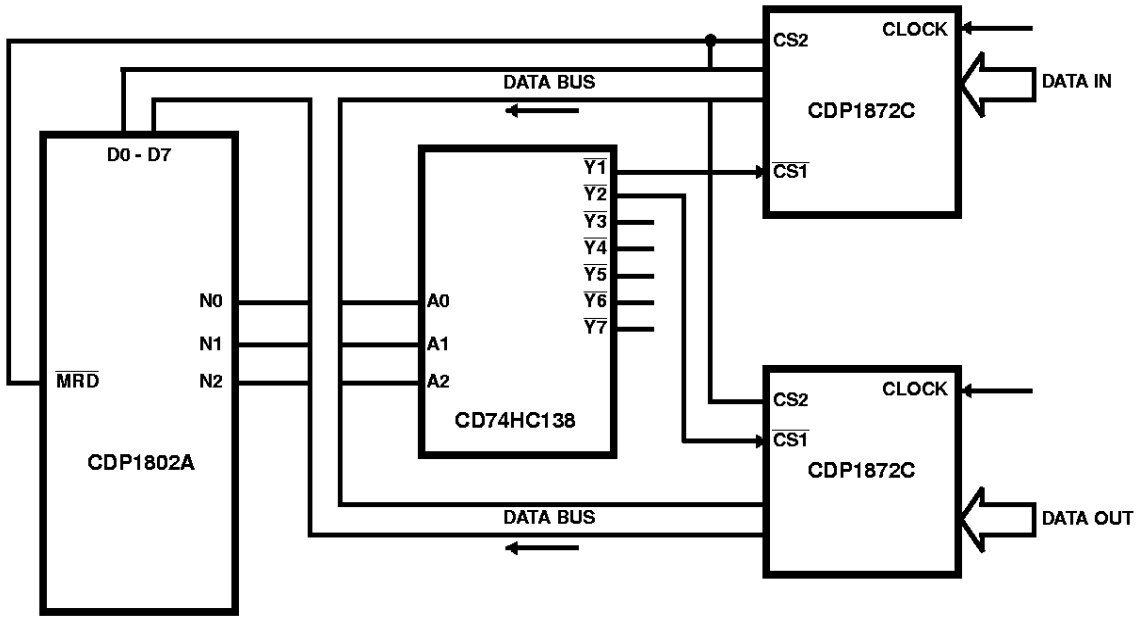


FIGURE 7. CDP1872C USED AS AN INPUT PORT AND SELECTED BY CD74HC138

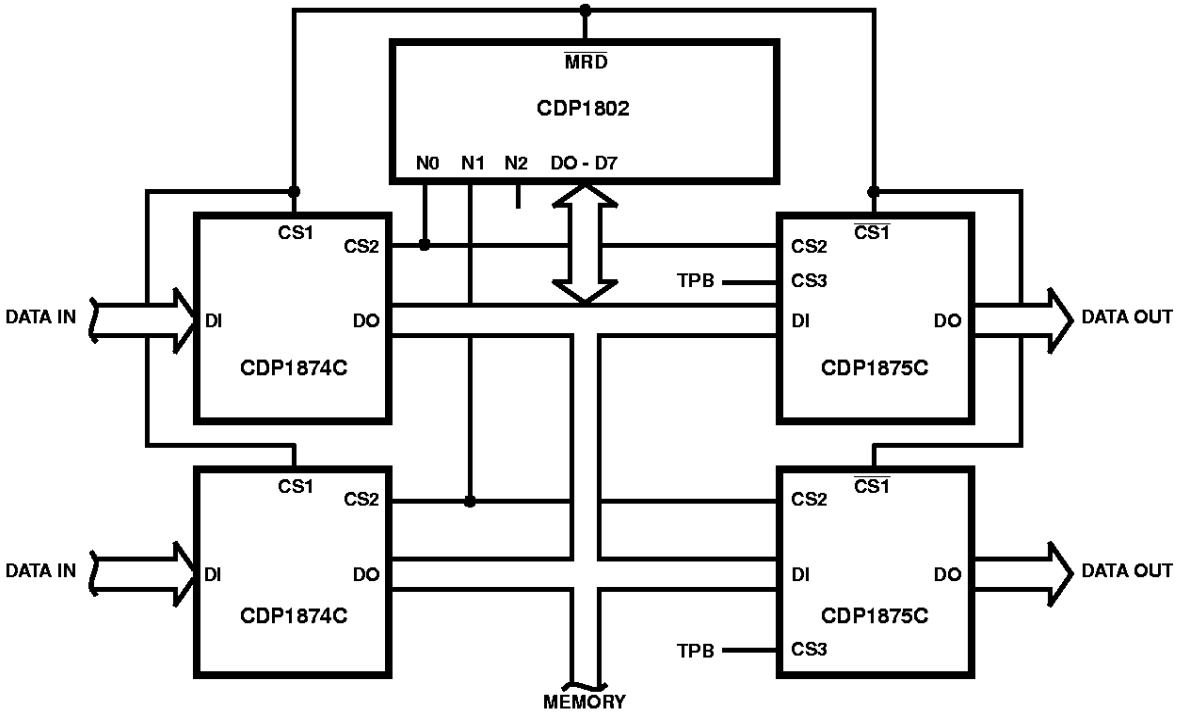


FIGURE 8. CDP1874C AND CDP1875C USED AS INPUT/OUTPUT BUFFERS