

# IS62C5128BL, IS65C5128BL

## 512K x 8 HIGH-SPEED CMOS STATIC RAM

JULY 2011

### FEATURES

- High-speed access time: 45ns
- Low Active Power: 50 mW (typical)
- Low Standby Power: 10  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single 5V  $\pm$  10% power supply
- Fully static operation: no clock or refresh required
- Available in 32-pin sTSOP-I, 32-pin SOP and 32-pin TSOP-II packages
- Commercial, Industrial and Automotive temperature ranges available
- Lead-free available

### DESCRIPTION

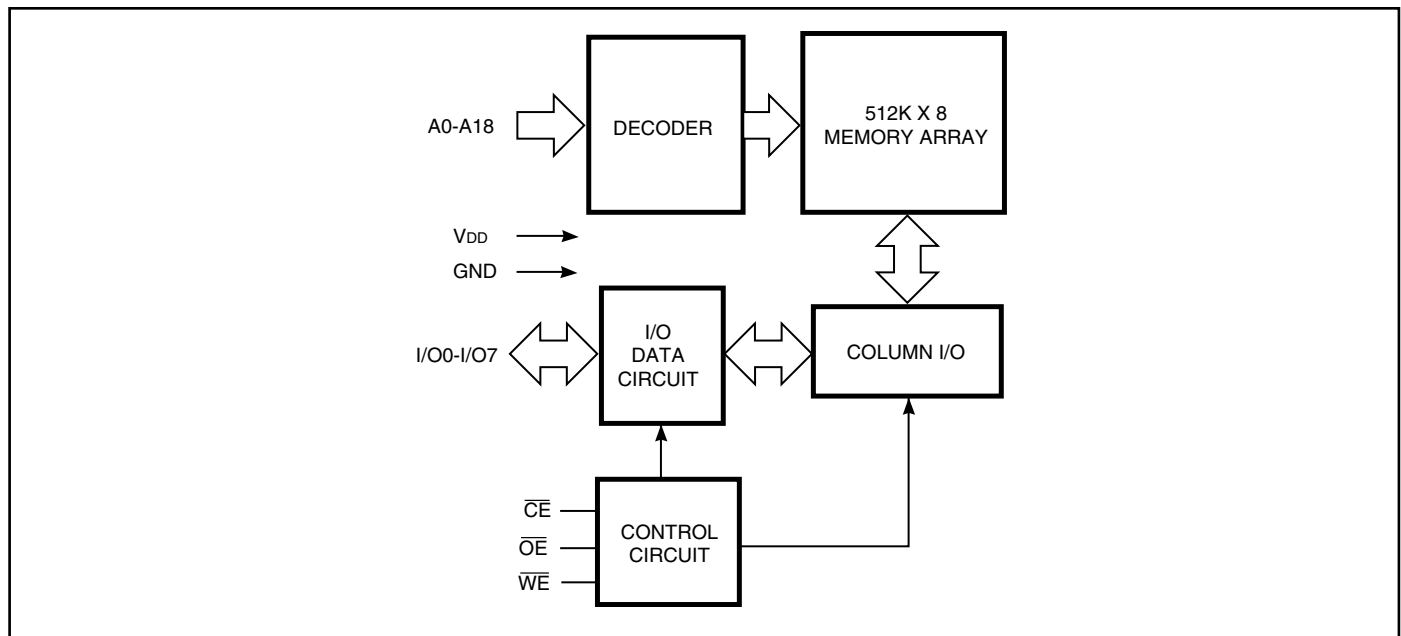
The *ISSI* IS62C5128BL and IS65C5128BL are high-speed, 4,194,304-bit static RAMs organized as 524,288 words by 8 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 45ns with low power consumption.

When  $\overline{CE}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs,  $\overline{CE}$  and  $\overline{OE}$ . The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IS62C5128BL and IS65C5128BL are packaged in the JEDEC standard 32-pin sTSOP-I, 32-pin SOP and 32-pin TSOP-II packages

### FUNCTIONAL BLOCK DIAGRAM



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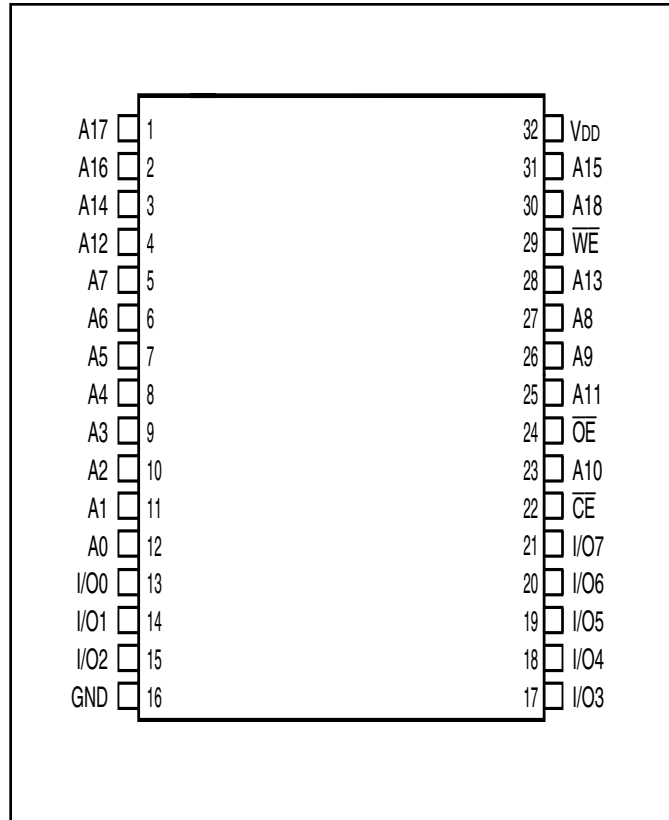
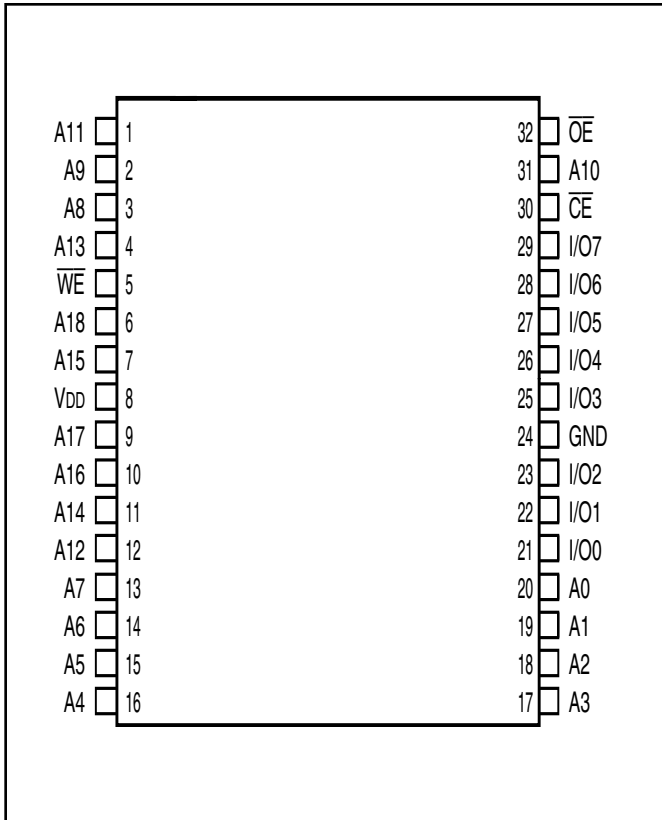
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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

**PIN CONFIGURATION**

**32-pin sTSOP (TYPE I)**

**32-pin SOP  
32-pin TSOP (TYPE II)**



**PIN DESCRIPTIONS**

A0-A18	Address Inputs
CE	Chip Enable 1 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O0-I/O7	I/O PIN
					V <sub>DD</sub> Current
Not Selected	X	H	X	High-Z	ISB1, ISB2
Output Disabled	H	L	H	High-Z	I <sub>CC1</sub> , I <sub>CC2</sub>
Read	H	L	L	D <sub>OUT</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>
Write	L	L	X	D <sub>IN</sub>	I <sub>CC1</sub> , I <sub>CC2</sub>

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.5	W
I <sub>OUT</sub>	DC Output Current (LOW)	20	mA

**Notes:**

- Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 5.0V.

**DC ELECTRICAL CHARACTERISTICS (Over Operating Range)**

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.4	—	V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 2.1 mA	—	0.4	V	
V <sub>IH</sub>	Input HIGH Voltage <sup>(1)</sup>		2.2	V <sub>DD</sub> + 0.5	V	
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V	
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	Com. Ind. Auto.	-1 -2 -5	1 2 5	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> Outputs Disabled	Com. Ind. Auto.	-1 -2 -5	1 2 5	μA

**Note:**

- V<sub>ILL</sub> (min) = -2.0V AC (pulse width <10 ns). Not 100% tested.  
V<sub>IHH</sub> (max) = V<sub>DD</sub> + 2.0V AC (pulse width <10 ns). Not 100% tested.

**OPERATING RANGE**

Range	Ambient Temperature	V <sub>DD</sub>	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	45
Industrial	-40°C to +85°C	5V ± 10%	45
Automotive	-40°C to +125°C	5V ± 10%	45

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	Test Conditions		-45 ns		Unit
				Min.	Max.	
I <sub>CC</sub>	Average operating Current	$\overline{CE} = V_{IL}, V_{DD} = \text{Max.}$ $I_{OUT} = 0 \text{ mA}, f = 0$	Com.	—	10	mA
			Ind.	—	10	
			Auto.	—	10	
I <sub>CC1</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	$V_{DD} = \text{Max.}, \overline{CE} = V_{IL}$ $I_{OUT} = 0 \text{ mA}, f = f_{MAX}$	Com.	—	15	mA
			Ind.	—	20	
			Auto.	—	25	
			typ. <sup>(2)</sup>		10	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	$V_{DD} = \text{Max.},$ $V_{IN} = V_{IH} \text{ or } V_{IL}, \overline{CE} \geq V_{IH},$ $f = 0$	Com.	—	1	mA
			Ind.	—	1.5	
			Auto.	—	2	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	$V_{DD} = \text{Max.},$ $\overline{CE} \geq V_{DD} - 0.2V,$ $V_{IN} \geq V_{DD} - 0.2V,$ or $V_{IN} \leq V_{SS} + 0.2V, f = 0$	Com.	—	10	μA
			Ind.	—	15	
			Auto.	—	35	
			typ.		4	

**Note:**

- At  $f = f_{MAX}$ , address and data inputs are cycling at the maximum frequency,  $f = 0$  means no input lines change.
- Typical values are measured at  $V_{DD} = 5V, T_A = 25^\circ\text{C}$  and not 100% tested.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)**

Symbol	Parameter	-45		Unit
		Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	45	—	ns
t <sub>AA</sub>	Address Access Time	—	45	ns
t <sub>OHA</sub>	Output Hold Time	3	—	ns
t <sub>ACE</sub>	$\overline{CE}$ Access Time	—	45	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	20	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	0	15	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	5	—	ns
t <sub>HZCE<sup>(2)</sup></sub>	$\overline{CE}$ to High-Z Output	0	15	ns
t <sub>LZCE<sup>(2)</sup></sub>	$\overline{CE}$ to Low-Z Output	5	—	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

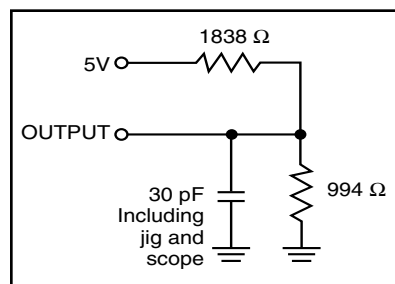
**AC TEST LOADS**


Figure 1

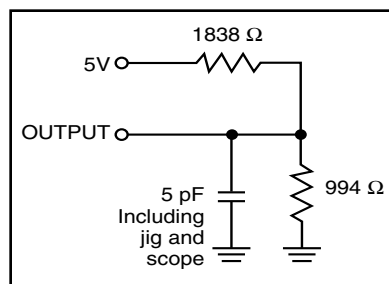
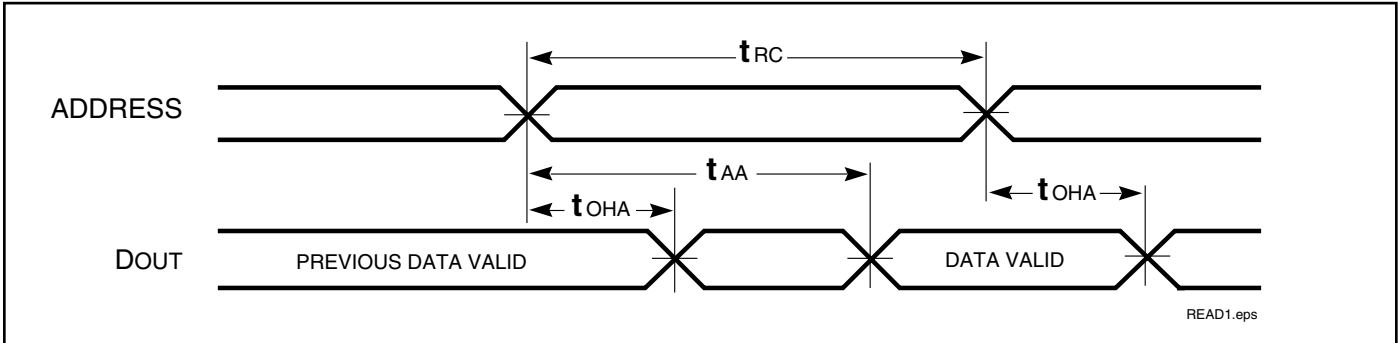
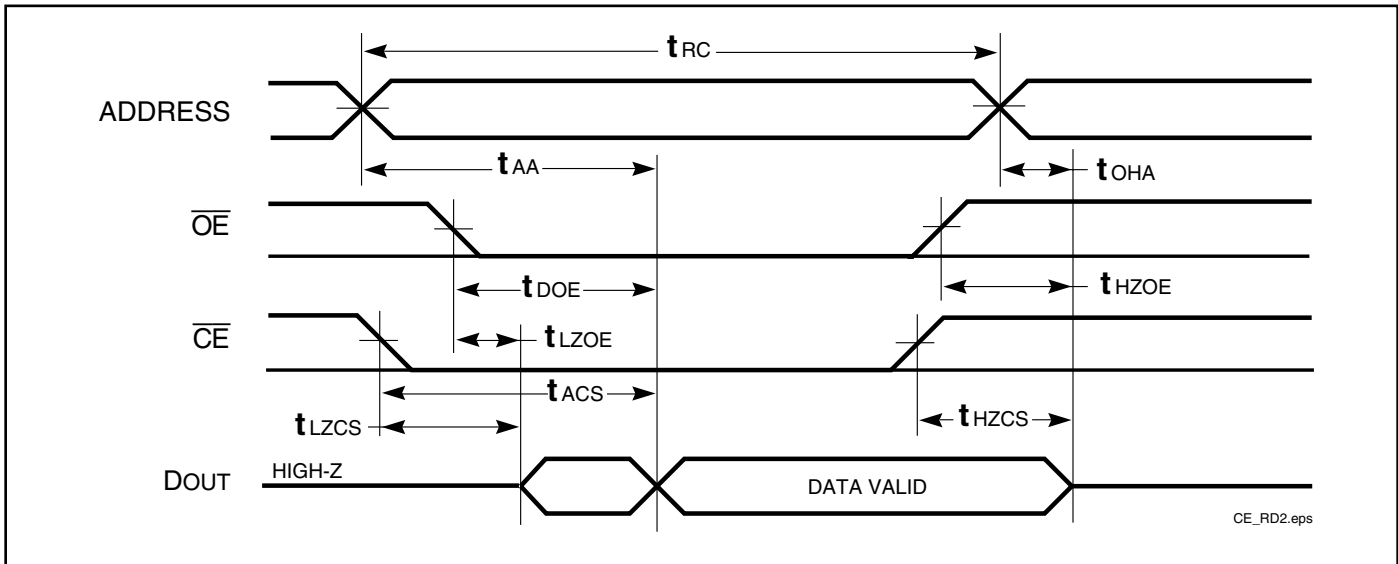


Figure 2

**AC WAVEFORMS**  
**READ CYCLE NO. 1<sup>(1,2)</sup>**



**READ CYCLE NO. 2<sup>(1,3)</sup>**



**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup> (Over Operating Range)**

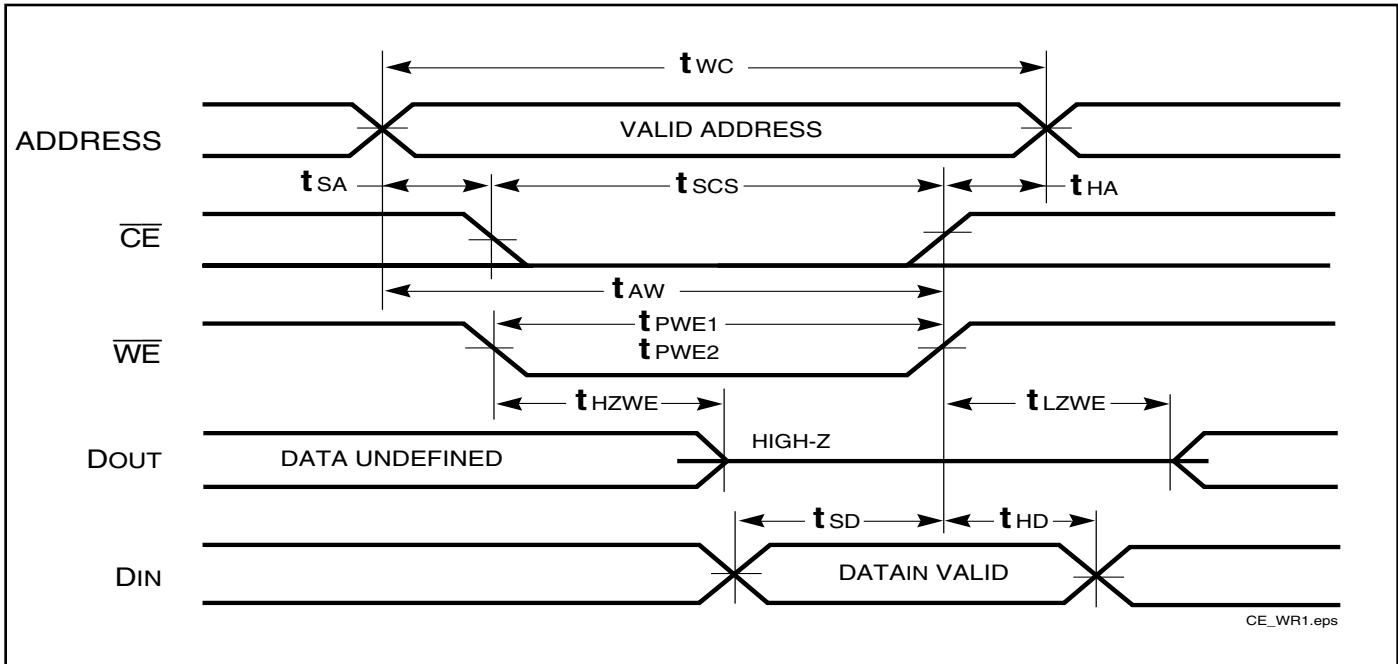
Symbol	Parameter	-45		Unit
		Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	45	—	ns
t <sub>SCE</sub>	$\overline{CE}$ to Write End	35	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	35	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	ns
t <sub>PWE1</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ =High)	35	—	ns
t <sub>PWE2</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ =Low)	35	—	ns
t <sub>SD</sub>	Data Setup to Write End	25	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	ns
t <sub>HZWE</sub> <sup>(2)</sup>	$\overline{WE}$ LOW to High-Z Output	—	15	ns
t <sub>LZWE</sub> <sup>(2)</sup>	$\overline{WE}$ HIGH to Low-Z Output	5	—	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

**AC WAVEFORMS**

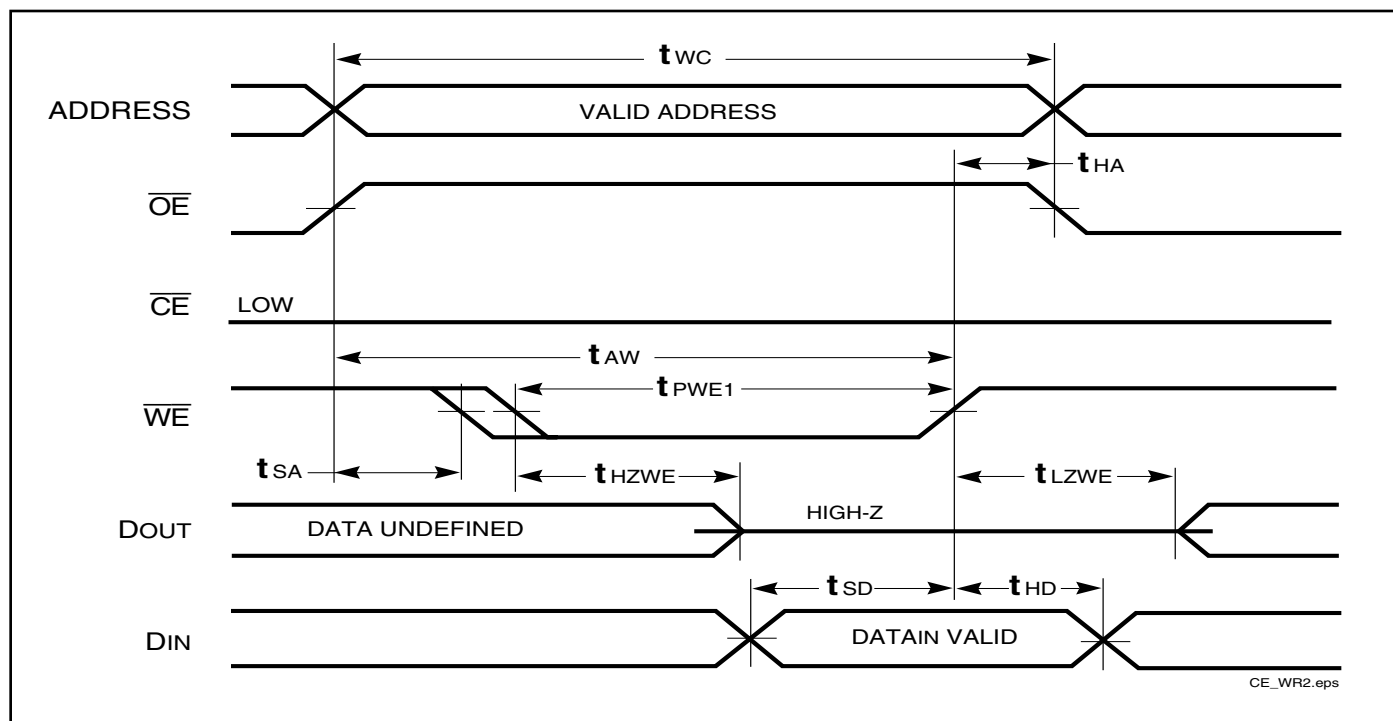
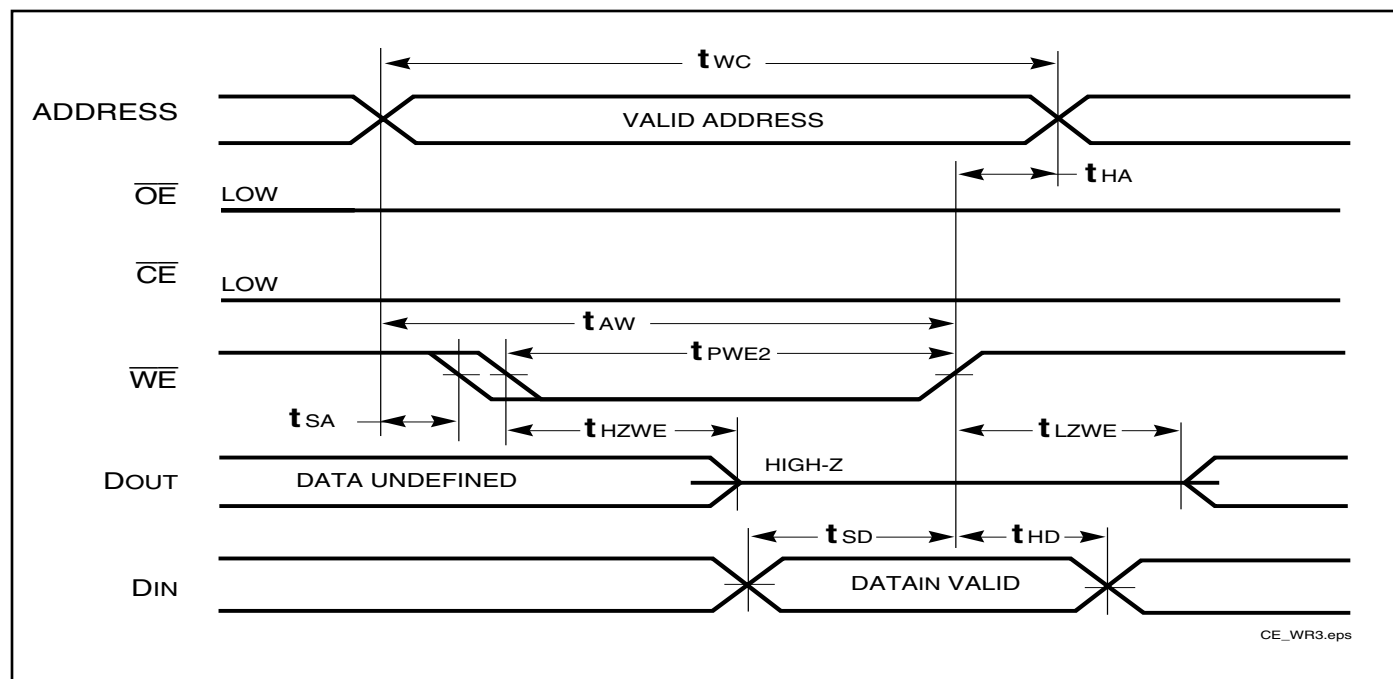
**WRITE CYCLE NO. 1 ( $\overline{WE}$  Controlled)<sup>(1,2)</sup>**



**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .



**WRITE CYCLE NO. 2** ( $\overline{OE}$  is HIGH During Write Cycle) <sup>(1,2)</sup>

**WRITE CYCLE NO. 3** ( $\overline{OE}$  is LOW During Write Cycle) <sup>(1)</sup>

**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .

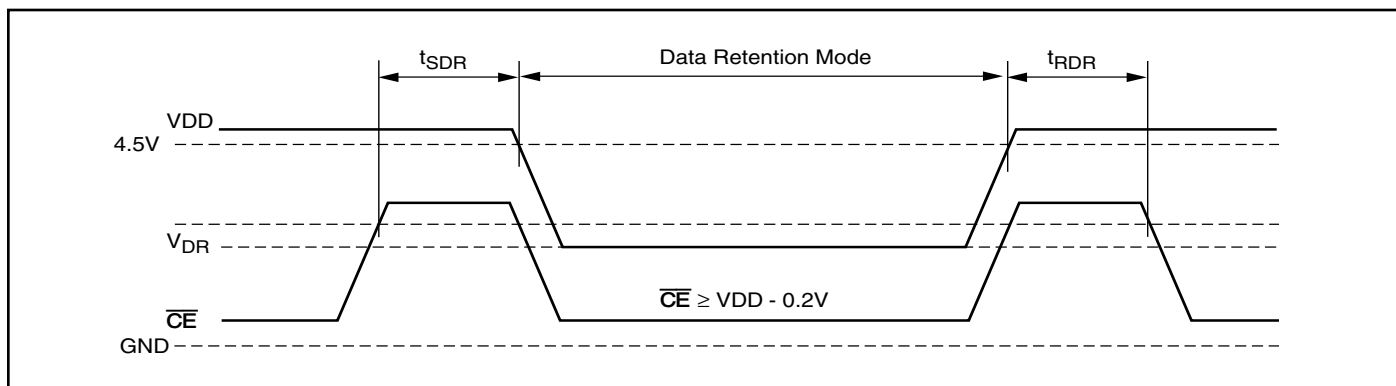
**DATA RETENTION SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Max.	Unit	
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform	2.0	5.5	V	
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	10	$\mu A$
		V <sub>IN</sub> $\geq V_{DD} - 0.2V$ , or V <sub>IN</sub> $\leq V_{SS} + 0.2V$	Ind.	—	15	
			Auto. typ. <sup>(1)</sup>	—	35	
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns	
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	ns	

**Note:**

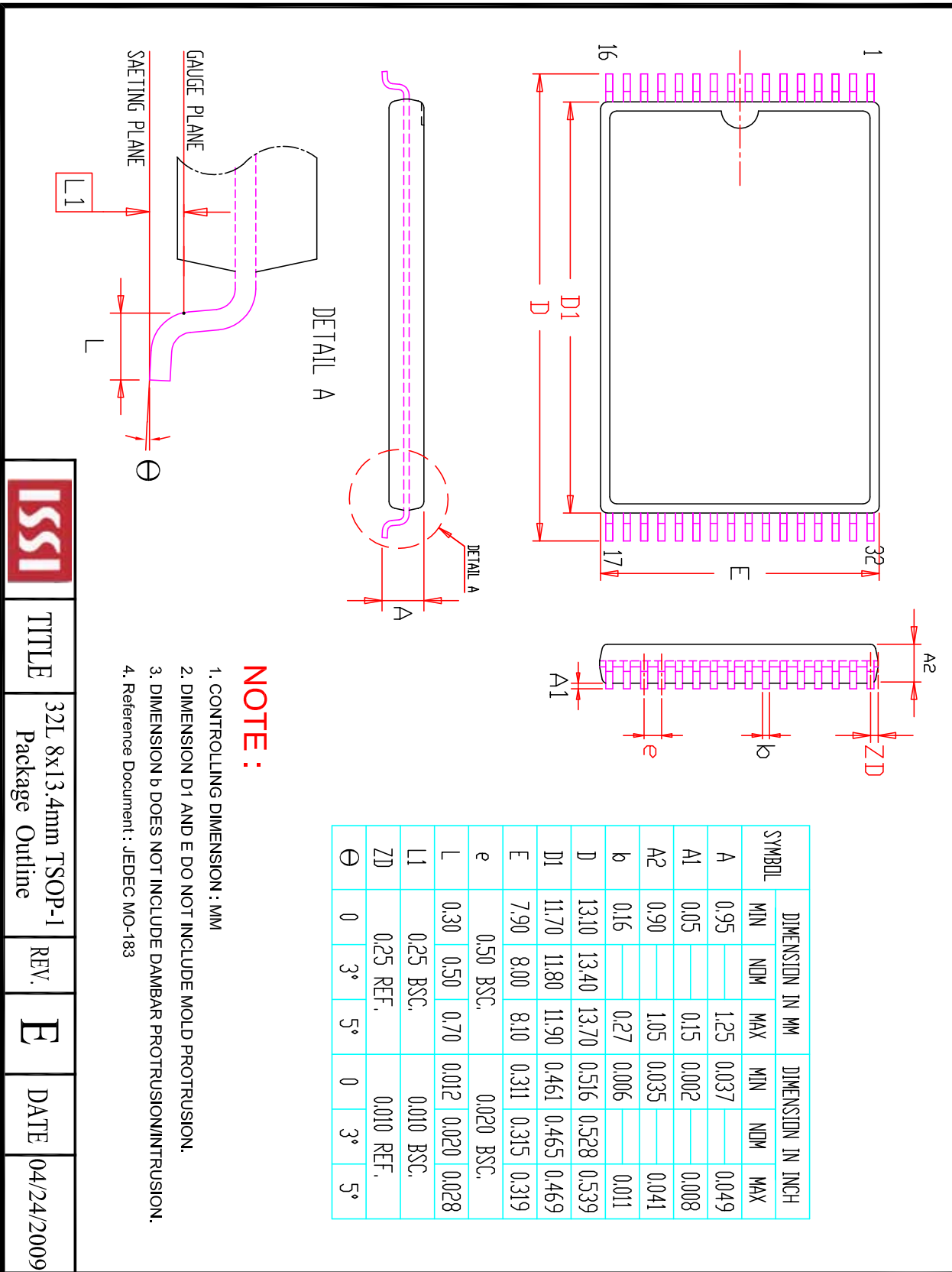
1. Typical Values are measured at V<sub>DD</sub> = 5V, T<sub>A</sub> = 25°C and not 100% tested.

**DATA RETENTION WAVEFORM ( $\overline{CE}$  Controlled)**



**ORDERING INFORMATION****Industrial Range: -40°C to +85°C**

<b>Speed (ns)</b>	<b>Order Part No.</b>	<b>Package</b>
45	IS62C5128BL-45QI	450-mil Plastic SOP
	IS62C5128BL-45QLI	450-mil Plastic SOP, Lead-free
	IS62C5128BL-45HI	32-pin STSOP-I
	IS62C5128BL-45HLI	32-pin STSOP-I, Lead-free
	IS62C5128BL-45TI	32-pin TSOP-II
	IS62C5128BL-45TLI	32-pin TSOP-II, Lead-free



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NDM	MAX	MIN	NDM	MAX
A	0.95		1.25	0.037		0.049
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°

**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183



TITLE

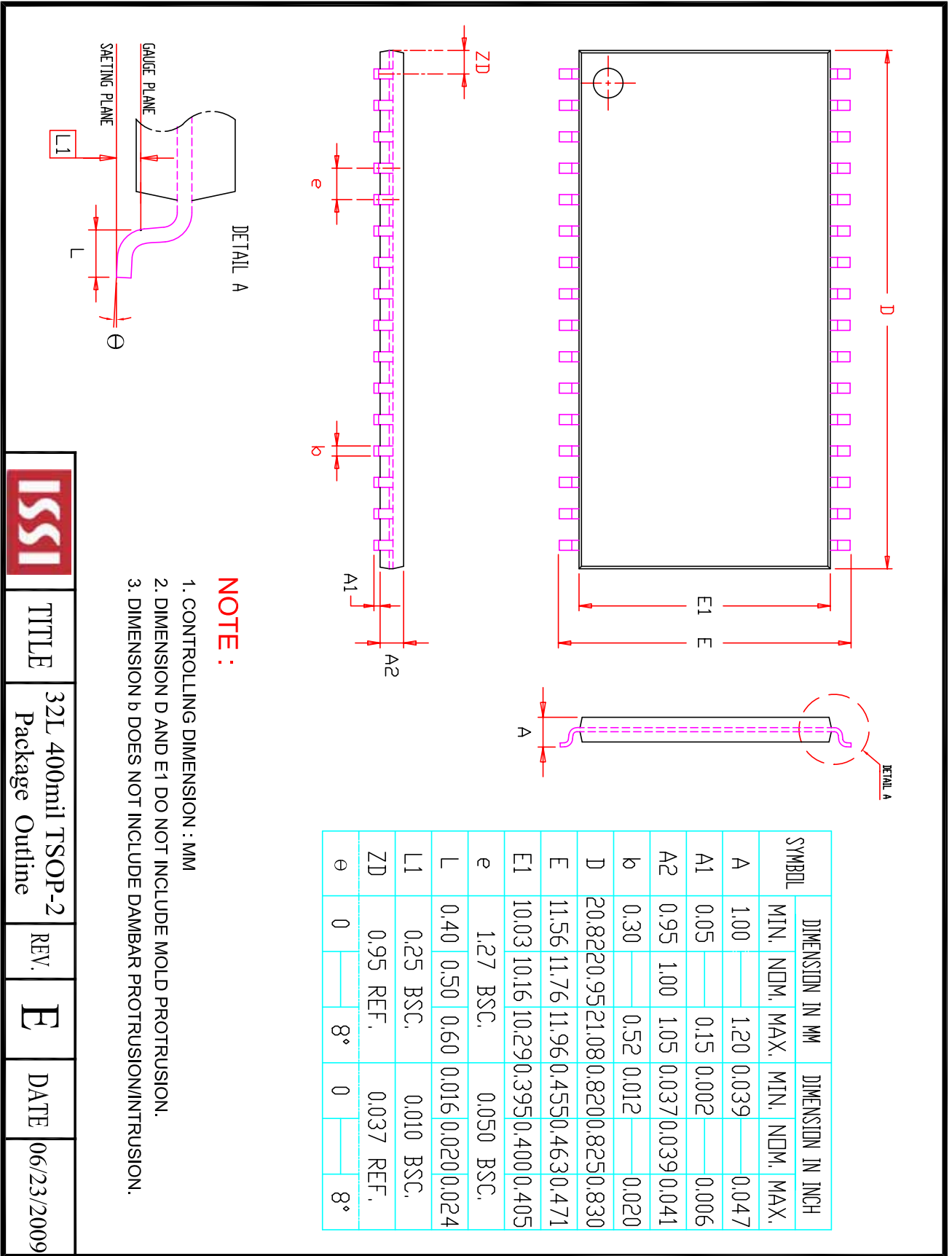
32L 8x13.4mm TSOP-1  
Package Outline

REV.

E

DATE

04/24/2009



TITLE

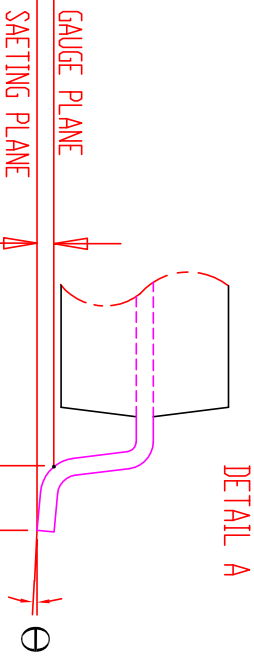
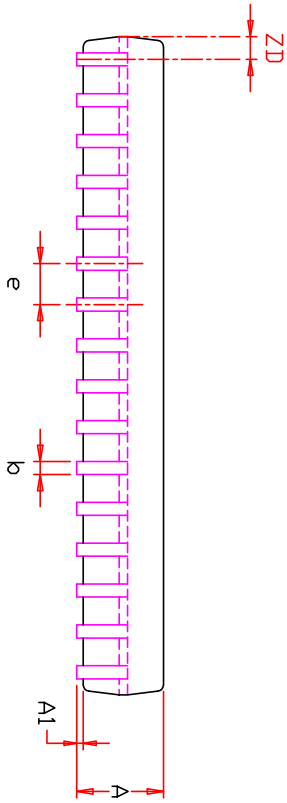
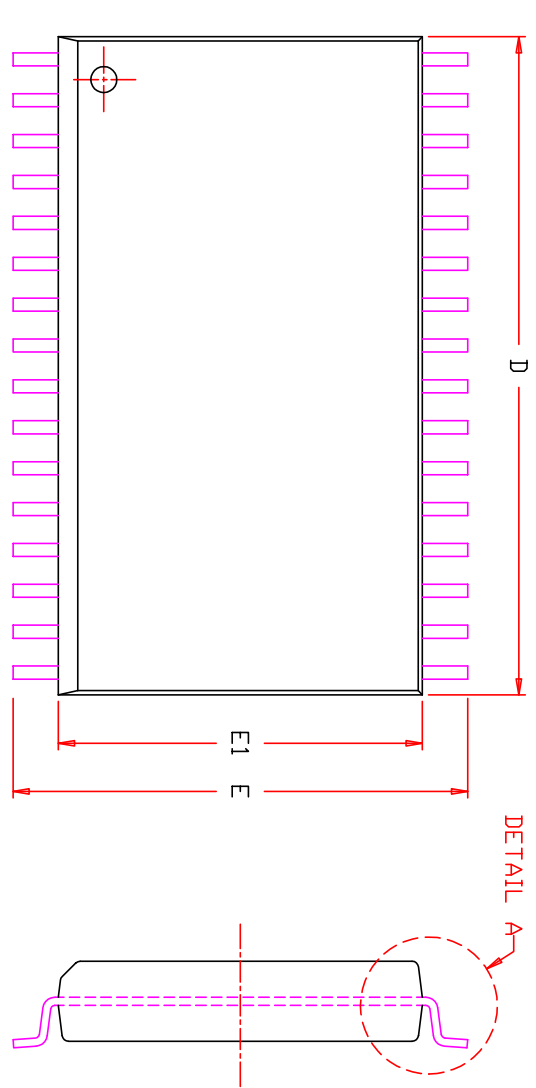
32L 400mil TSOP-2  
Package Outline

REV.

E

DATE

06/23/2009



**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.62		3.12	0.103		0.123
A1	0.05		0.30	0.002		0.012
b	0.33		0.51	0.013		0.020
D	20.24		20.750,797			0.817
E	13.79		14.450,543			0.569
E1	11.18		11.43	0.440		0.450
e	1.27	BSC.		0.050	BSC.	
L	0.38		1.27	0.015		0.050
L1	0.25	BSC.		0.010	BSC.	
ZD	0.725	REF.		0.029	REF.	
ϑ	0		8°	0		8°



TITLE

32L 450mil SOP  
Package Outline

REV.

D

DATE

04/20/2009

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