National Semiconductor

93L38
8-Bit Multiple Port Register

General Description

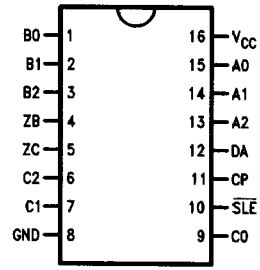
The 93L38 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously. The circuit uses TTL technology and is compatible with all TTL families.

Features

- Master/slave operation permitting simultaneous write/read without race problems
- Simultaneously read two bits and write one bit in any one of eight bit positions
- Readily expandable to allow for larger word sizes

Connection Diagram

Dual-In-Line Package



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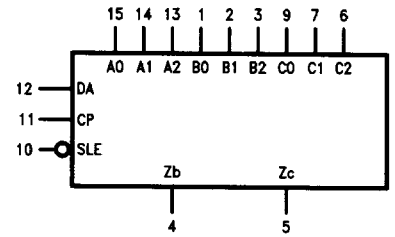
Order Number 93L38DMQB or 93L38FMQB
See NS Package Number J16A or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A2	Write Address Inputs
DA	Data Input
B0–B2	B Read Address Inputs
C0–C2	C Read Address Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{SLE}$	Slave Enable Input (Active LOW)
ZB	B Output
ZC	C Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L38 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_A to CP	30 22			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_A to CP	0 −4.0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to CP	0 0			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to CP	0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	40 30			ns

Electrical Characteristics over recommended operating free air temperature (unless othewise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all input grounded.

Switching Characteristics $V_{CC} = +5.0V, T_A = +25°C$ (See Section 1 for Test Waveforms and Output Load

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay B_n or C_n or Z_n		68 95	ns
t_{PLH} t_{PHL}	Propagation Delay D_A to Z_n		70 92	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Z_n		65 57	ns

Functional Description

The 93L38 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line (D_A) enters the selected master. This selection is accomplished by coding the three write input select lines (A0–A2) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs (B0–B2 and C0–C2). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ($\overline{SLE}$), the slave latches are continuously enabled.

The signals are available on the output pins (Z_B and Z_C). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

The method of parallel expansion is shown in *Figure A*. One 93L38 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.

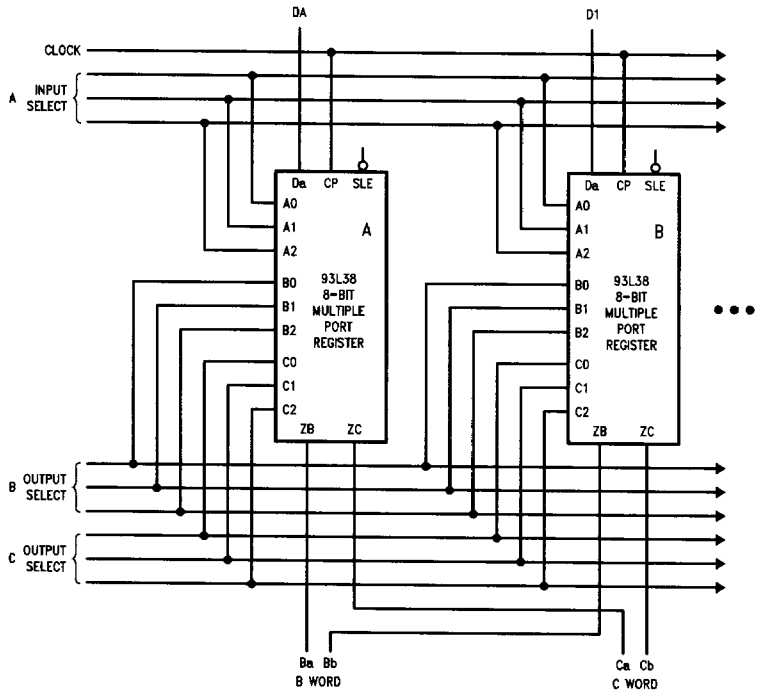

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FIGURE A. Parallel Expansion

Logic Diagram