



PRELIMINARY

CY7C1021V

64K x 16 Static RAM

Features

- 3.3V operation (3.0V–3.6V)
- High speed
 - $t_{AA} = 10/12/15$ ns
- CMOS for optimum speed/power
- Low active power (L version)
 - 540 mW (max.)
- Low CMOS Standby Power (L version)
 - 1.08 mW (max.)
- Automatic power-down when deselected
- Independent Control of Upper and Lower bits
- Available in 44-pin TSOP II and 400-mil SOJ

Functional Description

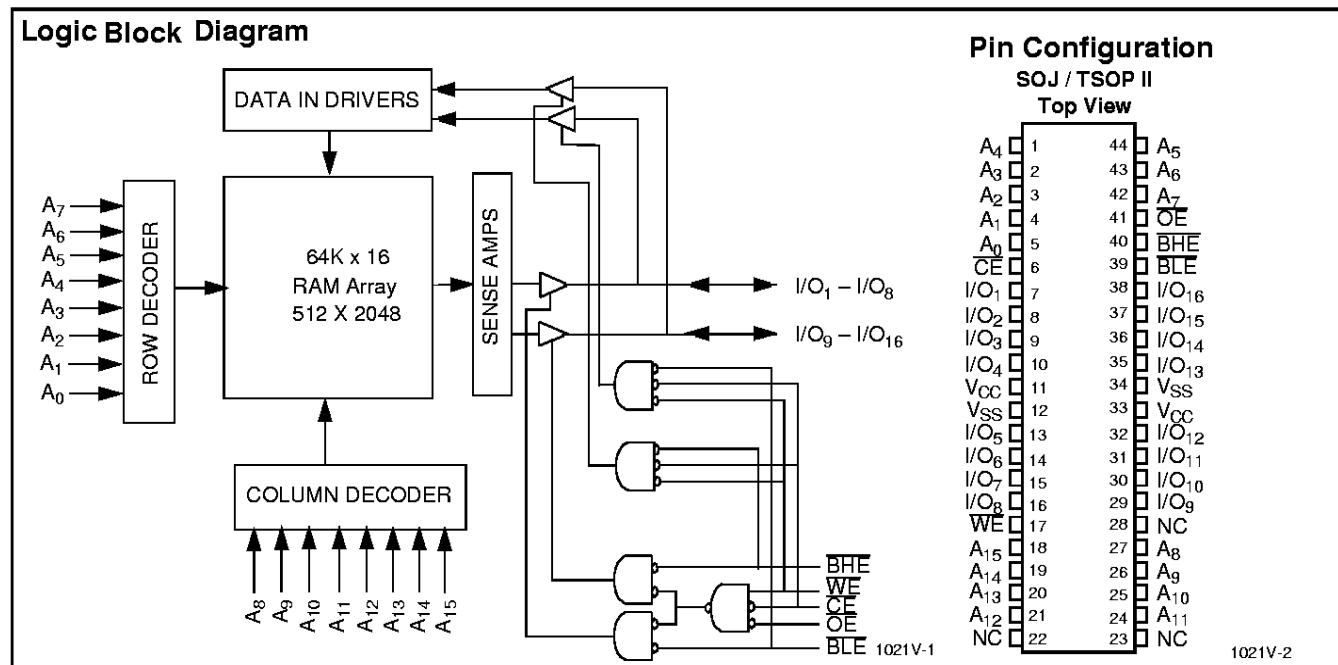
The CY7C1021V is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking chip enable (\overline{CE}) and write enable (\overline{WE}) inputs LOW. If byte low enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If byte high enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking chip enable (\overline{CE}) and output enable (\overline{OE}) LOW while forcing the write enable (\overline{WE}) HIGH. If byte low enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8 . If byte high enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_9 to I/O_{16} . See the truth table at the back of this datasheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1021V is available in 400-mil-wide SOJ and standard 44-pin TSOP Type II packages.



Selection Guide

		7C1021V-10	7C1021V-12	7C1021V-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	210	200	190
	L	160	150	140
Maximum CMOS Standby Current (mA)	Commercial	5	5	5
	L	0.300	0.300	0.300

Shaded areas contain advance information.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1].... -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State^[1]..... -0.5V to V_{CC} +0.5V

DC Input Voltage^[1]..... -0.5V to V_{CC} +0.5V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1021V-10		7C1021V-12		7C1021V-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3V	2.0	V _{CC} + 0.3V	2.0	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-2	+2	-2	+2	-2	+2	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		210		200		190	mA
			L	160		150		140	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		40		40		40	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f=0		5		5		5	mA
			L	300		300		300	μA

Shaded areas contain advance information.

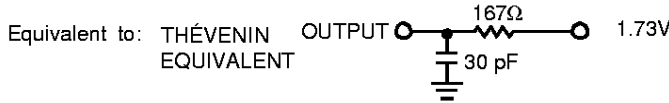
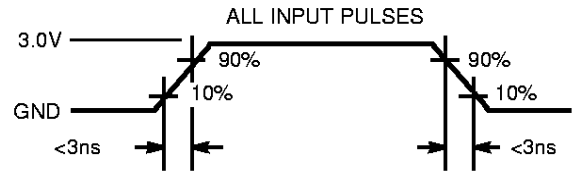
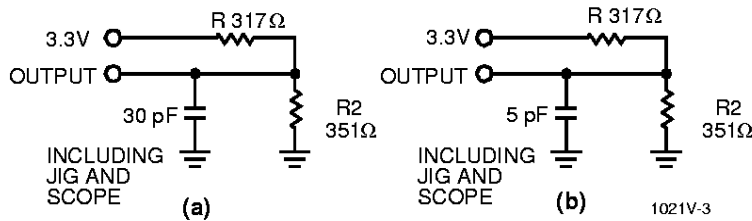
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	6	pF
C _{OUT}	Output Capacitance		8	pF

Notes:

- V_L (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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Switching Characteristics^[4] Over the Operating Range

Parameter	Description	7C1021V-10		7C1021V-12		7C1021V-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[5, 6]		5		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[5, 6]		5		6		7	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		12		12		15	ns
t_{DBE}	Byte enable to Data Valid		5		6		7	ns
t_{LZBE}	Byte enable to Low Z	0		0		0		ns
t_{HZBE}	Byte disable to High Z		5		6		7	ns
WRITE CYCLE^[7]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	8		8		10		ns
t_{AW}	Address Set-Up to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	7		8		10		ns
t_{SD}	Data Set-Up to Write End	5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[5, 6]		5		6		7	ns
t_{BW}	Byte enable to end of write	7		8		9		ns

Shaded areas contain advance information

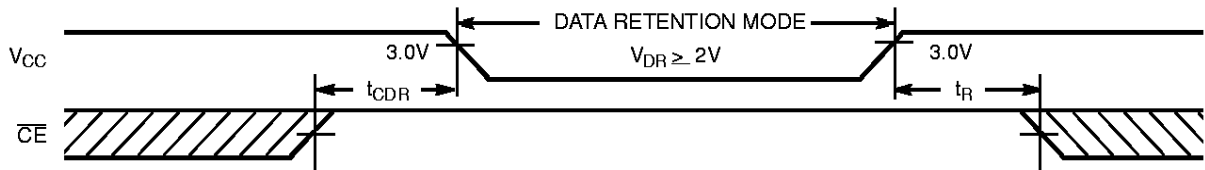
Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZOE} is less than t_{LZOE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and \overline{BHE} / \overline{BLE} LOW. \overline{CE} , \overline{WE} and \overline{BHE} / \overline{BLE} must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range (L version only)

Parameter	Description	Conditions ^[10]	Min.	Max.	Unit
V _{DR}	V _{CC} for Data Retention		2.0		V
I _{CCDR}	Data Retention Current	Com'l		100	μA
		V _{CC} = V _{DR} = 2.0V, CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V			
t _{CDR} ^[8]	Chip Deselect to Data Retention Time		0		ns
t _R ^[9]	Operation Recovery Time		t _{RC}		ns

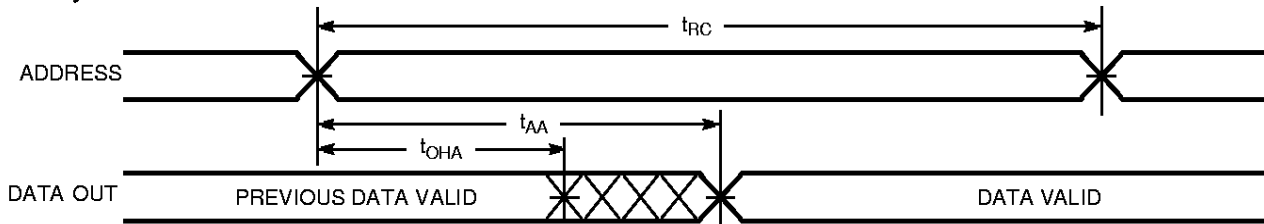
Data Retention Waveform



1021V-5

Switching Waveforms

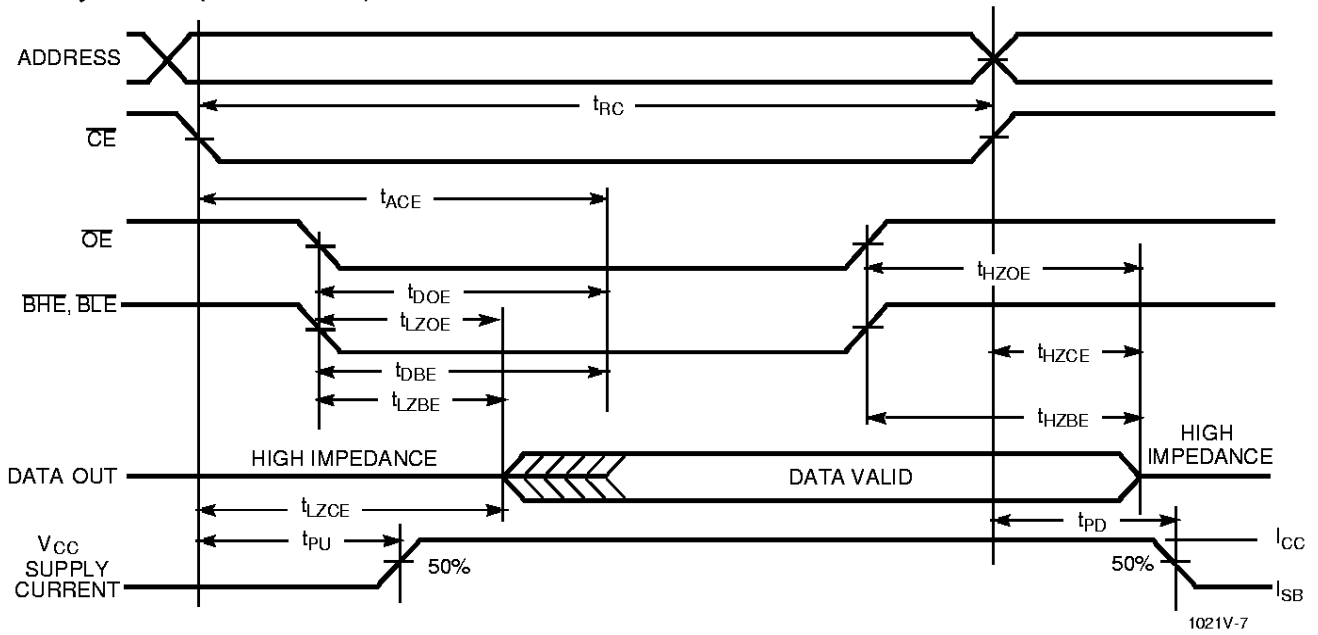
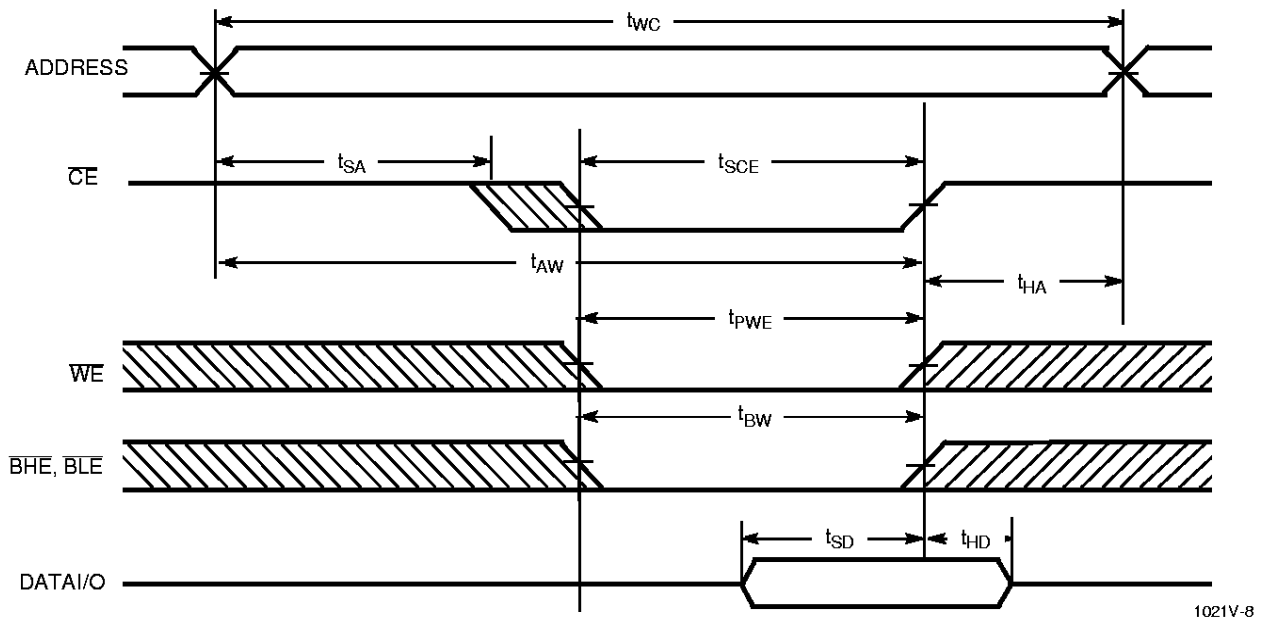
Read Cycle No.1 ^[11, 12]



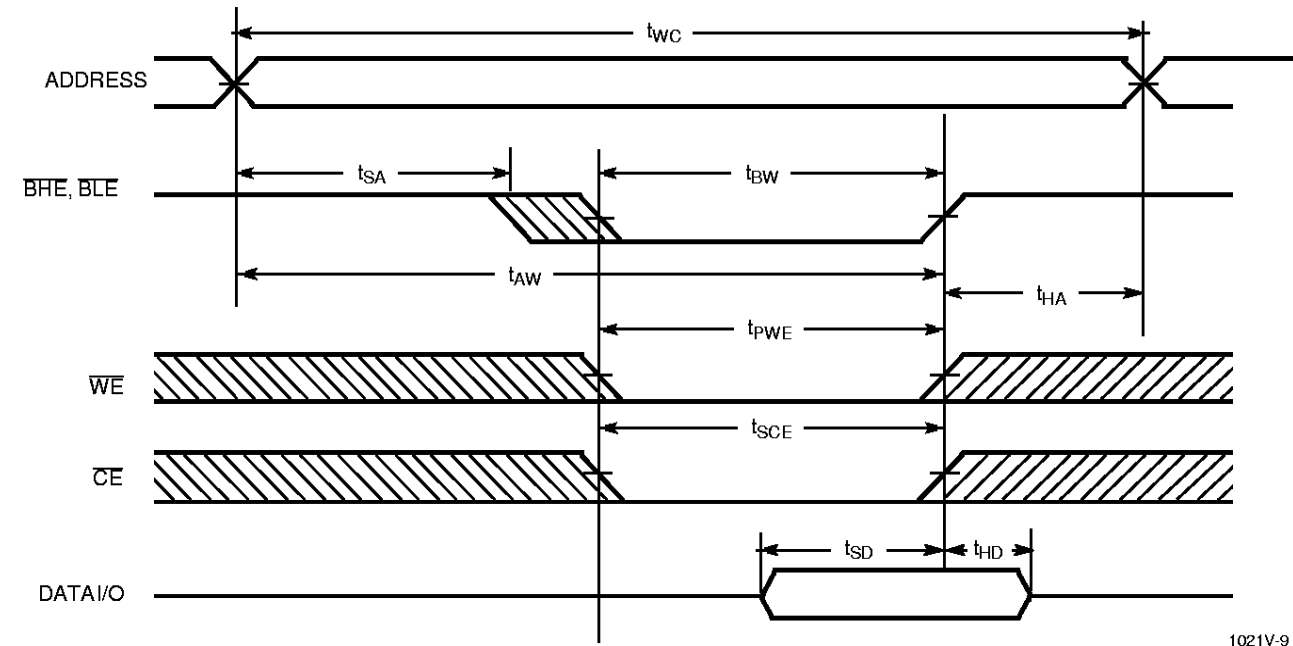
1021V-6

Notes:

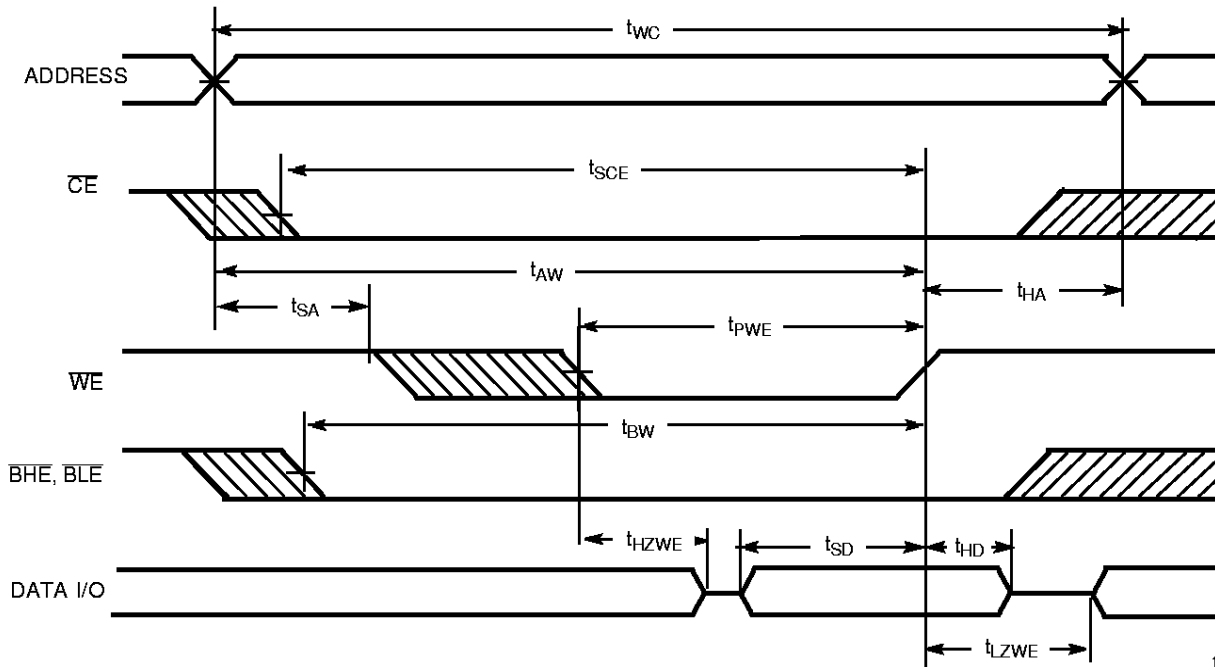
- 8. Tested initially and after any design or process changes that may affect these parameters.
- 9. t_r ≤ 3 ns for the -12 and -15 speeds. t_r ≤ 5 ns for the -20 and slower speeds.
- 10. No input may exceed V_{CC} + 0.5V.
- 11. Device is continuously selected. OE, CE, BHE and/or BHE = V_L
- 12. WE is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No.2 (\overline{OE} Controlled) [12, 13]

Write Cycle No. 1 (\overline{CE} Controlled) [14, 15]

Notes:

13. Address valid prior to or coincident with \overline{CE} transition LOW.
14. Data I/O is high impedance if \overline{OE} or BHE and/or BLE = V_{IH} .
15. If \overline{CE} goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 (BLE or BHE Controlled)


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Write Cycle No. 3 (WE Controlled, \overline{OE} LOW)


1021V-10



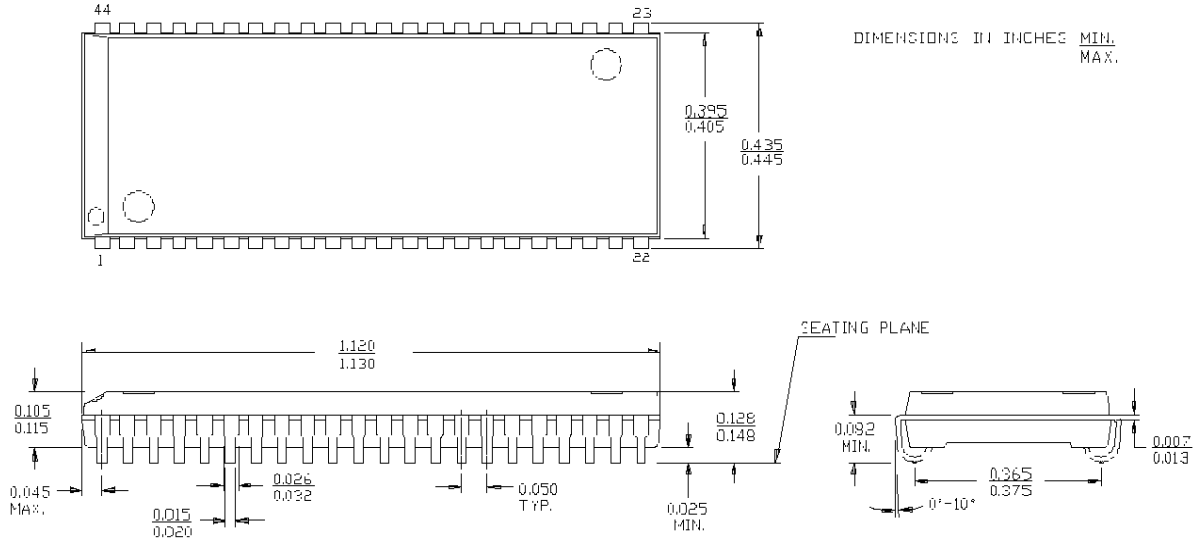
Truth Table

CE	OE	WE	BLE	BHE	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I _{SB})
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I _{CC})
			L	H	Data Out	High Z	Read - Lower bits only	Active (I _{CC})
			H	L	High Z	Data Out	Read - Upper bits only	Active (I _{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I _{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I _{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1021V33-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1021V33L-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1021V33-10ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C10201V33L-10ZC	Z44	44-Lead TSOP Type II	Commercial
12	CY7C1021V33-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1021V33L-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1021V33-12ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1021V33L-12ZC	Z44	44-Lead TSOP Type II	Commercial
15	CY7C1021V33-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1021V33L-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1021V33-15ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1021V33L-15ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1021V33-15ZI	Z44	44-Lead TSOP Type II	Industrial

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Package Diagrams
44-Lead (400-Mil) Molded SOJ V34

44-Pin TSOP II Z44
