FEATURES

- **Low Bias Current** ..... **5pA Max**
- **High Slew-Rate** ..... **±5V/μs Min**
- **Low Current Consumption** ..... **1.0mA Max**
- **High Gain** ..... **1000V/mV Min**
- **High Common-Mode Rejection** ..... **100dB Min**
- **Gain-Bandwidth Product** ..... **2.4MHz Typ**
- **Power Bandwidth** ..... **100kHz Typ**
- **Fast Overload Recovery Time** ..... **3.5μs Typ**
- **Low Harmonic Distortion** ..... **<0.01% at 5kHz**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99	PLASTIC 8-PIN	
250	OP43EJ	–	IND
750	OP43FJ	–	IND
500	OP43AJ*	–	MIL
1000	OP43BJ*	–	MIL
1500	–	OP43GP	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

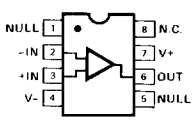
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

GENERAL DESCRIPTION

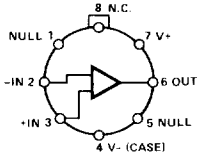
The OP-43 JFET operational amplifier is a high-speed version of the OP-41, featuring a slew rate of 6V/μs, gain-bandwidth product of 2.4MHz, and power bandwidth of 100kHz. Its high speed is achieved without compromising the low supply current, which is typically 750μA. The OP-43 has a bias current of only 5pA, and an open-loop gain of over 1 million. Common-mode rejection is an outstanding 115dB, far beyond that available with most FET op amps. The OP-43 is guaranteed stable for unity-gain circuits with ≤ 100pF loads. It is ideal for price-sensitive applications requiring low power-consumption combined with high speed and high accuracy.

The cascode input stage gives the OP-43 its exceptional CMR while improving CMR linearity with changing common-mode voltage. This input stage also stabilizes the bias current over the common-mode range. With its low power-consumption and a power-supply rejection ratio of 25μV/V, the OP-43 is an ideal choice for battery-operated systems. Using zener-zap trimming techniques, offset voltage is adjusted to below 250μV, thus eliminating the need for external nulling in many applications. In noninverting amplifier configurations, the outstanding CMR

PIN CONNECTIONS

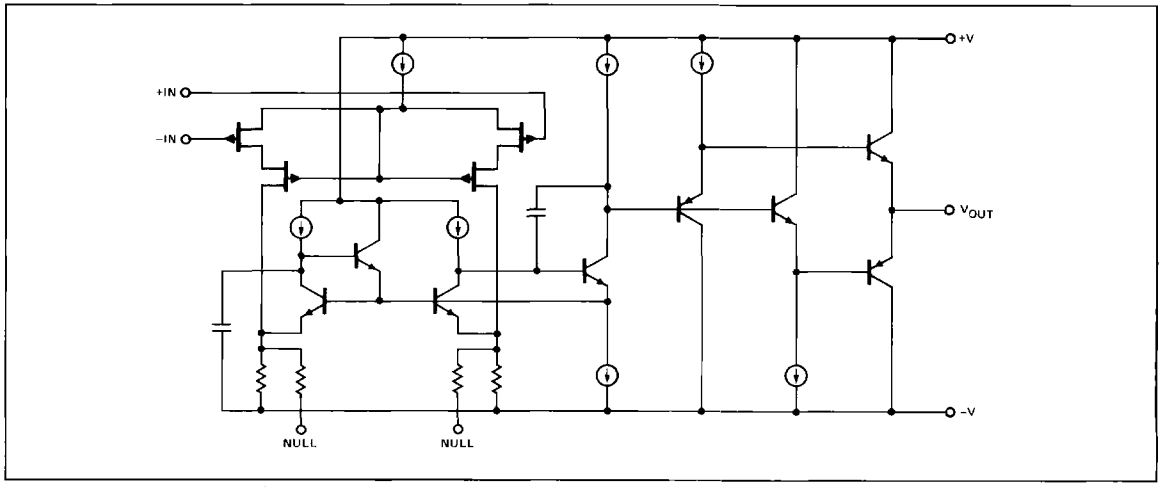


EPOXY MINI-DIP
(P-Suffix)



TO-99
(J-Suffix)

SIMPLIFIED SCHEMATIC



of the OP-43 insures linearity, while in high-gain configurations, linearity and accuracy are insured by the OP-43's guaranteed gain of 1 million into a 2kΩ load.

The OP-43 exhibits rapid recovery from signal overload. Following saturation at the positive supply, the output recovers in only 3.5μs. Recovery from saturation at the negative supply is even faster.

The combination of low offset and drift, low power, low bias current, high speed, and high gain plus the superior CMR and PSRR performance of the OP-43, makes the device suitable for a wide range of demanding applications including DAC output amplifiers. Where low power-consumption is required in battery-powered or portable instrumentation, the OP-43 permits high-gain and high-accuracy amplification along with high-speed. The low and stable bias current, combined with its high input impedance, makes it an excellent choice for interfacing with high impedance transducers or low-level current sources.

In applications where speed is not essential, and superb capacitive load driving capabilities are required, the OP-41 is recommended.

The standard "741" pin-out allows existing JFET designs and low-power bipolar designs, to be upgraded by direct replacement with the OP-43.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Input Voltage (Note 1) ..... ±18V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 1) ..... ±18V
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-43A, B (J) ..... –55°C to +125°C
OP-43E, F (J) ..... –25°C to +85°C
OP-43G (P) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec.) ..... +300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	θ_{JA} (NOTE 3)	θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES:
1. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
3. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-43A/E MIN	OP-43A/E TYP	OP-43A/E MAX	OP-43B/F MIN	OP-43B/F TYP	OP-43B/F MAX	OP-43G MIN	OP-43G TYP	OP-43G MAX	UNITS
Offset Voltage	V_{OS}	OP-43 E/F/G	—	200	250	—	400	750	—	500	1500	μV
		OP-43 A/B	—	200	500	—	400	1000	—	—	—	
Offset Current	I_{OS}	(Note 1)	—	0.04	1	—	0.05	2	—	0.05	5	pA
Bias Current	I_B	(Note 1)	—	3.0	5	—	3.5	10	—	3.5	25	pA
Open-Loop Voltage Gain	A_{VO}	R_L = 2kΩ, V_O = ±10V	1000	5000	—	500	4000	—	300	3000	—	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.3	±12.6	—	±12.0	±12.6	—	±11.0	±12.6	—	V
Supply Current	I_{SY}	V_O = 0V	—	0.75	1.0	—	0.75	1.2	—	0.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	±11.0	+15.0 −11.5	—	±11.0	+15.0 −11.5	—	±11.0	+15.0 −11.5	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±18V		5	25	—	10	80	—	10	80	μV/V
Noise Voltage Density Referred to Input	e_n	1kHz	—	32	—	—	32	—	—	32	—	$nV/\sqrt{Hz}$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±12	+20 −18	±36	±12	+20 −18	±36	±6	+20 −18	±36	mA
Slew Rate	SR		5	6	—	5	6	—	5	6	—	V/μs
Gain Bandwidth	GBW		—	2.4	—	—	2.4	—	—	2.4	—	MHz
Power Bandwidth	BW_P		—	100	—	—	100	—	—	100	—	kHz

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-43A/E MIN	OP-43A/E TYP	OP-43A/E MAX	OP-43B/F MIN	OP-43B/F TYP	OP-43B/F MAX	OP-43G MIN	OP-43G TYP	OP-43G MAX	UNITS
Settling Time	t_s	10V Step $A_V = -1$ to 0.1% to 0.01%	— —	2.5 5	— —	— —	2.5 5	— —	— —	2.5 5	— —	µs
Overload Recovery	t_{or}	Positive Going Negative Going	— —	1 3.5	— —	— —	1 3.5	— —	— —	1 3.5	— —	µs
Capacitive Load Stability	C_L	$A_V = +1$ (Note 3)	100	250	—	100	250	—	100	250	—	pF
Open-Loop Output Resistance	R_O		—	150	—	—	150	—	—	150	—	Ω
Supply Voltage	V_S	Rated Performance Derated Performance	— ±4.5	±15 —	— ±18	— ±4.5	±15 —	— ±18	— ±4.5	±15 —	— ±18	V

NOTES:
1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -55°C/+125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-43A MIN	OP-43A TYP	OP-43A MAX	OP-43B MIN	OP-43B TYP	OP-43B MAX	UNITS
Offset Voltage	V_{OS}		—	400	1000	—	600	2000	µV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	2.5	5	—	3.5	10	µV/°C
Offset Current	I_{OS}	(Note 1)	—	40	1000	—	50	2000	pA
Bias Current	I_B	(Note 1)	—	4000	7500	—	4500	15000	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.0	±12.5	—	±11.5	±12.5	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	0.75	1.2	—	0.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	±11.0	+15.0 −11.5	—	±11.0	+15.0 −11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	105	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	40	—	10	100	µV/V
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±6	+12 −17	±36	±6	+12 −17	±36	mA
Slew Rate	SR		5	6	—	5	6	—	V/µs
Gain Bandwidth	GBW		—	2.4	—	—	2.4	—	MHz
Power Bandwidth	BW_P		—	100	—	—	100	—	kHz
Capacitive Load Stability	C_L	$A_V = +1$ (Note 3)	100	250	—	100	250	—	pF

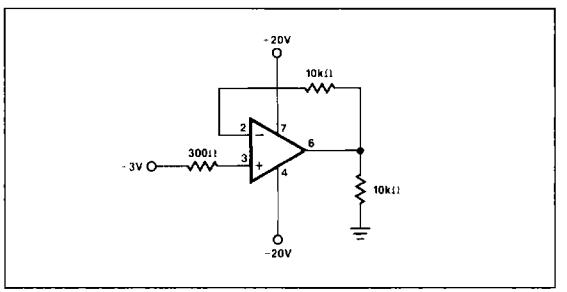
NOTES:
1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -25°C/+85°C$ for E/F grades and $-40°C/+85°C$ for G grade, unless otherwise noted.

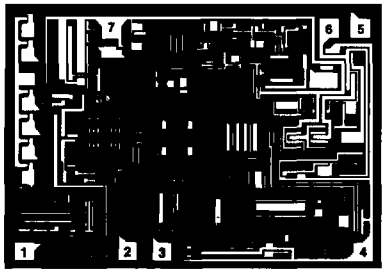
			OP-43E			OP-43F			OP-43G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	V_{OS}		—	250	750	—	500	1750	—	500	2000	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	3.5	8	—	7.5	—	—	7.5	—	μV/°C
Offset Current	I_{OS}	(Note 1)	—	5	100	—	10	200	—	20	—	pA
Bias Current	I_B	(Note 1)	—	240	500	—	300	1000	—	100	500	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	300	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.0	±12.6	—	±11.5	±12.5	—	±11.0	±12.6	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	0.75	1.2	—	0.75	1.2	—	0.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	±11.0	+15.0 -11.5	—	±11.0	+15.0 -11.5	—	±11.0	+15.0 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	110	—	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	40	—	10	100	—	10	100	μV/V
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±6	+16 -18	±36	±6	+16 -18	±36	±6	+20 -18	±36	mA
Slew Rate	SR		5	6	—	5	6	—	5	6	—	V/μs
Gain Bandwidth	GBW		—	2.4	—	—	2.4	—	—	2.4	—	MHz
Power Bandwidth	BW_P		—	100	—	—	100	—	—	100	—	kHz
Capacitive Load Stability	C_L	$A_V = +1$ (Note 3)	100	250	—	100	250	—	100	250	—	pF

NOTES:
1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.103 × 0.074 inch, 7622 sq. mils
(2.62 × 1.88mm, 4.92 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

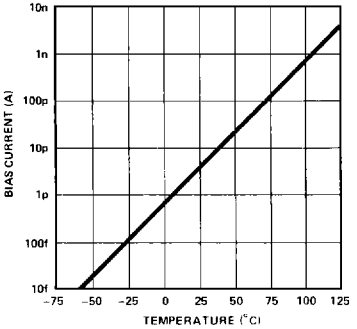
PARAMETER	SYMBOL	CONDITIONS	OP-43N LIMIT	UNITS
Offset Voltage	V_{OS}		750	μV MAX
Bias Current	I_B	(Note 1)	20	pA MAX
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12	V MIN
Supply Current	I_{SY}	$V_O = 0V$	1.2	mA MAX
Input Voltage Range	IVR	(Note 2)	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	80	μV/V MAX
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±12	mA MIN
Slew Rate	SR		5	V/μs MIN
Capacitive Load Stability	C_L	$A_V = +1$ (Note 3)	100	pF MIN

NOTES:
1. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

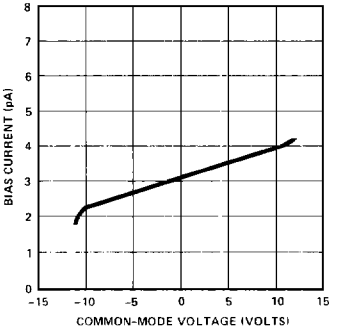
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

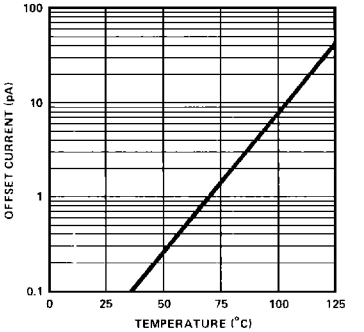
BIAS CURRENT vs TEMPERATURE



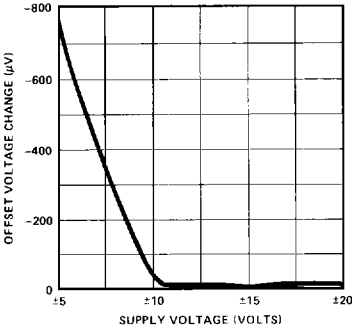
BIAS CURRENT vs COMMON-MODE VOLTAGE



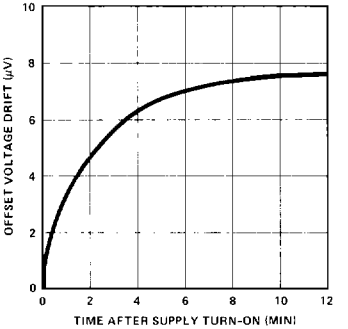
OFFSET CURRENT vs TEMPERATURE



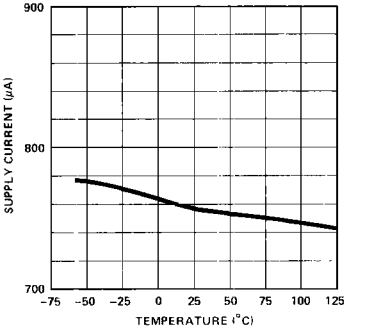
OFFSET VOLTAGE vs SUPPLY VOLTAGE



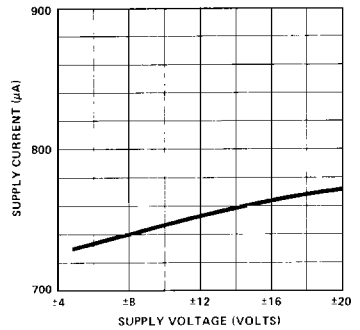
WARM-UP DRIFT vs TIME



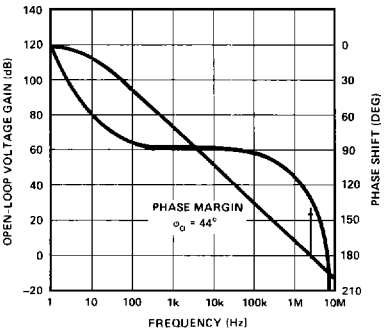
SUPPLY CURRENT vs TEMPERATURE



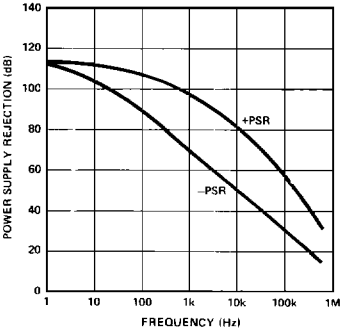
SUPPLY CURRENT vs SUPPLY VOLTAGE



OPEN-LOOP GAIN AND PHASE vs FREQUENCY

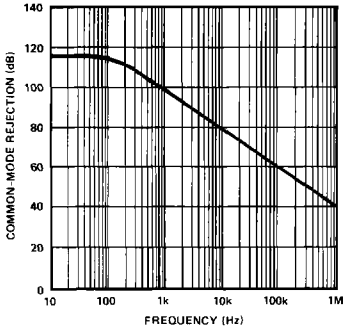


POWER SUPPLY REJECTION vs FREQUENCY

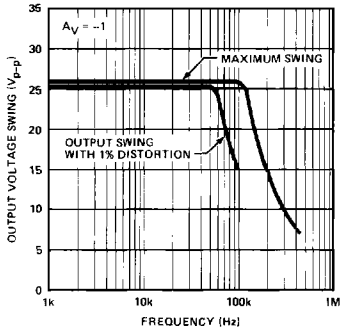


TYPICAL PERFORMANCE CHARACTERISTICS

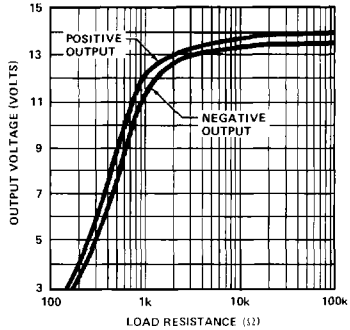
COMMON-MODE REJECTION vs FREQUENCY



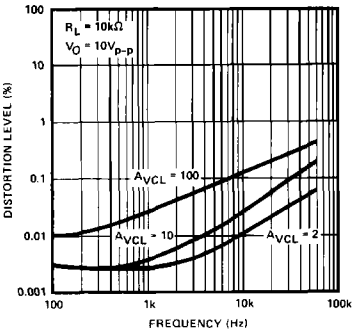
MAXIMUM OUTPUT SWING vs FREQUENCY



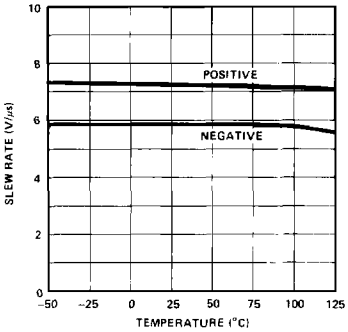
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



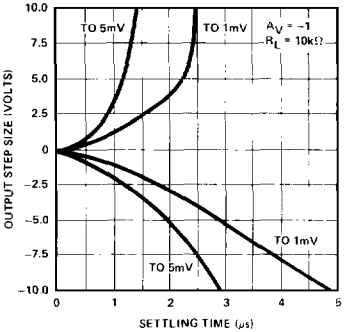
TOTAL HARMONIC DISTORTION vs FREQUENCY



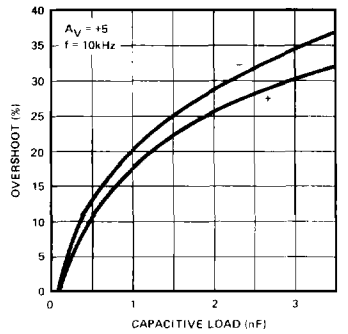
SLEW RATE vs TEMPERATURE



SETTLING TIME vs OUTPUT STEP SIZE



SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



APPLICATIONS INFORMATION

TYPICAL AC PERFORMANCE

The OP-43 is a high-speed op amp featuring a symmetrical 5V/μs minimum slew rate and a 2.4MHz gain-bandwidth product. It is guaranteed stable with a 100pF load over temperature. Typically, the OP-43 is capable of driving several hundred pF.

Figure 1 shows the OP-43's rapid overload recovery time. This is the time required for the output to return to its linear operating region, after the output saturates at each supply. Many op amps may be used in a system, and following a system overload, timing delays are necessary to allow all devices to stabilize. The fast recovery time of the OP-43 allows these delays to be much shorter, thus speeding overall system recovery. The photo also shows the well-controlled linear characteristics of the amplifier and its freedom from oscillations.

Figure 2 shows the small-signal transient response of the OP-43 with a gain of +1. When operated at higher closed-loop gains, transient response is further improved. In a gain of +5, there is essentially no overshoot with a 100pF load, and even with a 1000pF load, overshoot is minimal (Figure 3).

FIGURE 1: Overload Recovery Time at A_{VCL} = 10

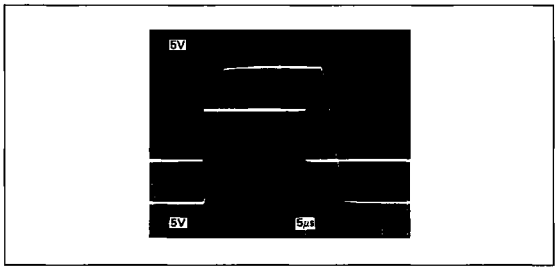


FIGURE 2: Small-Signal Transient Response at A_{VCL} = −1

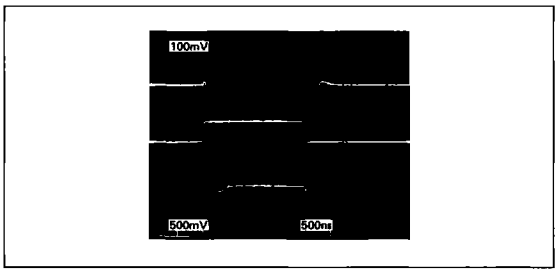
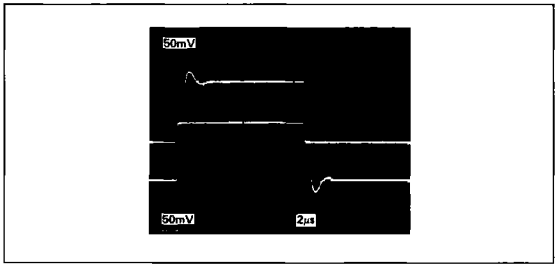


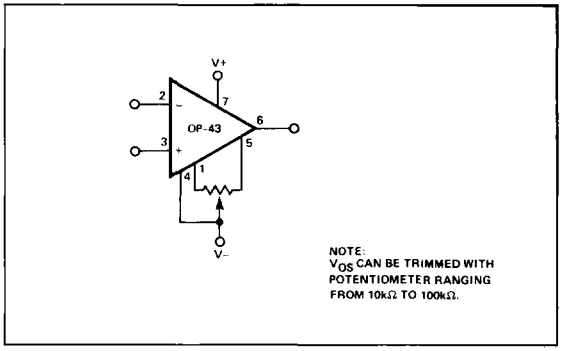
FIGURE 3: Small-Signal Transient Response at A_{VCL} = 5 with 1000pF Load



OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted by a potentiometer of 10kΩ to 100kΩ resistance. This potentiometer should be connected between pins 1 and 5 with the wiper connected to the V− supply. (See Figure 4.) Nulling V_{OS} will change TCV_{OS} by no more than 5μV/°C per millivolt of V_{OS} change.

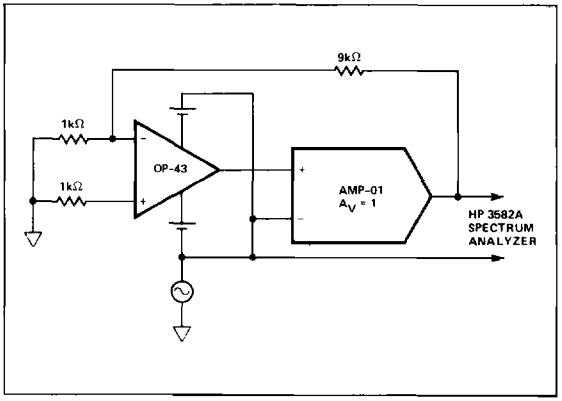
FIGURE 4: Input Offset Voltage Nulling



CMR MEASUREMENT METHODS

Two separate methods are used to measure the CMR. The first method is used over the range of 10Hz to 20kHz. This method grounds the input circuitry and applies the common-mode signal to the remainder of the op amp (Figure 5).

FIGURE 5: Circuit Used To Measure CMR From 10Hz to 29kHz



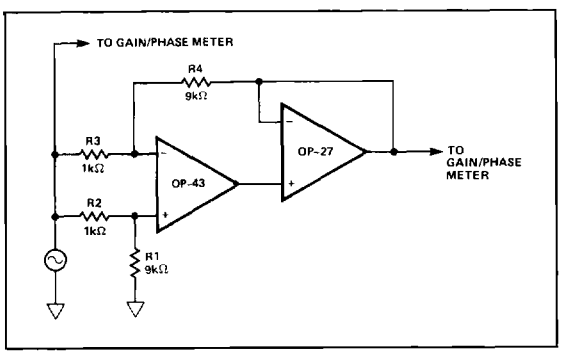
The AMP-01 eliminates loading on the output stage. This assures that the OP-41 output is not required to deliver current into the feedback circuit. The effects of the DUT open-loop gain changing with frequency are therefore significantly reduced. The circuit does not require tight resistor-matching. DC data sheet limits may be verified using this method. Circuit accuracy is dependent on the high CMR of the AMP-01.

An alternate circuit may be used to make high-frequency measurements from 2kHz to 500kHz (Figure 6). The 2kHz to 20kHz data overlap can be used to verify the accuracy of the respective test methods.

This method drives the input stage with the test signal and requires an accurate ratio of resistors, R4/R3 = R1/R2. To measure CMR to 100dB requires ratio matching to better than 10ppm. For this reason, it is not practical to use the second method at low frequencies where CMR is greater than 80—100dB.

Connecting the DUT directly to R4 can cause measurement errors. If the DUT is not buffered with a broadband low-output-impedance amplifier, the frequency-dependent output impedance of the DUT, in series with R4, rapidly unbalances the resistor ratios. This causes frequency dependent errors. The OP-27 provides good performance over the range of frequencies used.

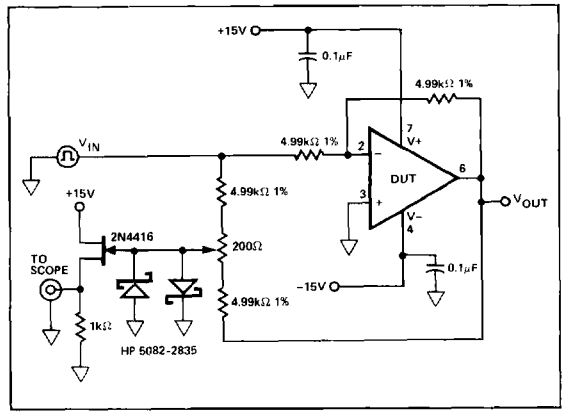
FIGURE 6: Circuit Used To Measure CMR From 2kHz to 500kHz



SETTLING-TIME MEASUREMENT

Figure 7 is the test circuit used to measure the settling time. This circuit uses the "false sum-node" technique. When the system is initially set up, the 200Ω pot is adjusted until the DC output voltage to the scope is unchanged when the input is changed from +10V to −10V. The 2N4416 FET buffer isolates the sum node from the scope probe load-capacitance. The pulse generator must be properly terminated and have ringing below the expected error signal. (2.5mV in a 5V pulse for 0.1% overshoot measurement.)

FIGURE 7: Settling-Time Test Circuit



GUARDING AND SHIELDING

High input impedances and low currents present a host of problems in a real circuit design. Unshielded high-impedance lines act as antennae, picking up line-frequency hum (50 or 60Hz) and noise from radio and television transmissions, as well as local radar installations and airports. Low currents are easily overwhelmed by leakage currents of 100pA or more existing on a clean PC board. To avoid these problems, careful attention must be paid to the physical design and layout of the circuit.

Hum and RF pickup are minimized by keeping all high-impedance leads inside shielded enclosures. Feedback and input resistors should be kept as close to the device as possible. A separate, shielded power supply should be used to prevent line noise from being retransmitted inside the shielded enclosure. Shielded cables should be used for all connections to devices outside the enclosure. These cables should be held rigid to prevent capacitively-coupled noise originating from mechanical flexing and vibration. The choice of exactly what type of cable to use depends heavily on the frequency range of interest. For high precision work, two-wire twisted-pair cable with an additional shield gives the best protection against interference and noise coupling. This type of cable will give good performance for most frequencies used with the OP-43. At frequencies above ~100kHz, however, the capacitance of this type of transmission line can seriously degrade performance. In this case, regular coaxial cable should be used.

For best results, the shield should be driven by a low impedance voltage of the same level as the input signal. This will minimize the differential voltage across the cable insulation, greatly reducing leakages and the effective input capacitance of the cable. Shielding should be connected in such a manner as to avoid ground loops. For the operating frequencies of the OP-43, this means connecting one end of the shield while the other is left free. The choice of which end is connected is dependent upon the specific application.

When the shield is grounded, and a transducer is being used which requires a ground reference, it is generally preferable to make the connection at the remote side. If the shield is being driven by the OP-43 as discussed below, the connection must be at the op amp end. Using these techniques, noise induced by electric fields can be virtually eliminated.

In a noninverting amplifier configuration, the shield may be attached to the inverting input of the op amp if the feedback voltage divider is of low impedance. Since the amplifier keeps the two inputs at the same potential, the shield will track the signal. This method is shown in Figure 8. If the shield is long, its inherent capacitance can present an excessive load on the input of the device. In this case, or if the feedback network causes the input to be a high impedance node, an OP-41 may be used as a buffer to drive the shield. (See Figure 9.) Since the OP-41 is driven by only a portion of the output signal, its slew-rate requirement is reduced. The circuit is stable with gains of 2 or more, but for optimal shielding the gain should be greater than 5. This will optimize the OP-41 buffer's ability to track the signal.

FIGURE 8: Guard Connections For Noninverting Amplifier

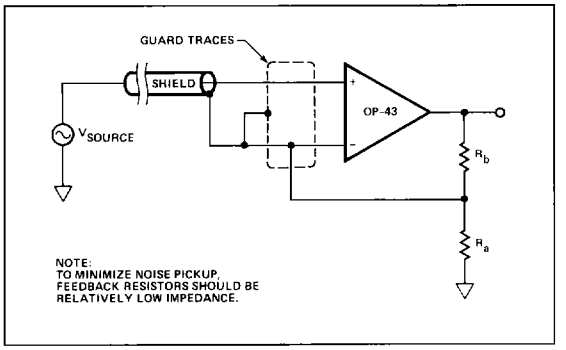
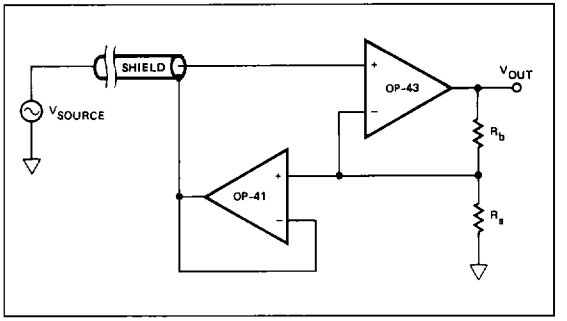


FIGURE 9: Noninverting Amplifier With Shield Driver



When the op amp is used as an inverting amplifier, it is not practical to drive the shield at the same potential as the signal, unless there are shield drivers associated with the signal source. In the case where the source lacks shield drivers, the shield is grounded.

The leakage currents on a PC board, even a clean one, can easily exceed the signals being amplified by a low-bias-current op amp. The best method of eliminating this problem is to use Teflon* insulators to support the wires and components to the inputs and feedback on the op amp. The op amp itself should be placed in a Teflon socket, if possible. This eliminates contact with the PC board for the sensitive high-impedance, low current inputs.

An alternative method is to guard all high impedance traces on the PC board. Guard traces should be placed on both sides of the PC board, around the inputs of the OP-43 and the signal traces. If the op amp is being used in the inverting mode, the guard traces should be connected to ground. In the noninverting mode, the guard traces should be driven by a portion of the OP-43's output signal, in the same manner as used with a cable shield (Figures 8, 9). Again, the idea is to minimize the differential voltages between the signal lines and the guard traces. When the guard drive voltage is equal to the input signal, leakage currents will be effectively eliminated.

CURRENT-TO-VOLTAGE CONVERSION

One of the most common applications of low-bias-current amplifiers is as a current-to-voltage converter. A wide-range photodetector is shown in Figure 10, which has excellent sensitivity and speed. It demonstrates a method of achieving higher gains without using large feedback resistors, by taking the feedback from a fraction of the output. Not only will this method reduce the noise associated with the resistors, but it allows the use of more easily obtained components. This circuit makes an excellent receiver for fiber optic uses.

ACTIVE FILTERS

The low bias current and high speed of the OP-43 make it well suited to active filter applications, allowing the use of smaller capacitors and larger resistors to obtain low frequency poles. Two configurations based upon the Sallen & Key type filters are shown in Figures 11 and 12.

For the highpass design, the cutoff frequency f_O and quality factor Q of the filter are defined by

$$f_O = \frac{1}{2\pi RC} \qquad K = 1 + \frac{R_b}{R_a}$$

$$Q = \frac{1}{3 - K} \qquad H = K$$

where K is the gain of the voltage-controlled-voltage-source (i.e. the noninverting op amp), and H is the overall gain of the filter. The transfer function of this filter is

$$\frac{V_{OUT}(\omega)}{V_{IN}(\omega)} = \frac{H(j\omega)^2}{(j\omega)^2 + j\left(\frac{\omega_o}{Q}\right)\omega + \omega_o^2}$$

where $\omega = 2\pi f$ and $j = \sqrt{-1}$.

*Teflon is a registered trademark of the Dupont Company.

FIGURE 10: Photodetector/Fiber-Optic Receiver

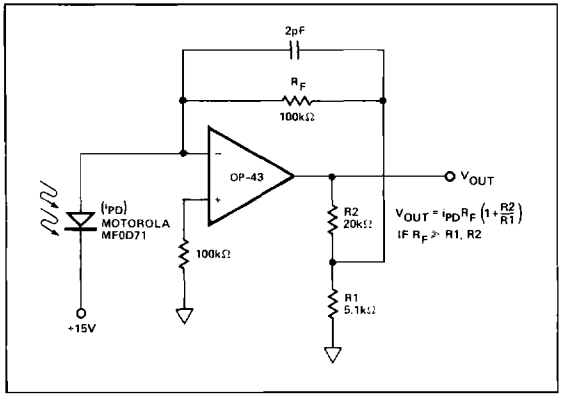


FIGURE 11: Highpass Filter

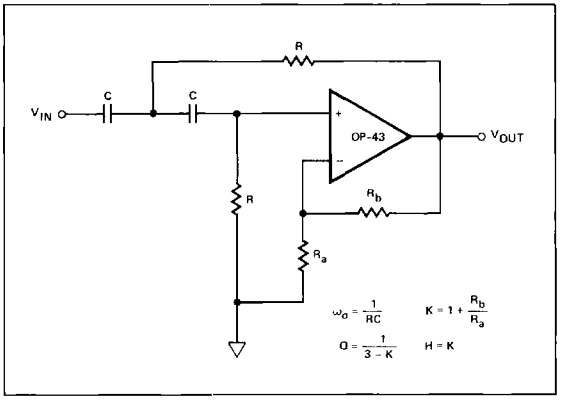
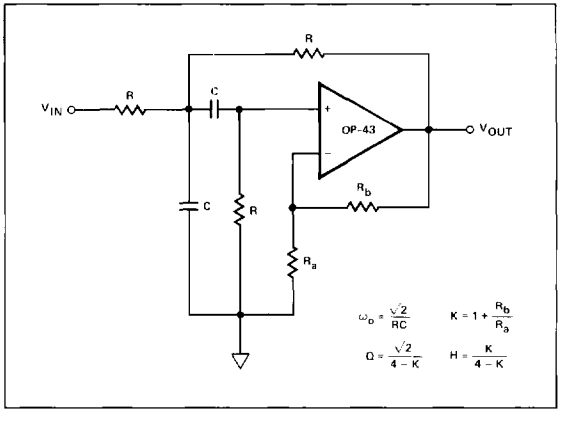


FIGURE 12: Bandpass Filter



As an example, consider a filter with a cutoff frequency of 10kHz and a Q of 5. This will give a steep rolloff with a peak at the edge of the passband. We choose 100pF as a convenient capacitor value, then solving for R and K, we arrive at values of 158kΩ and 2.8, respectively. R_a and R_b are chosen to be 10kΩ and 18kΩ to arrive at the required gain (K) of 2.8, thus giving the desired configuration. The resultant filter displays the desired transfer function and enters a high-frequency rolloff when the op amp goes into slew-rate limiting, about 100kHz for the OP-43 with a ±10V output swing.

The bandpass filter has a center frequency f_O and Q defined by

$$f_O = \frac{\sqrt{2}}{2\pi RC} \qquad K = 1 + \frac{R_b}{R_a}$$

$$Q = \frac{\sqrt{2}}{4-K} \qquad H = \frac{K}{4-K}$$

and its transfer function is

$$\frac{V_{OUT}(\omega)}{V_{IN}(\omega)} = \frac{H\left(\frac{\omega_o}{Q}\right)j\omega}{(j\omega)^2 + j\left(\frac{\omega_o}{Q}\right)\omega + \omega_o^2}$$

Several other designs are possible, with both the highpass and the bandpass filter topographies shown, using unequal values for the resistors and capacitors. For a more complete treatment, consult one of the many books available on active filters, such as **Daryanani:** *Principles of Active Network Synthesis and Design* (Wiley, 1976) or **Huelsman and Allen:** *Introduction to the Theory and Design of Active Filters* (McGraw-Hill, 1980).

INTERFACING TO HIGH IMPEDANCE TRANSDUCERS

Because of its low bias current and very high input-impedance, many high impedance transducers may be directly interfaced with the OP-43. When connecting transducers in this manner, it should be remembered that a return path for the DC bias current, no matter how small it is, must always be provided. If this is neglected, the bias current will charge stray capacitances around the input and create drift problems. With the OP-43, the drift will be significantly smaller than that found with other low-cost devices, but one must still avoid the temptation to eliminate all DC current paths.

Figure 13 shows the OP-43 as a differential amplifier with a piezoelectric pressure transducer. The common-mode rejection of this circuit is primarily dependent upon the resistor matching. A high input impedance is necessary to obtain good low-frequency response. The OP-43's low bias current allows high value resistors to be used in this low-cost circuit, giving it the required impedance. In addition, the cable shield should be grounded to prevent excessive noise pickup. The differential input impedance is

$$R_D = R1 + R3$$

while the gain of the circuit is

$$A_{CL} = \frac{R2}{R1}$$

The OP-43 is especially attractive in this application, where it allows a high-input-impedance differential amplifier to be constructed at minimal cost, while retaining the speed necessary to record transient phenomena.

Extremely high input-impedance is achieved at both inputs using the two op amp instrumentation amplifier shown in Figure 14. The input impedance is that of each OP-43. Common-mode rejection is again dependent upon matching the resistor ratios. The gain of the circuit is given by

$$A_{CL} = 2\left(1 + \frac{R}{R_G}\right)$$

Since each device operates with a gain of 2, the common-mode range is only ±5.5V.

FIGURE 13: Differential Amplifier

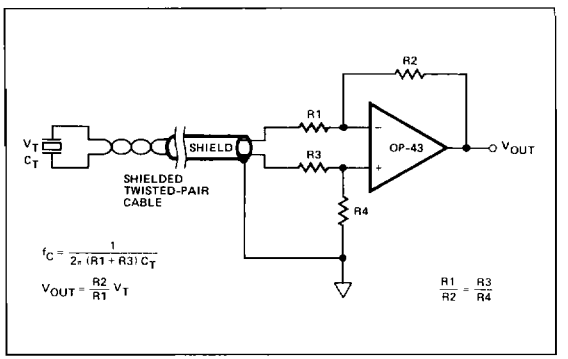
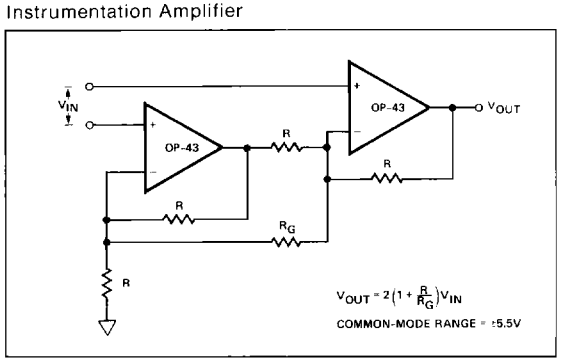


FIGURE 14: High Input-Impedance Instrumentation Amplifier



ISOLATION AMPLIFIER

In conjunction with two optocouplers, or a dual optocoupler such as the Hewlett-Packard HCPL-2530, three OP-43's can be combined to create an isolation amplifier. In this sort of amplifier, the input and the output operate on separate power supplies, allowing extremely high common-mode voltages to be dealt with. In industrial applications, an isolation amplifier protects instrumentation from high voltages at the sensing site. When interfacing with a computing system, an isolation amplifier will protect the rest of the system from a sensor which accidentally becomes shorted to a high voltage.

The basic isolation amplifier circuit is shown in Figure 15(a). The circuit operates on the principle that the nonlinearities of one optocoupler will be tracked by the nonlinearities of another, if they are well matched. By using an optocoupler in the feedback loop of the second OP-43, the nonlinearities of the isolating optocoupler will be cancelled. The operation of the isolation amplifier can be better understood by examining the individual sections of the circuit.

Figure 15(b) shows the isolated input section of the circuit. The output of the OP-43 drives a current through LED_a. Resistor $R3_a$ provides a constant bias for the LED, allowing it to operate at full speed. Since the bias current of the OP-43 is negligible, the current flowing through LED_a will be

$$I_{Fa} = \frac{V_{IN}}{R2_a} + \frac{V_{-2} - V_{IN}}{R3_a}$$

Each LED will induce a current I_C in its associated phototransistor. This current is given by

$$I_{Ca} = K_a \left[\frac{I_{Fa}}{I_{Fa}'}\right]^{n_a} \qquad I_{Cb} = K_b \left[\frac{I_{Fb}}{I_{Fb}'}\right]^{n_b}$$

Thus, the current flowing through the output transistor on the *a* side will be

$$I_{Ca} = K_a \left[\frac{\frac{V_{IN}}{R2_a} + \frac{V_{-1} - V_{IN}}{R3_a}}{I_{Fa}'}\right]^{n_a}$$

Similarly, by analyzing the currents flowing through LED_b, we arrive at an equation for I_{Cb}, which is

$$I_{Cb} = K_b \left[\frac{\frac{V_O}{R2_b} + \frac{V_{-2} - V_O}{R3_b}}{I_{Fb}'}\right]^{n_b}$$

These currents, flowing through resistors R4, form the input for the *b* side of the isolation amplifier, as shown in Figure 15(c). The feedback on the op amp through the optocoupler, forces the noninverting input to the same potential as the inverting input. Note that the output transistor in the optocoupler inverts the polarity of the signal, causing negative feedback through the noninverting input. This effectively reverses the function of the op amp's input pins. The feedback voltage on the noninverting input will be $V_{IN+} = V_{IN-}$, or $I_{Ca} R4_a = I_{Cb} R4_b$.

At this point, we make the assumption that the two optocouplers are well matched, i.e. their current transfer ratios K, as well as their nonlinear response defined by n and I_F', are similar. In addition, since the LEDs are being biased directly from the power supplies, we assume that the supplies for the two sides are both stable and matched in their voltage level. Since the resistors for the *a* and *b* sides are the same values, it can be seen by inspection of the above equations for I_{Ca} and I_{Cb} that $V_O = V_{IN}$. In reality, the optocouplers are not perfectly matched, giving rise to offset and nonlinearity effects.

The last OP-43 is an output buffer for the isolation amplifier. The input to this amplifier is V_O from Figure 15(b), which was shown above to be equivalent to V_{IN}. The low bias current ensures that it does not affect the voltage it is amplifying. Gain is realized in this stage, and any offsets induced in the previous stages may be corrected by offsetting this op amp. Although shown in the circuit as a simple gain stage, this output amplifier may take any form desired. It may be configured as a filter or other waveshaping circuit as needed. The only requirement is that the buffer not disturb the currents in the optocoupler feedback circuit, thus non-inverting amplifier configurations are preferred. For highest linearity, the currents in the two LEDs should track as closely as possible.

In the circuit shown, the LEDs have been biased by resistor R3. For greater accuracy, a precision current sink of approximately 3mA could be substituted for the resistors. In addition, the collectors of the optocoupler output transistors could be connected to a more stable voltage source than the power supplies. These measures would decrease the sensitivity of the amplifier to the power supplies.

With stable supplies, the circuit has excellent response and displays less than 0.5% DC nonlinearity with a $2V_{p-p}$ signal. The high speed of the OP-43 gives the circuit a power bandwidth of 100kHz, while the majority of the power budget is consumed in biasing the LEDs. The dual optocoupler provides isolation against 600VDC common-mode voltages. Higher isolations may be achieved using two separate optocouplers, such as HP's 6N136.

FIGURE 15: Isolation Amplifier