



Integrated Device Technology, Inc.

FAST CMOS BUS INTERFACE LATCHES

IDT54/74FCT841AT/BT/CT/DT

FEATURES:

• Common features:

- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

• Features for FCT841T:

- A, B, C and D speed grades
- High drive outputs (-15mA IOH, 48mA IOL)
- Power off disable outputs permit "live insertion"

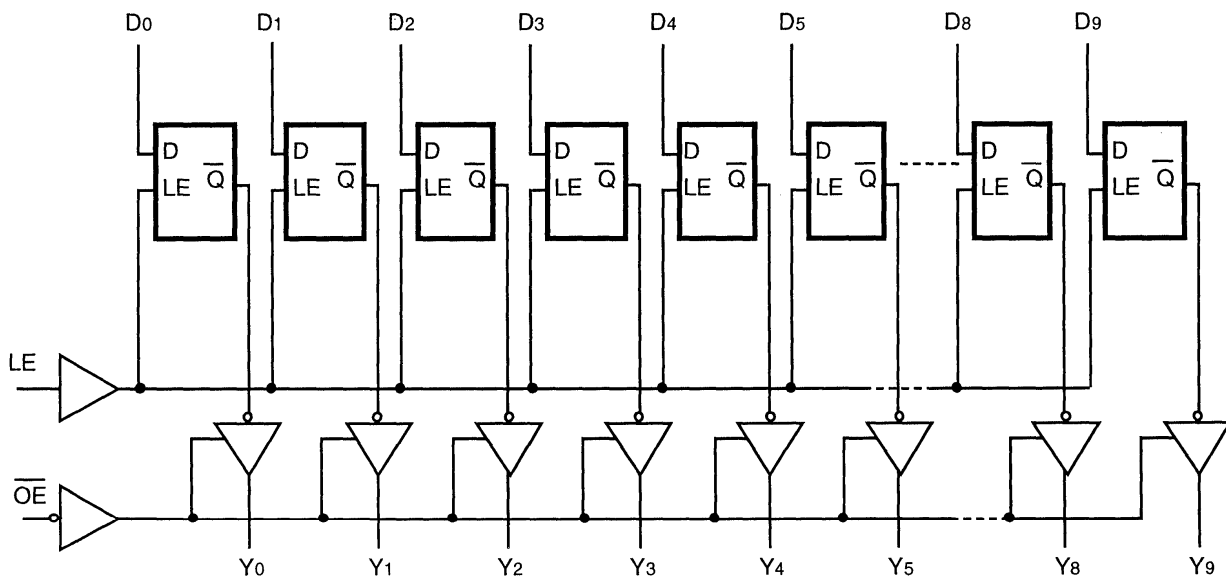
DESCRIPTION:

The FCT8xxT series is built using an advanced dual metal CMOS technology.

The FCT8xxT bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The FCT841T are buffered, 10-bit wide versions of the popular FCT373T function. They are ideal for use as an output port requiring high IOL/IOH.

All of the FCT8xxT high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes to ground and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



2571 drw 01

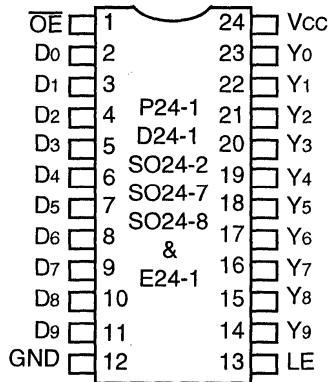
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

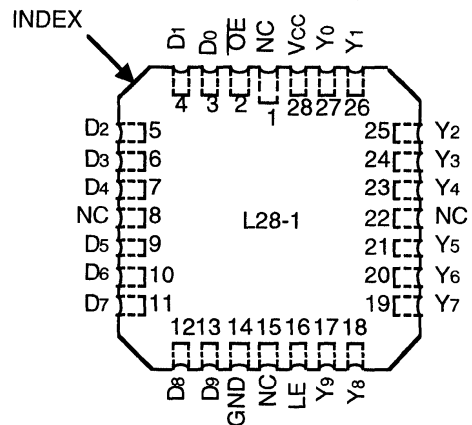
AUGUST 1995

PIN CONFIGURATIONS



**DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW**

2571 drw 02



**LCC
TOP VIEW**

2571 drw 03

PIN DESCRIPTION

Name	I/O	Description
D _i	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y _i	O	The 3-state latch outputs.
\overline{OE}	I	The output enable control. When \overline{OE} is LOW, the outputs are enabled. When \overline{OE} is HIGH, the outputs V _i are in high-impedance (off) state.

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FUNCTION TABLE⁽¹⁾

Inputs			Internal	Output	Function
\overline{OE}	LE	D _i	Q _i	Y _i	
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE:

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1. H=HIGH, L=LOW, X=Don't Care, NC=No Change, Z=High Impedance

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	-0.5 to V _{CC} +0.5	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	-60 to +120	-60 to +120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

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1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	V _{CC} = Max. V _I = 2.7V	—	—	±1	μA
I _{IL}	Input LOW Current ⁽⁴⁾		V _I = 0.5V	—	—	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	V _{CC} = Max. V _O = 2.7V	—	—	±1	μA
I _{OZL}			V _O = 0.5V	—	—	
I _I	Input HIGH Current ⁽⁴⁾	V _{CC} = Max., V _I = V _{CC} (Max.)	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V
V _H	Input Hysteresis	—	—	200	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}	—	0.01	1	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT841T

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OH} = -6mA MIL.	2.4	3.3	—	V
		I _{OH} = -8mA COM'L.	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OL} = 32mA MIL.	—	0.3	0.5	V
		I _{OL} = 48mA COM'L.	—	—	—	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾	-60	-120	-225	mA
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V	—	—	±1	μA

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5μA at TA = -55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open \overline{OE} = GND LE = V _{CC} One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle \overline{OE} = GND LE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	1.5	3.5	mA
			V _{IN} = 3.4 V _{IN} = GND	—	1.8	4.5	
		V _{CC} = Max. Outputs Open f _i = 2.5MHz 50% Duty Cycle \overline{OE} = GND LE = V _{CC} Eight Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	3.0	6.0 ⁽⁵⁾	
			V _{IN} = 3.4 V _{IN} = GND	—	5.0	14.0 ⁽⁵⁾	

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions ⁽¹⁾	FCT841AT				FCT841BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay DI to Y1 (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay LE to Y1	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	
tPZH tPZL	Output Enable Time \overline{OE} to Y1	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	
tPHZ tPLZ	Output Disable Time \overline{OE} to Y1	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	
tsu	Data to LE Set-up Time	CL = 50pF	2.5	—	2.5	—	2.5	—	2.5	—	ns
th	Data to LE Hold Time	RL = 500Ω	2.5	—	3.0	—	2.5	—	2.5	—	ns
tw	LE Pulse Width HIGH ⁽³⁾		4.0	—	5.0	—	4.0	—	4.0	—	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions ⁽¹⁾	FCT841CT				FCT841DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay DI to Y1 (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	5.5	1.5	6.3	1.5	4.2	—	—	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	13.0	1.5	15.0	1.5	8.0	—	—	
tPLH tPHL	Propagation Delay LE to Y1	CL = 50pF RL = 500Ω	1.5	6.4	1.5	6.8	1.5	4.0	—	—	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	15.0	1.5	16.0	1.5	8.0	—	—	
tPZH tPZL	Output Enable Time \overline{OE} to Y1	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.3	1.5	4.8	—	—	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	12.0	1.5	13.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time \overline{OE} to Y1	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	5.7	1.5	6.0	1.5	4.0	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	6.3	1.5	4.0	—	—	
tsu	Data to LE Set-up Time	CL = 50pF	2.5	—	2.5	—	1.5	—	—	—	ns
th	Data to LE Hold Time	RL = 500Ω	2.5	—	2.5	—	1.0	—	—	—	ns
tw	LE Pulse Width HIGH ⁽³⁾		4.0	—	4.0	—	3.0	—	—	—	ns

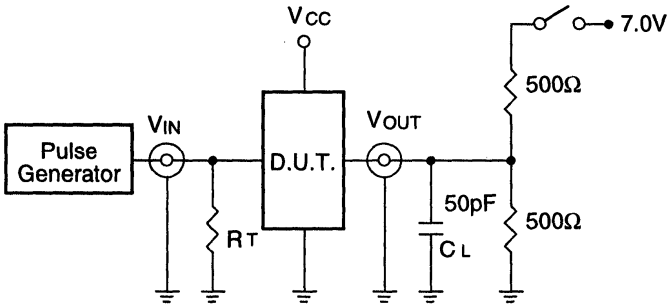
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

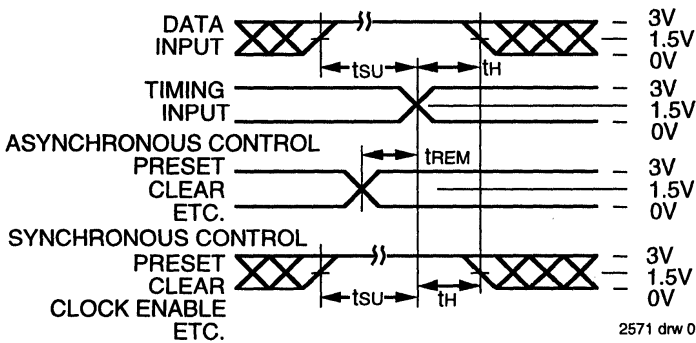
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.
RT= Termination resistance: should be equal to Z₀ of the Pulse Generator.

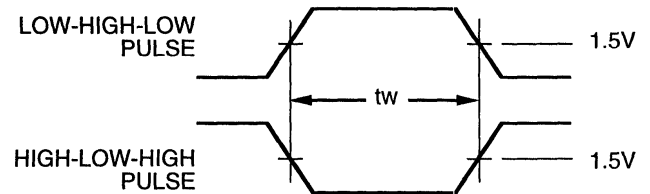
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SET-UP, HOLD AND RELEASE TIMES



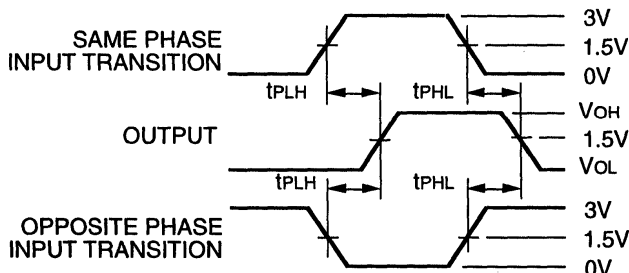
2571 drw 05

PULSE WIDTH



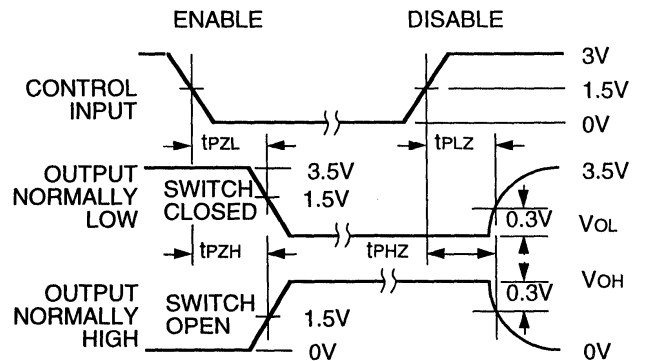
2571 drw 06

PROPAGATION DELAY



2571 drw 07

ENABLE AND DISABLE TIMES

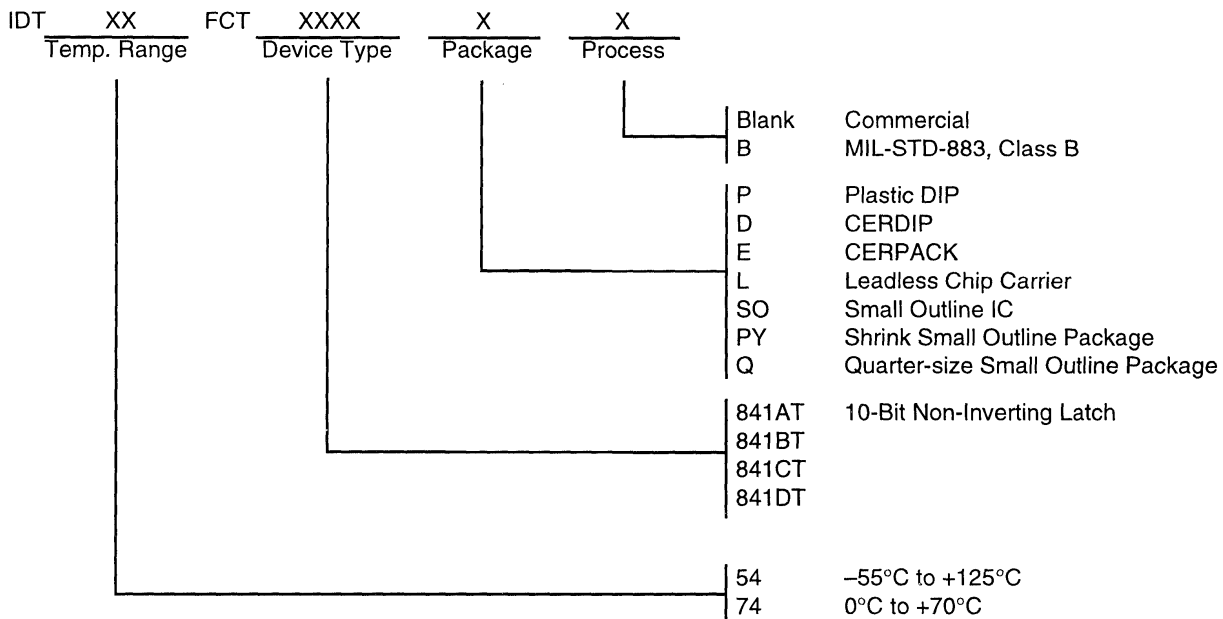


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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns

ORDERING INFORMATION



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