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- Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic DIPs
- Input and Output Latches with Active-High Enables
- Fast Compare to Zero
- Arithmetic and Logical Comparison
- Open-Collector P = Q Output

description

These Advanced Schottky devices are capable of performing high-speed arithmetic or logical comparisons on two 8-bit binary or two's complement words. Three fully decoded decisions about words P and Q are externally available at the outputs. These devices are fully expandable to any word length by connecting the totem pole P>Q and P<Q outputs of each stage to the P>Q and P<Q inputs of the next higher-order stage. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. The opencollector P=Q output may be wire-ANDed together.

Both input words P and Q plus all three outputs (P>Q, P<Q, and P = Q) are equipped with latches to provide the designer with temporary data storage for avoiding race conditions. The enable circuitry is implemented with minimal delay times to enhance performance when the devices are cascaded for longer word lengths. Each latch is transparent when the appropriate latch enable, PLE, QLE, or OLE is high.

The enable inputs PLE and QLE and data inputs P and Q utilize pnp input transistors to reduce the low-level input current requirement to typically -0.25 mA, which minimizes loading effects.

The Q register may be cleared to zero for a fast comparison of the P word to zero.

The SN54AS866 is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74AS866A is characterized for operation from 0°C to 70°C.

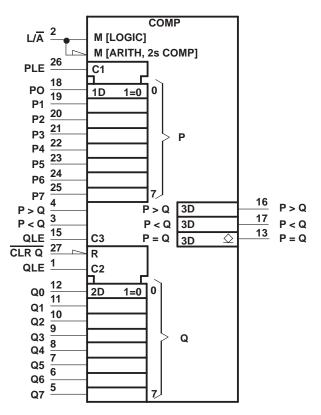


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SN54AS866 JD PACKAGE SN74AS866A N PACKAGE (TOP VIEW)					
QLE L/A P < Qin P > Qin Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q1 Q0 P = Qout GND	1 2 3 4 5 6 7 8 9 10 11 12 13 14	E	Qout Qout		
SN74AS86					
UID ~		P > Qout 12 P > Qout 12 P < Qout 12 P = 0 P = 0	25 P7 24 P6 23 P5 22 P4 21 P3 20 P2 19 P1		

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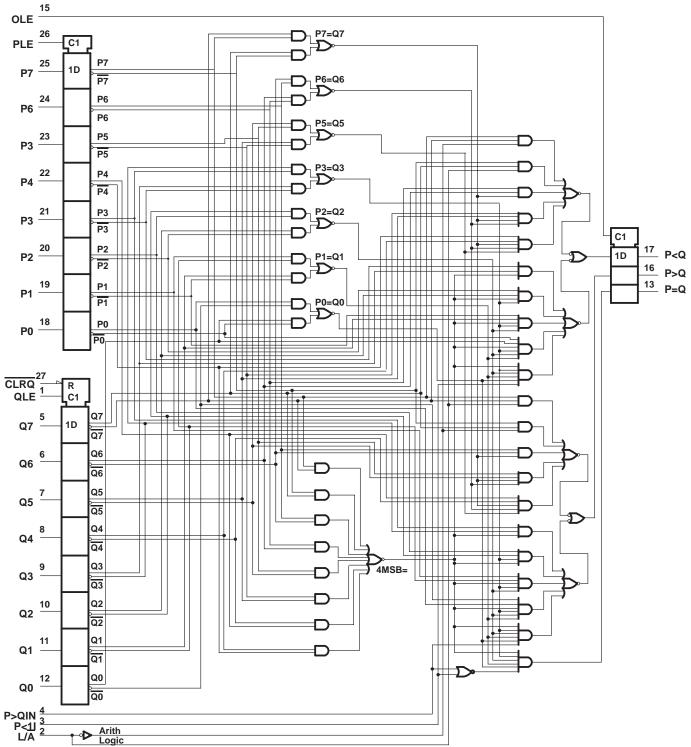
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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logic diagram (positive logic)



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			FUNCTION TA	BLE					
	. 77	DATA INPUTS	INPUTS INPUTS			OUTPUTS			
COMPARISON	L/A	P0-P7, Q0-Q7	P>Q	P <q< th=""><th>P>Q</th><th>P<q< th=""><th>P=Q</th></q<></th></q<>	P>Q	P <q< th=""><th>P=Q</th></q<>	P=Q		
Logical	Н	P>Q	Х	Х	Н	L	L		
Logical	Н	P <q< td=""><td>Х</td><td>Х</td><td>L</td><td>Н</td><td>L</td></q<>	Х	Х	L	Н	L		
Logical	Н	P=Q	L	L	L	L	Н		
Logical	Н	P=Q	L	Н	L	Н	L		
Logical	Н	P=Q	Н	L	Н	L	L		
Logical	Н	P=Q	Н	Н	Н	Н	L		
Arithmetic	L	P AG Q	Х	Х	Н	L	L		
Arithmetic	L	Q AG P	Х	Х	L	Н	L		
Arithmetic	L	P=Q	L	L	L	L	Н		
Arithmetic	L	P=Q	L	Н	L	Н	L		
Arithmetic	L	P=Q	Н	L	Н	L	L		
Arithmetic	L	P=Q	Н	Н	Н	Н	L		

AG = arithmetically greater than

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC}		
Input voltage		
Off-state output voltage, P = Q output		
Operating free-air temperature range:	SN54AS866	–55°C to 125°C
	SN74AS866A	0°C to 70°C
Storage temperature range		–65°C to 150°C

recommended operating conditions

		SI	SN54AS866		SN74AS866A			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2	6	llr.	2			V
VIL	Low-level input voltage		PH.	0.8			0.8	V
IOH	High-level output current, all outputs except P=Q		SC.	-2			-2	mA
VOH	High-level output voltage, P=Q output	202		5.5			5.5	V
IOL	Low-level output current	8,		20			20	mA
t _{su}	Setup time to PLE, OLE, OLE↓	2			2			ns
t _h	Hold time after PLE, QLE, OLE \downarrow	4			4			
tA	Operating free-air temperature	-55		125	0	70		°C

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		AMETER TEST CONDITIONS		SN	54AS866	6	SN74AS866A			
ŀ	ARAMETER			MIN	TYP†	MAX	MIN	TYP [†]	MAX	UNIT
VIK		V _{CC} = 4.5 V,	lj = – 18 mA			-1.2			-1.2	V
VOH	P>Q, P <q< td=""><td>$V_{CC} = 4.5 V \text{ to } 5.5 V,$</td><td>$I_{OH} = -2 \text{ mA}$</td><td>V_{CC}-2</td><td></td><td></td><td>V_{CC}-2</td><td></td><td></td><td></td></q<>	$V_{CC} = 4.5 V \text{ to } 5.5 V,$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2			V _{CC} -2			
IOH	P=Q only	V _{CC} = 4.5 V,	V _{OH} = 5.5 V			0.25			0.25	mA
VOL	•	V _{CC} = 4.5 V,	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
Ι		V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
Lu .	L/A, OLE		\/. 07\/		AF	40			40	
ΙΗ	Others	V _{CC} = 5.5 V,	V _I = 2.7 V	-	<u> </u>	20			20	μA
	L/A, OLE,			200	,					
	P>Qin,			PRODUC		-4			-4	
կլ	P <qin< td=""><td>V_{CC} = 5.5 V,</td><td>$V_{I} = 0.4 V$</td><td><i><</i>`</td><td></td><td></td><td></td><td></td><td></td><td>mA</td></qin<>	V _{CC} = 5.5 V,	$V_{I} = 0.4 V$	<i><</i> `						mA
	CLRQ	1 **				-2			-2	
	P, Q, PLE, QLE	1			- 0.25	-1		- 0.25		
10‡	•	V _{CC} = 5.5 V,	V _O = 2.25 V	-20		-112	-20		-112	mA
ICC		V _{CC} = 5.5 V,	See Note 1		160	240		160	240	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

NOTE 1: I_{CC} is measured with all inputs high except L/ \overline{A} , which is low.

switching characteristics (see Note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)			$V_{CC} = 4$ $C_L = 50$ $R_L = 50$ $T_A = MI$) pF, 0 Ω,			UNIT
			SI	N54AS86	66	SN	74AS86	δA	
			MIN	TYP†	MAX	MIN	TYP†	MAX	
^t PLH	L/Ā		1	8.5	14	1	8.5	19	
^t PHL	L/A		1	7.5	14	1	7	13	ns
^t PLH	P <q, p="">Q</q,>		1	5	10	1	5	8	-
^t PHL		P <q, p="">Q</q,>	1	5.5	10	1	5.5	8	ns
^t PLH	Any P or Q		1	13.5	21	1	13.5	17.5	-
^t PHL	Data Input		0	10	17	1	10	15	ns
^t PLH	CLRQ		1	16	21	1	16	20	-
^t PHL	ULKQ		1	12	17	1	12	16	ns

PARAMETER	FROM (INPUT)	TO (OUTPUT)		$C_1 = 50$	4.5 V to 0 pF, 80 Ω, IN to MA			UNIT
		(,	SN54AS	6866	SN	74AS86	6A	
			MIN TYP	† мах	MIN	TYP†	MAX	
^t PLH	P <q,< td=""><td>P=Q</td><td>1 6.</td><td>5 12</td><td>1</td><td>6.5</td><td>16</td><td></td></q,<>	P=Q	1 6.	5 12	1	6.5	16	
^t PHL	P>Q	P=Q	1	8 14	1	8	14	ns
^t PLH	Any P or Q	D O	1 1	0 15	1	10	17	
^t PHL	Data Input	P=Q	1,5	9 14	1	9	14	ns
^t PLH	CLRQ	P=Q	<u> </u>	2 17	1	12	24	20
^t PHL	ULKQ	r=Q	२ 1 1	3 18	1	13	21	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25° C.

[‡] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit, IOS.

§ For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuit and voltage waveforms are shown in Section 1 of the ALS/AS Logic Data Book, 1986.

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TYPICAL APPLICATION DATA

This sequence of comparisons illustrates how the $\overline{\text{CLRQ}}$ function can be used to perform dual comparisons of the varying P terms (P0, P1, etc.). When $\overline{\text{CLRQ}}$ is high, the P term is compared to the Q term. When $\overline{\text{CLRQ}}$ is taken low, the P term is compared to zero. This or similar sequences can enhance performance and reduce package count to perform value range checks.

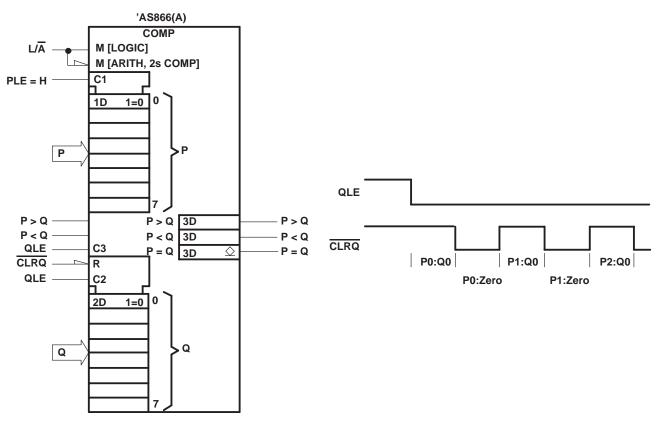


Figure 1. Magnitude Comparisons Combined With Quick Comparisons to Zero (Range Verifications)



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