- **Function, Pinout, and Drive Compatible With FCT and F Logic**
- **Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **Dual 1-of-8 Decoder With Enables**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **CY54FCT138T**
  - **32-mA Output Sink Current**
  - **12-mA Output Source Current**
- **CY74FCT138T**
  - **64-mA Output Sink Current**
  - **32-mA Output Source Current**

CY54FCT138T . . . D PACKAGE
CY74FCT138T . . . Q OR SO PACKAGE
(TOP VIEW)

A_0	1	16 V_{CC}
A_1	2	15 $\overline{O}_0$
A_2	3	14 $\overline{O}_1$
$\overline{E}_1$	4	13 $\overline{O}_2$
$\overline{E}_2$	5	12 $\overline{O}_3$
E_3	6	11 $\overline{O}_4$
$\overline{O}_7$	7	10 $\overline{O}_5$
GND	8	9 $\overline{O}_6$
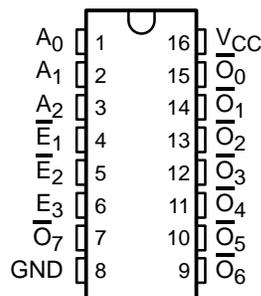
CY54FCT138T . . . L PACKAGE
(TOP VIEW)

Top pins (left to right): A_1 (3), A_0 (2), NC (1), V_{CC} (20), $\overline{O}_0$ (19)

A_2	4	18 $\overline{O}_1$
$\overline{E}_1$	5	17 $\overline{O}_2$
NC	6	16 NC
$\overline{E}_2$	7	15 $\overline{O}_3$
E_3	8	14 $\overline{O}_4$

Bottom pins (left to right): $\overline{O}_7$ (9), GND (10), NC (11), $\overline{O}_6$ (12), $\overline{O}_5$ (13)
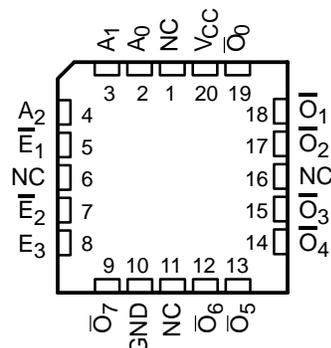
NC – No internal connection

description

The 'FCT138T devices are 1-of-8 decoders. These devices accept three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provide eight mutually exclusive active-low outputs ($\overline{O}_0$–$\overline{O}_7$). The 'FCT138T devices feature three enable inputs: two active low ($\overline{E}_1$, $\overline{E}_2$) and one active high (E_3).

All outputs are high unless $\overline{E}_1$ and $\overline{E}_2$ are low and E_3 is high. This multiple-enable function allows easy parallel expansion of the device to a 1-of-32 (five lines to 32 lines) decoder with just four 'FCT138T devices and one inverter.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION
A	Address inputs
$\overline{E}_1$, $\overline{E}_2$	Enable inputs (active low)
E_3	Enable input (active high)
$\overline{O}$	Outputs

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

ORDERING INFORMATION

T$_A$	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QSOP – Q	Tape and reel	5	CY74FCT138CTQCT	FT138-3
	SOIC – SO	Tube	5	CY74FCT138CTSOC	FCT138C
		Tape and reel	5	CY74FCT138CTSOCT	
	QSOP – Q	Tape and reel	5.8	CY74FCT138ATQCT	FT138-1
	SOIC – SO	Tube	5.8	CY74FCT138ATSOC	FCT138A
		Tape and reel	5.8	CY74FCT138ATSOCT	
	QSOP – Q	Tape and reel	9	CY74FCT138TQCT	FT138
−55°C to 125°C	LCC – L	Tube	6	CY54FCT138CTLMB	
	LCC – L	Tube	12	CY54FCT138TLMB	
	CDIP – D	Tube	12	CY54FCT138TDMB	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E$_3$	A$_0$	A$_1$	A$_2$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High logic level, L = Low logic level, X = Don't care

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic diagram (positive logic)

Pin numbers shown are for the D, Q, and SO packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	−0.5 V to 7 V
DC input voltage range	−0.5 V to 7 V
DC output voltage range	−0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	90°C/W
SO package	57°C/W
Ambient temperature range with power applied, T_A	−65°C to 135°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

PARAMETER		CY54FCT138T			CY74FCT138T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−32	mA
I_{OL}	Low-level output current			32			64	mA
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		CY54FCT138T			CY74FCT138T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = −18 mA		−0.7	−1.2				V
	V_{CC} = 4.75 V,	I_{IN} = −18 mA					−0.7	−1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = −32 mA				2			
		I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.3	0.55	
V_{hys}	All inputs			0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}			5				µA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}						5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V						±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V						±1	
I_{OS}‡	V_{CC} = 5.5 V,	V_{OUT} = 0 V	−60	−120	−225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V				−60	−120	−225	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V			±1			±1	µA
I_{CC}	V_{CC} = 5.5 V,	$V_{IN} \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V		0.1	0.2				mA
	V_{CC} = 5.25 V,	$V_{IN} \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V					0.1	0.2	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open			0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open						0.5	2	
I_{CCD}¶	V_{CC} = 5.5 V, Outputs open, One bit switching at 50% duty cycle, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V			0.06	0.12				mA/MHz
	V_{CC} = 5.25 V, Outputs open, One bit switching at 50% duty cycle, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V						0.06	0.12	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

TEXAS INSTRUMENTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT138T			CY74FCT138T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_C#	V_{CC} = 5.5 V, Outputs open, Switch $\overline{E}_1$, $\overline{E}_2$, or E_3	One output switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V		0.7	1.4				mA
			V_{IN} = 3.4 V or GND		1	2.4				
	V_{CC} = 5.25 V, Outputs open, Switch $\overline{E}_1$, $\overline{E}_2$, or E_3	One output switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V					0.7	1.4‖	
			V_{IN} = 3.4 V or GND					1	2.4‖	
C_i					5	10		5	10	pF
C_o					9	12		9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.
# I_C　　= $I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$
　Where:
　I_C　　= Total supply current
　I_{CC}　= Power-supply current with CMOS input levels
　ΔI_{CC}　= Power-supply current for a TTL high input (V_{IN} = 3.4 V)
　D_H　= Duty cycle for TTL inputs high
　N_T　= Number of TTL inputs at D_H
　I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
　f_0　　= Clock frequency for registered devices, otherwise zero
　f_1　　= Input signal frequency
　N_1　= Number of inputs changing at f_1
　All currents are in milliamperes and all frequencies are in megahertz.
‖ Values for these conditions are examples of the I_{CC} formula.

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT138T		CY54FCT138CT		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	$\overline{O}$	1.5	12	1.5	6	ns
t_{PHL}			1.5	12	1.5	6	
t_{PLH}	$\overline{E}_1$ or $\overline{E}_2$	$\overline{O}$	1.5	12.5	1.5	6.1	ns
t_{PHL}			1.5	12.5	1.5	6.1	
t_{PLH}	E_3	$\overline{O}$	1.5	12.5	1.5	6.1	ns
t_{PHL}			1.5	12.5	1.5	6.1	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT138T		CY74FCT138AT		CY74FCT138CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	$\overline{O}$	1.5	9	1.5	5.8	1.5	5	ns
t_{PHL}			1.5	9	1.5	5.8	1.5	5	
t_{PLH}	$\overline{E}_1$ or $\overline{E}_2$	$\overline{O}$	1.5	9	1.5	5.9	1.5	5	ns
t_{PHL}			1.5	9	1.5	5.9	1.5	5	
t_{PLH}	E_3	$\overline{O}$	1.5	9	1.5	5.9	1.5	5	ns
t_{PHL}			1.5	9	1.5	5.9	1.5	5	

TEXAS INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
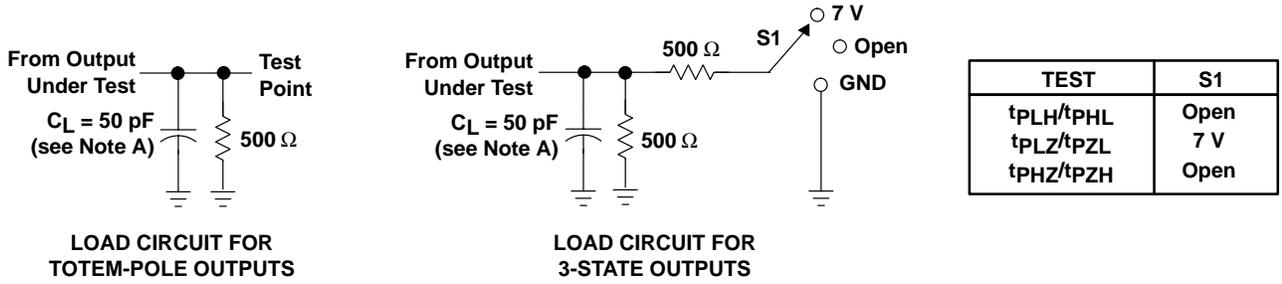
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

C_L = 50 pF (see Note A)

LOAD CIRCUIT FOR 3-STATE OUTPUTS

C_L = 50 pF (see Note A)
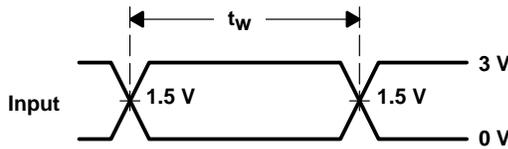
VOLTAGE WAVEFORMS PULSE DURATION
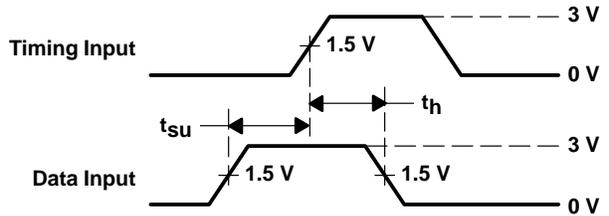
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES
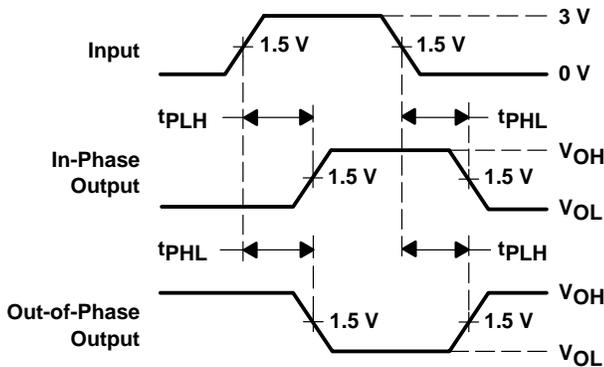
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS
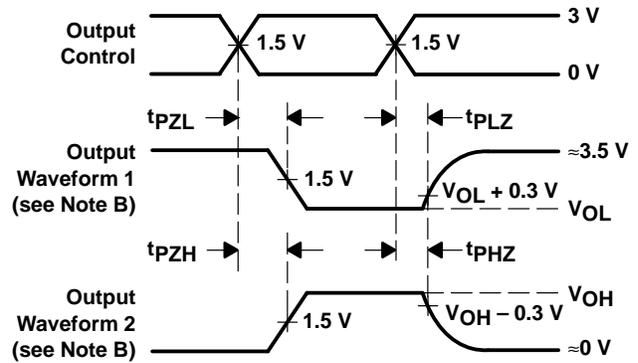
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
     Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9223302M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9223302M2A CY54FCT 138TLMB	Samples
5962-9223302MEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9223302MEA CY54FCT138TDMB	Samples
5962-9223306M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9223306M2A CY54FCT 138CTLMB	Samples
5962-9223306MEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9223306MEA	Samples
CY54FCT138CTLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9223306M2A CY54FCT 138CTLMB	Samples
CY54FCT138TDMB	ACTIVE	CDIP	J	16	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9223302MEA CY54FCT138TDMB	Samples
CY54FCT138TLMB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9223302M2A CY54FCT 138TLMB	Samples
CY74FCT138ATQCT	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT138-1	Samples
CY74FCT138ATSOC	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138A	Samples
CY74FCT138ATSOCG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138A	Samples
CY74FCT138ATSOCT	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138A	Samples
CY74FCT138CTQCT	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT138-3	Samples
CY74FCT138CTSOC	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT138C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT138TQCT	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT138	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT138ATQCT	SSOP	DBQ	16	2500	340.5	338.1	20.6
CY74FCT138ATSOCT	SOIC	DW	16	2000	350.0	350.0	43.0
CY74FCT138CTQCT	SSOP	DBQ	16	2500	340.5	338.1	20.6
CY74FCT138TQCT	SSOP	DBQ	16	2500	340.5	338.1	20.6

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