

## 1.8-V PHASE LOCK LOOP CLOCK DRIVER

### FEATURES

- 1.8-V/1.9-V Phase Lock Loop Clock Driver for Double Data Rate (DDR II) Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 125 MHz to 410 MHz
- Application Frequency: 160 MHz to 410 MHz
- Low Current Consumption: <200 mA Typ
- Low Jitter (Cycle-Cycle):  $\pm 40$  ps
- Low Output Skew: 35 ps
- Stabilization Time <6  $\mu$ s
- Distributes One Differential Clock Input to Ten Differential Outputs
- 52-Ball  $\mu$ BGA (MicroStar Junior™ BGA, 0,65-mm pitch)
- External Feedback Pins (FBIN,  $\overline{\text{FBIN}}$ ) are Used to Synchronize the Outputs to the Input Clockst
- Meets or Exceeds CUA877/CAU878 Specification PLL Standard for PC2-3200/4300/5300/6400o
- Fail-Safe Inputs

### DESCRIPTION

The CDCUA877 is a high-performance, low-jitter, low-skew, zero-delay buffer that distributes a differential clock input pair (CK,  $\overline{\text{CK}}$ ) to ten differential pairs of clock outputs ( $\text{Y}_n$ ,  $\overline{\text{Y}}_n$ ) and to one differential pair of feedback clock outputs (FBOU,  $\overline{\text{FBOU}}$ ). The clock outputs are controlled by the input clocks (CK,  $\overline{\text{CK}}$ ), the feedback clocks (FBIN,  $\overline{\text{FBIN}}$ ), the LVCMOS control pins (OE, OS), and the analog power input ( $\text{AV}_{\text{DD}}$ ). When OE is low, the clock outputs, except FBOU/ $\overline{\text{FBOU}}$ , are disabled while the internal PLL continues to maintain its locked-in frequency. OS (output select) is a program pin that must be tied to GND or  $\text{V}_{\text{DD}}$ . When OS is high, OE functions as previously described. When OS and OE are both low, OE has no affect on  $\text{Y}_7/\overline{\text{Y}}_7$ , they are free running. When  $\text{AV}_{\text{DD}}$  is grounded, the PLL is turned off and bypassed for test purposes.

When both clock inputs (CK,  $\overline{\text{CK}}$ ) are logic low, the device enters in a low power mode. An input logic detection circuit on the differential inputs, independent from input buffers, detects the logic low level and performs in a low power state where all outputs, the feedback, and the PLL are off. When the clock inputs transition from being logic low to being differential signals, the PLL turns back on, the inputs and the outputs are enabled, and the PLL obtains phase lock between the feedback clock pair (FBIN,  $\overline{\text{FBIN}}$ ) and the clock input pair (CK,  $\overline{\text{CK}}$ ) within the specified stabilization time.

The CDCUA877 is able to track spread spectrum clocking (SSC) for reduced EMI. This device operates from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

### AVAILABLE OPTIONS

$\text{T}_\text{A}$	52-Ball BGA <sup>(1)</sup>
$-40^\circ\text{C}$ to $85^\circ\text{C}$	CDCUA877ZQL

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



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**Table 1. Terminal Functions**

NAME	BGA	MLF	I/O	DESCRIPTION
AGND	G1	7		Analog ground
AV <sub>DD</sub>	H1	8		Analog power
CK	E1	4	I	Clock input with a (10 kΩ to 100 kΩ) pulldown resistor
$\overline{\text{CK}}$	F1	5	I	Complementary clock input with a (10 kΩ to 100 kΩ) pulldown resistor
FBIN	E6	27	I	Feedback clock input
$\overline{\text{FBIN}}$	F6	26	I	Complementary feedback clock input
FBOUT	H6	24	O	Feedback clock output
$\overline{\text{FBOUT}}$	G6	25	O	Complementary feedback clock output
OE	F5	22	I	Output enable (asynchronous)
OS	D5	21	I	Output select (tied to GND or VDD)
GND	B2, B3, B4, B5, C2, C5, H2, H5, J2, J3, J4, J5	10		Ground
V <sub>DDQ</sub>	D2, D3, D4, E2, E5, F2, G2, G3, G4, G5	1, 6, 9, 15, 20, 23, 28, 31, 36		Logic and output power
Y[0:9]	A2, A1, D1, J1, K3, A5, A6, D6, J6, K4	38, 39, 3, 11, 14, 34, 33, 29, 19, 16	O	Clock outputs
$\overline{\text{Y}}[0:9]$	A3, B1, C1, K1, K2, A4, B6, C6, K6, K5	37, 40, 2, 12, 13, 35, 32, 30, 18, 17	O	Complementary clock outputs

**Table 2. Function Table**

INPUTS					OUTPUTS				PLL
AV <sub>DD</sub>	OE	OS	CK	$\overline{\text{CK}}$	Y	$\overline{\text{Y}}$	FBOUT	$\overline{\text{FBOUT}}$	
GND	H	X	L	H	L		L	H	Bypassed/Off
GND	H	X	H	L	H		H	L	Bypassed/Off
GND	L	H	L	H	L <sub>Z</sub>	L <sub>Z</sub>	L	H	Bypassed/Off
GND	L	L	H	L	L <sub>Z</sub> Y7 Active	L <sub>Z</sub> $\overline{\text{Y7}}$ Active	H	L	Bypassed/Off
1.8 V Nomnal	L	H	L	H	L <sub>Z</sub>	L <sub>Z</sub>	L	H	On
1.8 V Nomnal	L	L	H	L	L <sub>Z</sub> Y7 Active	L <sub>Z</sub> $\overline{\text{Y7}}$ Active	H	L	On
1.8 V Nomnal	H	X	L	H	L	H	L	H	On
1.8 V Nomnal	H	X	H	L	H	L	H	L	On
1.8 V Nomnal	X	X	L	L	L <sub>Z</sub>	L <sub>Z</sub>	L <sub>Z</sub>	L <sub>Z</sub>	Off
X	X	X	H	H	Reserved				

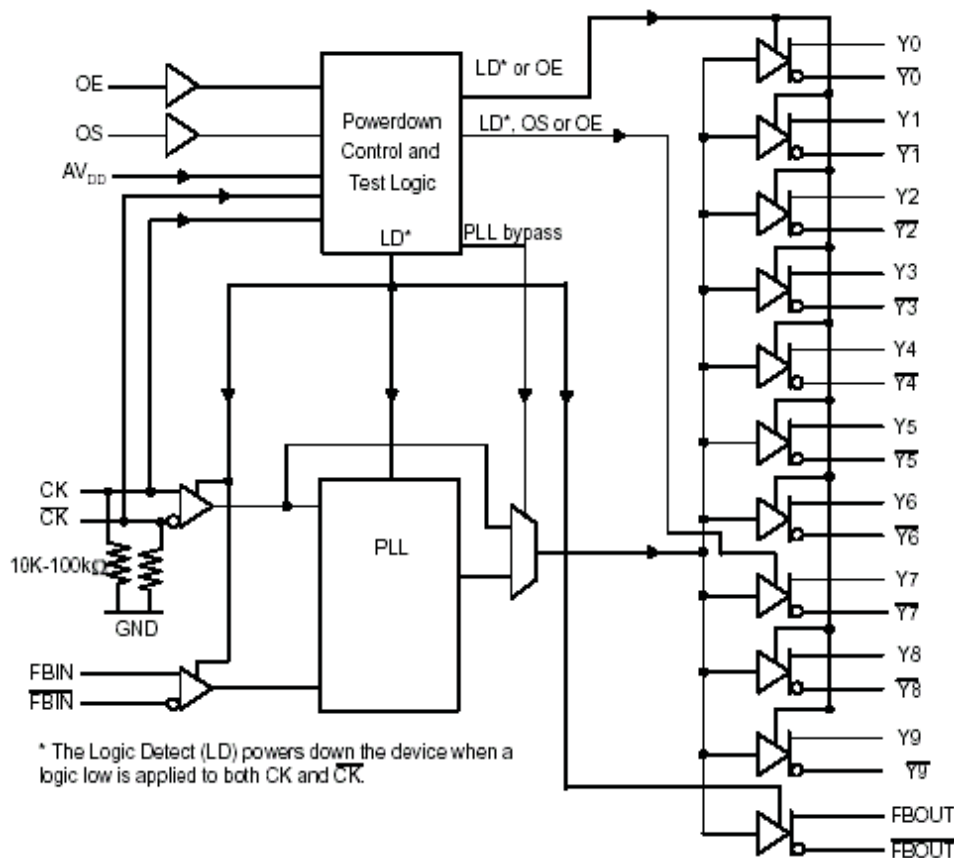


Figure 1. Logic Diagram (Positive Logic)

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE	UNIT
V <sub>DDQ</sub> A <sub>VDD</sub>	Supply voltage range	-0.5 to 2.5	V
V <sub>I</sub>	Input voltage range <sup>(2) (3)</sup>	-0.5 to V <sub>DDQ</sub> + 0.5	V
V <sub>O</sub>	Output voltage range <sup>(2) (3)</sup>	-0.5 to V <sub>DDQ</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current, (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DDQ</sub> )	±50	mA
I <sub>OK</sub>	Output clamp voltage, (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDQ</sub> )	±50	mA
I <sub>O</sub>	Continuous output current, (V <sub>O</sub> = 0 to V <sub>DDQ</sub> )	±50	mA
I <sub>DDC</sub>	Continuous current through each V <sub>DDQ</sub> or GND	±100	mA
R <sub>θJA</sub>	Thermal resistance, junction-to-ambient <sup>(4)</sup>	No airflow	151.9
		Airflow 150 ft/min	146.1
R <sub>θJC</sub>	Thermal resistance, junction-to-case <sup>(4)</sup>	No airflow	102.4
T <sub>STG</sub>	Storage temperature range	-65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.  
 (2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 (3) This value is limited to 2.5 V maximum.  
 (4) The package thermal impedance is calculated in accordance with JESD51 and JEDEC2S1P (high-k board).

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT	
V <sub>DDQ</sub>	Output supply voltage	1.7	1.8	1.9	V	
AV <sub>DD</sub>	Supply voltage <sup>(1)</sup>	V <sub>DDQ</sub>				
V <sub>IL</sub>	Low-level input voltage <sup>(2)</sup>	CK, $\overline{\text{CK}}$ , OE, OS	0.35 × V <sub>DDQ</sub>		V	
V <sub>IH</sub>	High-level input voltage <sup>(2)</sup>	CK, $\overline{\text{CK}}$ , OE, OS	0.65 × V <sub>DDQ</sub>		V	
I <sub>OH</sub>	High-level output current (see <a href="#">Figure 2</a> )				–9 mA	
I <sub>OL</sub>	Low-level output current (see <a href="#">Figure 2</a> )				9 mA	
V <sub>IX</sub>	Input differential-pair cross voltage	(V <sub>DDQ</sub> /2)–0.15	(V <sub>DDQ</sub> /2)+0.15		V	
V <sub>I</sub>	Input voltage level	–0.3	V <sub>DDQ</sub> +0.3		V	
V <sub>ID</sub>	Input differential voltage <sup>(2)</sup> (see <a href="#">Figure 10</a> )	DC	0.3		V <sub>DDQ</sub> +0.4	V
		AC	0.6		V <sub>DDQ</sub> +0.4	V
T <sub>A</sub>	Operating free-air temperature	–40			85 °C	

(1) The PLL is turned off and bypassed for test purposes when AV<sub>DD</sub> is grounded. During this test mode, V<sub>DDQ</sub> remains within the recommended operating conditions and no timing parameters are ensured.

(2) V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on  $\overline{\text{CK}}$ , see [Figure 10](#) for definition. The CK and  $\overline{\text{CK}}$  V<sub>IH</sub> and V<sub>IL</sub> limits define the dc low and high levels for the logic detect state.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	AV <sub>DD</sub> , V <sub>DDG</sub>	MIN	TYP	MAX	UNIT
V <sub>IK</sub>	Input (cl inputs)	I <sub>I</sub> = -18 mA	1.7 V			-1.2	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -100 = A	1.7 V to 1.9 V	VDDQ			V
		I <sub>OH</sub> = -9 mA	1.7 V	-0.2	1.1		
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 100 μA				0.1	V
		I <sub>OL</sub> = 9 mA	1.7 V			0.6	
I <sub>O(DL)</sub>	Low-level output current, disabled	V <sub>O(DL)</sub> = 100 mV, OE = L	1.7 V	100			μA
V <sub>OD</sub>	Differential output voltage <sup>(1)</sup>		1.7 V	0.5			V
I <sub>I</sub>	Input current	CK, $\overline{CK}$	1.9 V			±250	μA
		OE, OS, FBIN, $\overline{FBIN}$	1.9 V			±10	
I <sub>DD(LD)</sub>	Supply current, static (I <sub>DDQ</sub> + I <sub>ADD</sub> )	CK and $\overline{CK}$ = L	1.9 V			500	μA
I <sub>DD</sub>	Supply current, dynamic (I <sub>DDQ</sub> + I <sub>ADD</sub> ) (see <sup>(2)</sup> for C <sub>PD</sub> calculation)	CK and $\overline{CK}$ = 410 MHz, All outputs are open (not connected to a PCB)	1.9 V			225	mA
		All outputs are loaded with 2 pF and 120-Ω termination resistor, CK and $\overline{CK}$ = 410 MHz	1.9 V			225	mA
C <sub>I</sub>	Input capacitance	CK, $\overline{CK}$	V <sub>I</sub> = V <sub>DD</sub> or GND	1.8 V	2	3	pF
		FBIN, $\overline{FBIN}$	V <sub>I</sub> = V <sub>DD</sub> or GND	1.8 V	2	3	
C <sub>I(Δ)</sub>	Change in input current	CK, $\overline{CK}$	V <sub>I</sub> = V <sub>DD</sub> or GND	1.8 V		0.25	pF
		FBIN, $\overline{FBIN}$	V <sub>I</sub> = V <sub>DD</sub> or GND	1.8 V		0.25	

(1) V<sub>OD</sub> is the magnitude of the difference between the true and complimentary outputs. See Figure 10 for a definition.

(2) Total I<sub>DD</sub> = I<sub>DDQ</sub> + I<sub>ADD</sub> = f<sub>CK</sub> × C<sub>PD</sub> × V<sub>DDQ</sub>, solving for C<sub>PD</sub> = (I<sub>DDQ</sub> + I<sub>ADD</sub>)/(f<sub>CK</sub> × V<sub>DDQ</sub>) where f<sub>CK</sub> is the input frequency, V<sub>DDQ</sub> is the power supply, and C<sub>PD</sub> is the power dissipation capacitance.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>CK</sub>	Clock frequency (operating) <sup>(1) (2)</sup>	AV <sub>DD</sub> , V <sub>DD</sub> = 1.8 V ±0.1 V	125		410	MHz
	Clock frequency (application) <sup>(1) (3)</sup>	AV <sub>DD</sub> , V <sub>DD</sub> = 1.8 V ±0.1 V	160		410	MHz
t <sub>DC</sub>	Duty cycle, input clock	AV <sub>DD</sub> , V <sub>DD</sub> = 1.8 V ±0.1 V	40%		60%	
t <sub>L</sub>	Stabilization time <sup>(4)</sup>	AV <sub>DD</sub> , V <sub>DD</sub> = 1.8 V ±0.1 V			6	μs

(1) The PLL must be able to handle spread spectrum induced skew.

(2) Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters (used for low speed system debug).

(3) Application clock frequency indicates a range over which the PLL must meet all timing parameters.

(4) Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal, within the value specified by the static phase offset t<sub>(φ)</sub>, after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and  $\overline{CK}$  go to a logic low state, enter the power-down mode, and later return to active operation. CK and  $\overline{CK}$  may be left floating after they have been driven low for one complete clock cycle.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{en}$	Enable time, OE to any Y/ $\bar{Y}$	See <a href="#">Figure 12</a>			8	ns
$t_{dis}$	Disable time, OE to any Y/ $\bar{Y}$	See <a href="#">Figure 12</a>			8	ns
$t_{jit(cc+)}$	Cycle-to-cycle period jitter <sup>(2)</sup>	160 MHz to 410 MHz, See <a href="#">Figure 5</a>	0		40	ps
$t_{jit(cc-)}$			0		-40	
$t_{(\phi)}$	Static phase offset time <sup>(3)</sup>	See <a href="#">Figure 6</a>	-50		50	ps
$t_{(\phi)dyn}$	Dynamic phase offset time, <sup>(4)</sup>	See <a href="#">Figure 11</a>	-20		20	ps
$t_{sk(o)}$	Output clock skew <sup>(4)</sup>	See <a href="#">Figure 7</a>			35	ps
$t_{jit(per)}$	Period jitter <sup>(2)(5)</sup>	160 MHz to 270 MHz, see <a href="#">Figure 8</a>	-30		30	ps
		271 MHz to 410 MHz, see <a href="#">Figure 8</a>	-20		20	
$t_{jit(hper)}$	Half-period jitter <sup>(2)(5)</sup>	160 MHz to 270 MHz, see <a href="#">Figure 9</a>	-75		75	ps
		271 MHz to 410 MHz, see <a href="#">Figure 9</a>	-50		50	
$\Sigma t_{(su)}$	$ t_{jit(per)}  +  t_{(\phi)dyn}  + t_{sk(o)}$ <sup>(6)</sup>	271 MHz to 410 MHz			80	ps
$\Sigma t_{(h)}$	$ t_{(\phi)dyn}  + t_{sk(o)}$ <sup>(6)</sup>	271 MHz to 410 MHz			60	ps
SR	Slew rate, OE	See <a href="#">Figure 3</a> and <a href="#">Figure 8</a>	0.5			V/ns
	Input clock skew rate	See <a href="#">Figure 3</a> and <a href="#">Figure 8</a>	1	2.5	4	
	Output clock slew rate <sup>(7)(8)</sup>	See <a href="#">Figure 3</a> and <a href="#">Figure 8</a>	1.5	2.5	3	
$V_{OX}$	Output differential-pair cross voltage <sup>(9)</sup>	See <a href="#">Figure 2</a>	$(V_{DDQ}/2) - 0.1$		$(V_{DDQ}/2) + 0.1$	V
	SSC modulation frequency		30		33	kHz
	SSC clock input frequency deviation		0%		-0.5%	
	PLL loop bandwidth		2			MHz

- (1) There are two different terminations that are used with the following tests. The load/board in [Figure 2](#) is used to measure the input and output differential-pair cross voltage only. The load/board in [Figure 3](#) is used to measure all other tests. For consistency, equal length cables must be used.
- (2) This parameter is assured by design and characterization.
- (3) Phase static offset time does not include jitter.
- (4) For full frequency range of 160MHz to 410MHz.
- (5) Period jitter, half-period jitter specifications are separate specifications that must be met independently of each other.
- (6) In the frequency range of 271 MHz to 410 MHz, the minimum and maximum values of  $t_{jit(per)}$  and  $t_{(\phi)dyn}$  and the maximum value for  $t_{sk(o)}$  must not exceed the corresponding minimum and maximum values of the 160 MHz to 270 MHz range. In addition, the sum of the specified values for  $|t_{jit(per)}|$ ,  $|t_{(\phi)dyn}|$ , and  $t_{sk(o)}$  must meet the requirements for the  $\Sigma t_{(su)}$  and the sum of the specified values for  $|t_{(\phi)dyn}|$  and  $t_{sk(o)}$  must meet the requirements for the  $\Sigma t_{(h)}$ .
- (7) The output slew rate is determined from the IBIS model into the load shown in [Figure 4](#).
- (8) To eliminate the impact of input slew rates on static phase offset, the input skew rates of reference clock input CK and  $\bar{CK}$  and feedback clock inputs FBIN and  $\bar{FBIN}$  are recommended to be nearly equal. The 2.5-V/ns skew rates are shown as a recommended target. Compliance with these typical values is not mandatory if it can adequately shown that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
- (9) Output differential-pair cross voltage specified at the DRAM clock input or the test load.

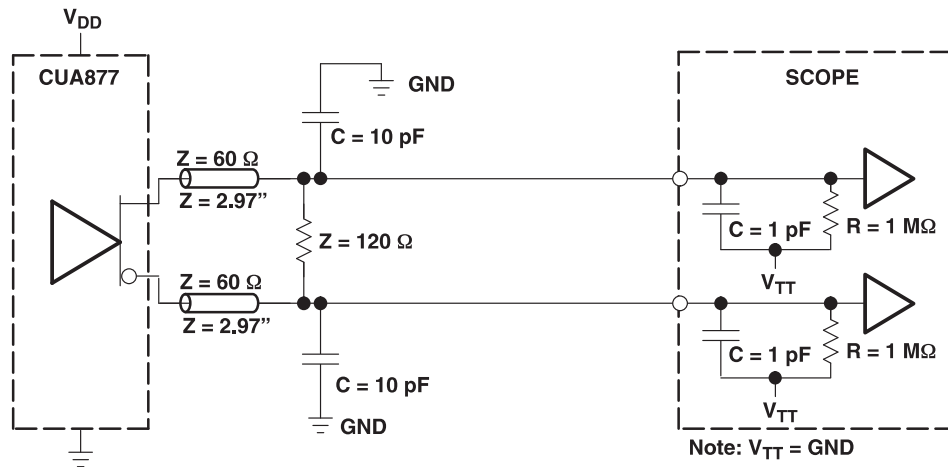


Figure 2. Output Load Test Circuit 1 (Using High-Impedance Probe)

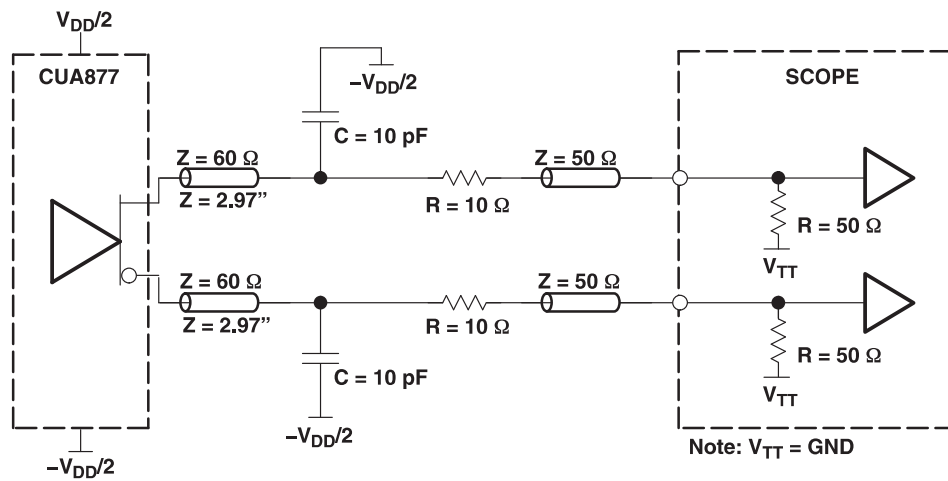


Figure 3. Output Load Test Circuit 2 (Using SMA Coaxial Cable)

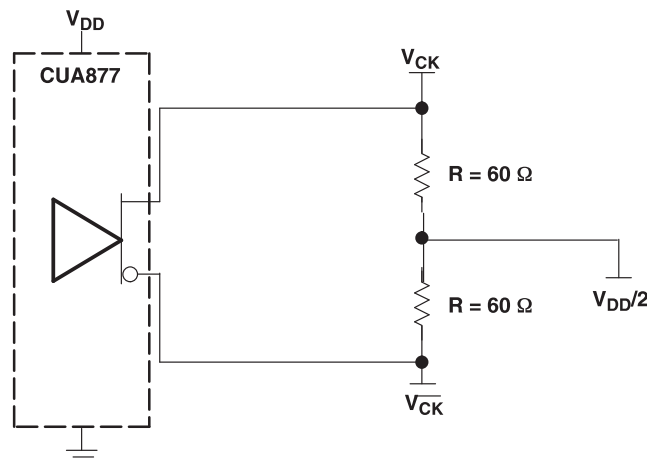


Figure 4. IBIS Model Output Load



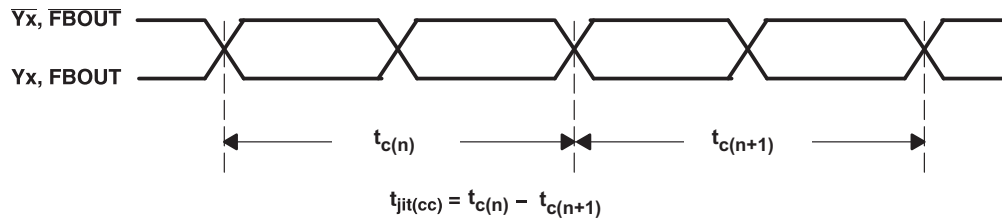


Figure 5. Cycle-To-Cycle Period Jitter

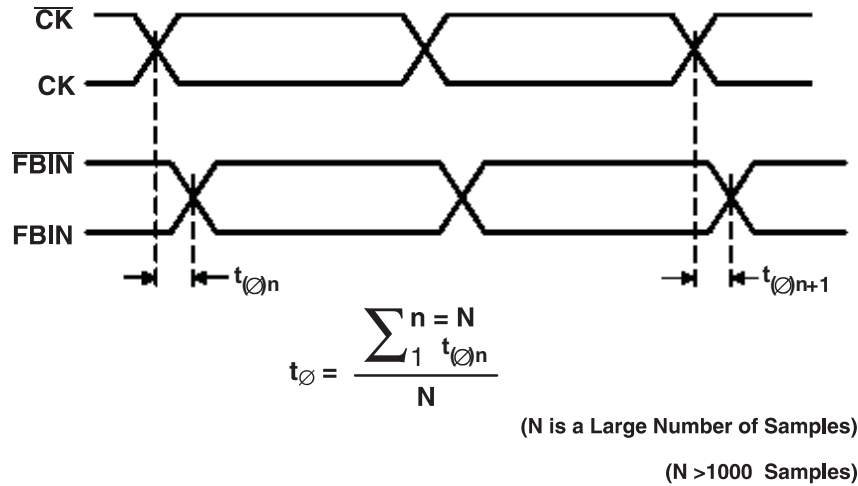


Figure 6. Static Phase Offset

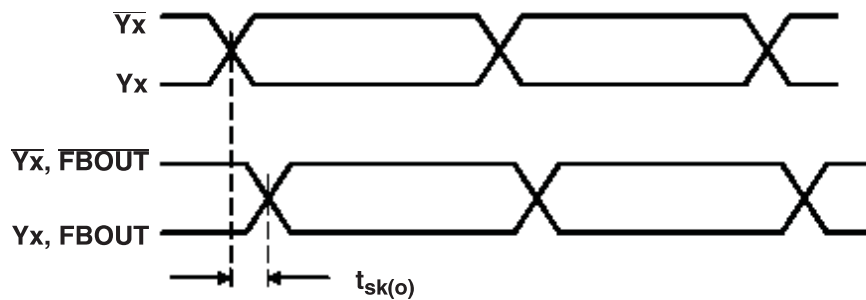
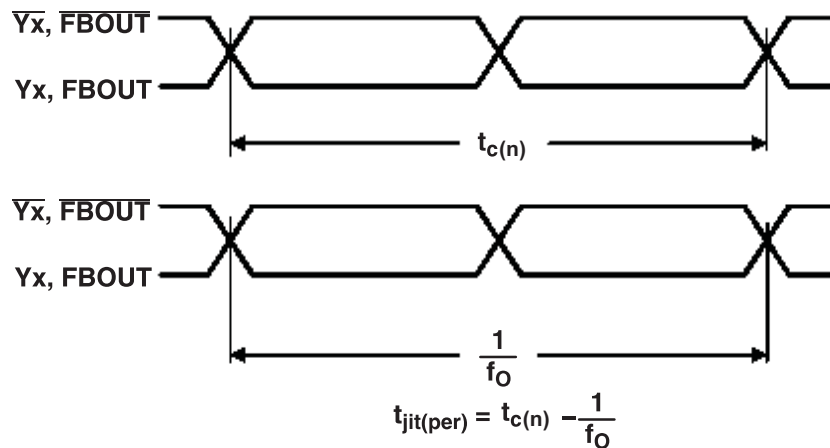
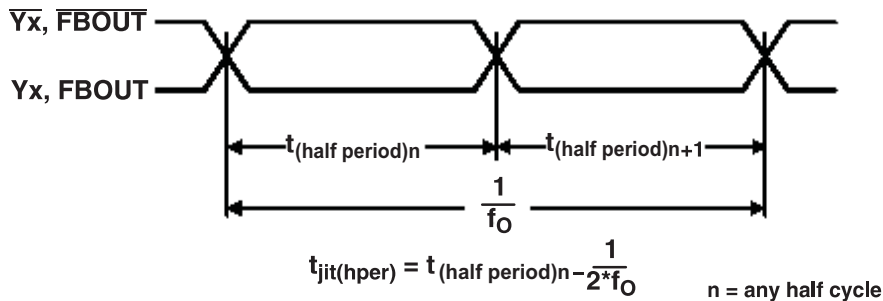


Figure 7. Output Skew



$f_0$  = Average Input Frequency Measured at CK/CK

Figure 8. Period Jitter



( $f_0$  = Average Input Frequency Measured at CK/CK)

Figure 9. Half-Period Jitter

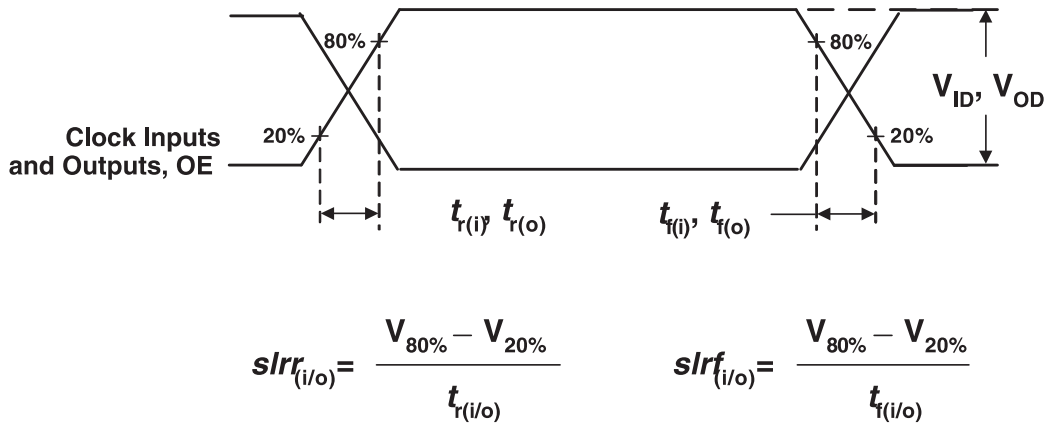


Figure 10. Input and Output Slew Rates

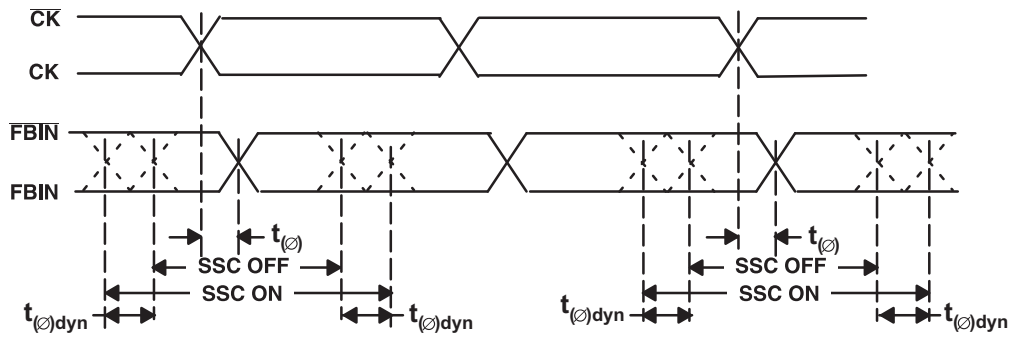


Figure 11. Dynamic Phase Offset

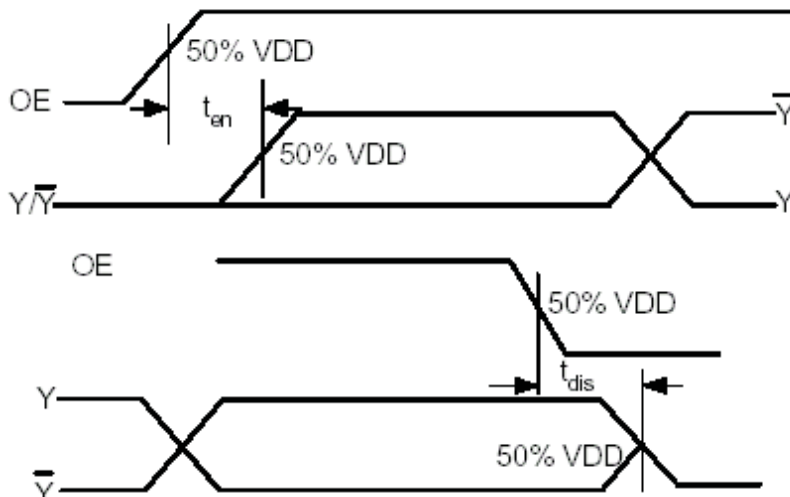
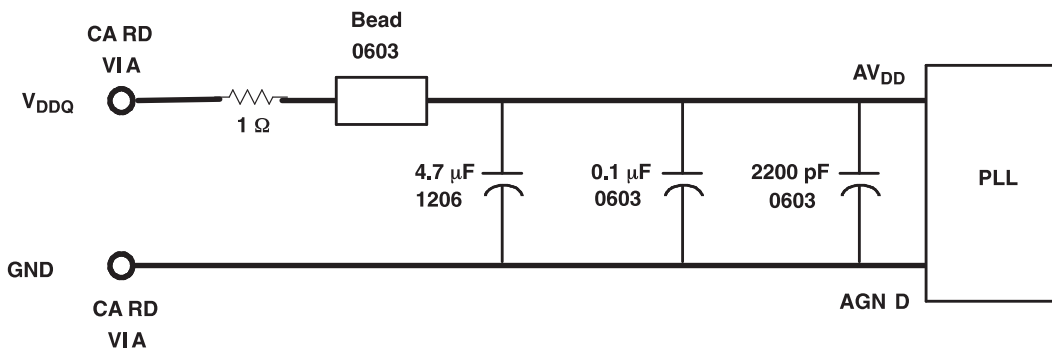


Figure 12. Time Delay Between OE and Clock Output (Y,  $\bar{Y}$ )



- Place the 2200-pF capacitor close to the PLL.
- Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).
- Recommended bead: Fair-Rite PN 2506036017Y0 or equivalent (0.8Ω dc maximum, 600Ω at 100 MHz).

Figure 13. Recommended AV<sub>DD</sub> Filtering

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDCUA877ZQLR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQL	52	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR
CDCUA877ZQLT	ACTIVE	BGA MI CROSTA R JUNI OR	ZQL	52	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCUA877ZQLR	BGA MICROSTAR JUNIOR	ZQL	52	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
CDCUA877ZQLT	BGA MICROSTAR JUNIOR	ZQL	52	250	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

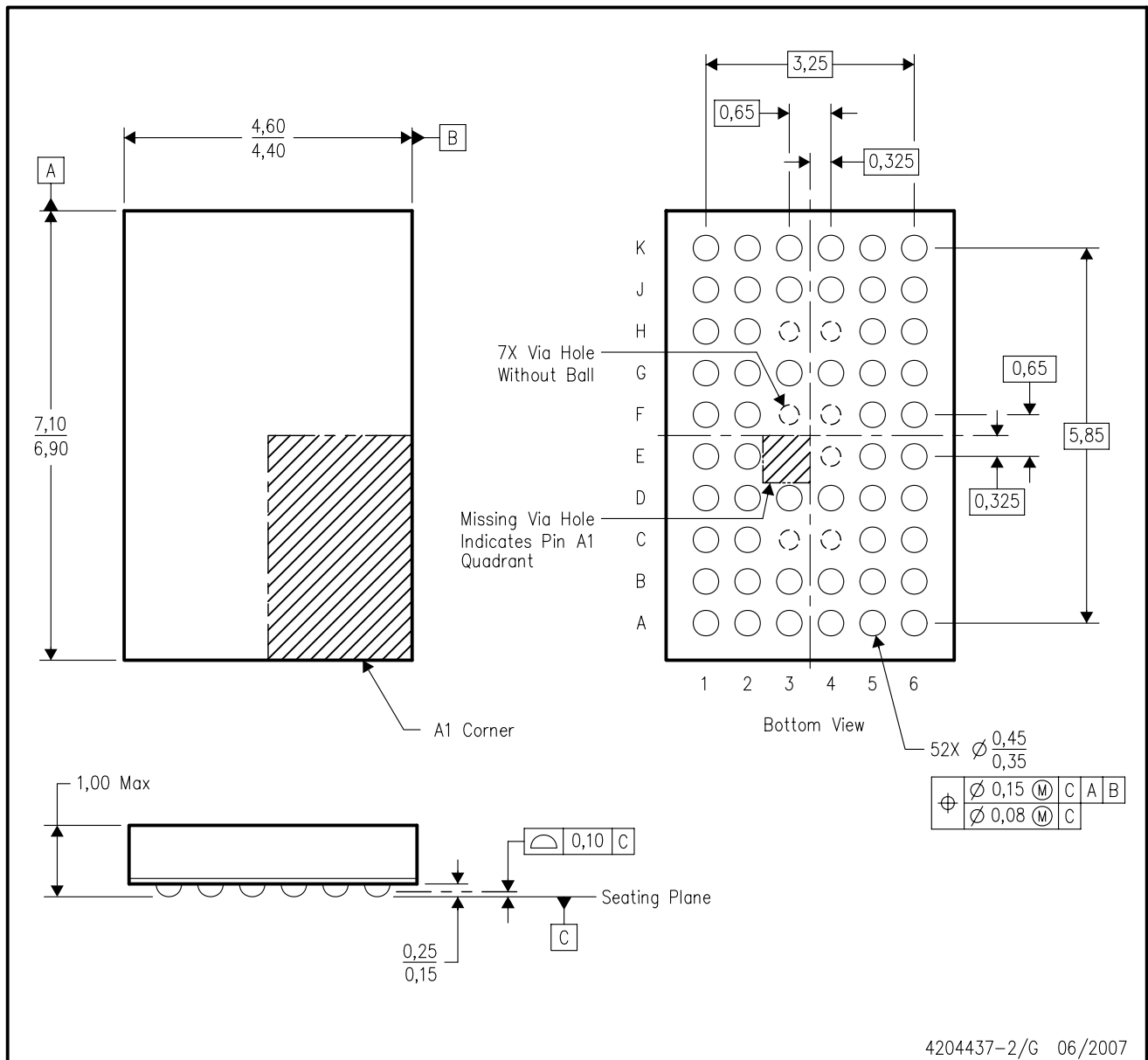
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCUA877ZQLR	BGA MICROSTAR JUNIOR	ZQL	52	1000	333.2	345.9	28.6
CDCUA877ZQLT	BGA MICROSTAR JUNIOR	ZQL	52	250	333.2	345.9	28.6

ZQL (R-PBGA-N52)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BA-2.
  - D. This package is lead-free. Refer to the 52 GQL package (drawing 4200583) for tin-lead (SnPb).

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