

# NTD5N50

Preferred Device

## Product Preview

# TMOS 7 E-FET™

## Power Field Effect Transistor

### N-Channel Enhancement-Mode Silicon Gate

This advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

#### New Features of TMOS 7

- Ultra Low On-Resistance Provides Higher Efficiency
- Reduced Gate Charge

#### Features Common to TMOS 7 and TMOS E-FETS

- Avalanche Energy Specified
- Diode Characterized for Use in Bridge Circuits
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature
- Industry Standard DPAK Surface Mount Package

#### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	500	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	500	Vdc
Gate-Source Voltage	$V_{GS}$ $V_{GSM}$	$\pm 20$	Vdc
— Continuous — Non-Repetitive ( $t_p \leq 10 \text{ ms}$ )		$\pm 40$	
Drain — Continuous	$I_D$ $I_{DM}$	5.0	Adc
— Continuous @ $100^\circ\text{C}$		3.4	
— Single Pulse ( $t_p \leq 10 \mu\text{s}$ )		18	
Total Power Dissipation Derate above $25^\circ\text{C}$ Total Power Dissipation @ $T_C = 25^\circ\text{C}$ when mounted with the minimum recommended pad size	$P_D$	96	Watts
		0.77	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 100 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $I_L = 5 \text{ A}$ , $L = 10 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	125	mJ
Thermal Resistance	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}^{(1)}$	1.30 100 71.4	$^\circ\text{C}/\text{W}$
— Junction-to-Case			
— Junction-to-Ambient			
Maximum Lead Temperature for Soldering Purposes, $1/8"$ from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

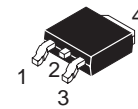
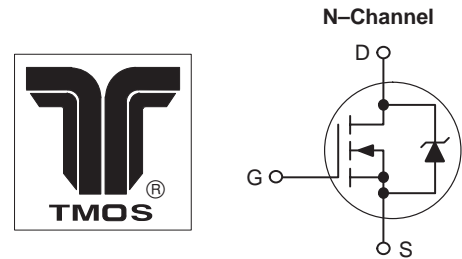
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**TMOS POWER FET**  
**5 AMPERES**  
**500 VOLTS**  
 $R_{DS(on)} = 1.7 \Omega$



**CASE 369A**  
**DPAK**  
**STYLE 2**

PIN ASSIGNMENT	
1	Gate
2	Drain
3	Source
4	Drain

#### ORDERING INFORMATION

Device	Package	Shipping
NTD5N50	DPAK	75 Units/Rail
NTD5N50T4	DPAK	2500 Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

# NTD5N50

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 0.25 mAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	500 —	— 590	— —	Vdc mV/°C
Zero Gate Voltage Collector Current (V <sub>DS</sub> = 500 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 500 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS(f)</sub> I <sub>GSS(r)</sub>	— —	— —	100 100	nAdc

### ON CHARACTERISTICS (1)

Gate Threshold Voltage I <sub>D</sub> = 0.25 mA, V <sub>DS</sub> = V <sub>GS</sub> Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0 —	2.7 6.4	4.0 —	Vdc mV/°C
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 2.5 Adc)	R <sub>DS(on)</sub>	—	1.3	1.7	Ohm
Drain-to-Source On-Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 2.5 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 5 Adc, T <sub>J</sub> = 125°C)	V <sub>DS(on)</sub>	— —	— —	10.2 8.9	Vdc
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 2.5 Adc)	g <sub>FS</sub>	2.0	4.0	—	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	520	730	pF
Output Capacitance		C <sub>oss</sub>	—	170	240	
Transfer Capacitance		C <sub>riss</sub>	—	11	20	

### SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	(V <sub>DD</sub> = 250 Vdc, I <sub>D</sub> = 5 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	7.0	10	ns
Rise Time		t <sub>r</sub>	—	9.0	20	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	20	40	
Fall Time		t <sub>f</sub>	—	10	20	
Gate Charge	(V <sub>DS</sub> = 400 Vdc, I <sub>D</sub> = 5 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>T</sub>	—	10	20	nC
		Q <sub>1</sub>	—	2.0	—	
		Q <sub>2</sub>	—	3.0	—	
		Q <sub>3</sub>	—	5.0	—	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage (1)	(I <sub>S</sub> = 5 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 5 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	— —	0.9 0.8	1.0 —	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 5 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	415	—	ns
		t <sub>a</sub>	—	100	—	
		t <sub>b</sub>	—	315	—	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	—	1.8	—	μC

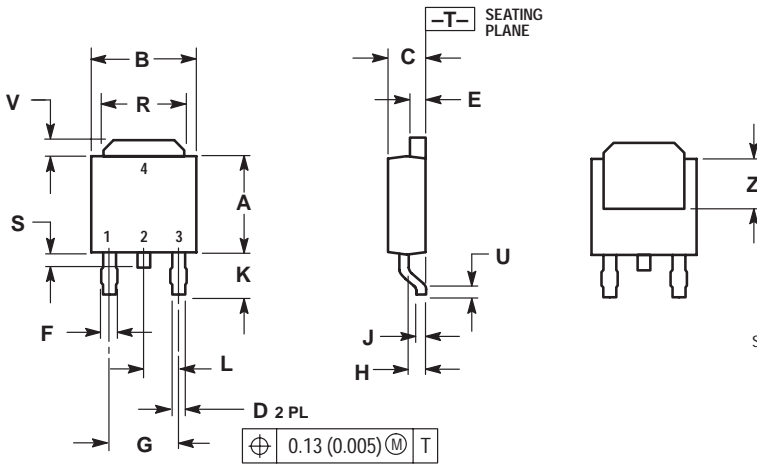
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

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## PACKAGE DIMENSIONS

### DPAK CASE 369A-13 ISSUE AA



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC	4.58 BSC		
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC	2.29 BSC		
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

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