NTD5N50

Preferred Device

Product Preview

TMOS 7 E-FET™ Power Field Effect Transistor

N–Channel Enhancement–Mode Silicon Gate

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

New Features of TMOS 7

- Ultra Low On–Resistance Provides Higher Efficiency
- Reduced Gate Charge

Features Common to TMOS 7 and TMOS E–FETS

- Avalanche Energy Specified
- Diode Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Industry Standard DPAK Surface Mount Package

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \leq 10$ ms)	 V_{GS} V_{GSM}	 ±20 ±40	Vdc
Drain — Continuous — Continuous @ 100°C — Single Pulse ($t_p \leq 10$ μs)	I_D I_D I_{DM}	5.0 3.4 18	Adc
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_C = 25°C when mounted with the minimum recommended pad size	P_D	96 0.77 1.75	Watts W/°C W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 5 A, L = 10 mH, R_G = 25 Ω)	E_{AS}	125	mJ
Thermal Resistance — Junction–to–Case — Junction–to–Ambient — Junction–to–Ambient (1)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 1.30 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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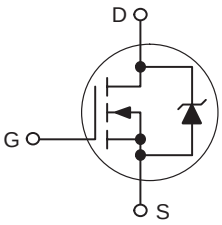
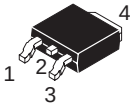
http://onsemi.com

TMOS POWER FET
5 AMPERES
500 VOLTS
$R_{DS(on)}$ = 1.7 Ω

N–Channel





CASE 369A
DPAK
STYLE 2

PIN ASSIGNMENT	
1	Gate
2	Drain
3	Source
4	Drain

ORDERING INFORMATION

Device	Package	Shipping
NTD5N50	DPAK	75 Units/Rail
NTD5N50T4	DPAK	2500 Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

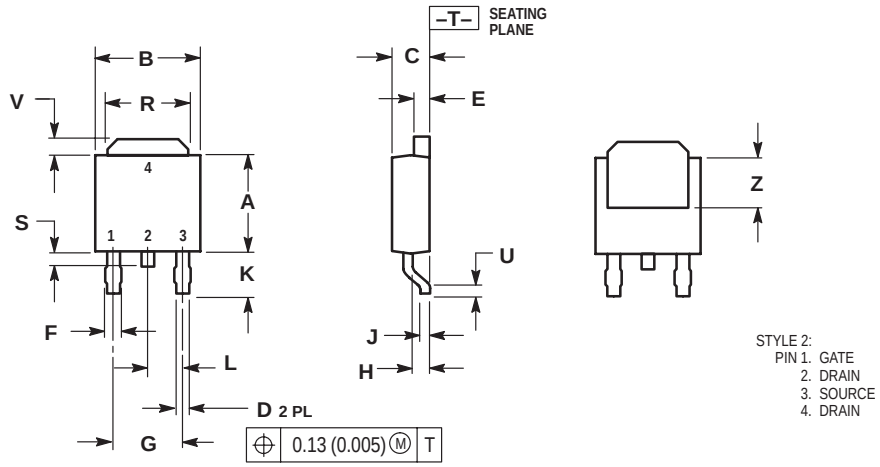
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	 500 —	 — 590	 — —	Vdc mV/°C
Zero Gate Voltage Collector Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)	I_{DSS}	 — —	 — —	 10 100	µAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)	$I_{GSS(f)}$ $I_{GSS(r)}$	— —	— —	100 100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage I_D = 0.25 mA, V_{DS} = V_{GS} Temperature Coefficient (Negative)	$V_{GS(th)}$	 2.0 —	 2.7 6.4	 4.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	$R_{DS(on)}$	—	1.3	1.7	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2.5 Adc) (V_{GS} = 10 Vdc, I_D = 5 Adc, T_J = 125°C)	$V_{DS(on)}$	 — —	 — —	 10.2 8.9	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.5 Adc)	g_{FS}	2.0	4.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	520	730	pF
Output Capacitance		C_{oss}	—	170	240	
Transfer Capacitance		C_{rss}	—	11	20	
SWITCHING CHARACTERISTICS (2)					
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 5 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	7.0	10	ns
Rise Time		t_r	—	9.0	20	
Turn–Off Delay Time		$t_{d(off)}$	—	20	40	
Fall Time		t_f	—	10	20	
Gate Charge	(V_{DS} = 400 Vdc, I_D = 5 Adc, V_{GS} = 10 Vdc)	Q_T	—	10	20	nC
		Q_1	—	2.0	—	
		Q_2	—	3.0	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (1)	(I_S = 5 Adc, V_{GS} = 0 Vdc) (I_S = 5 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.9 0.8	 1.0 —	Vdc
Reverse Recovery Time	(I_S = 5 Adc, V_{GS} = 0 Vdc, di_S/dt = 100 A/µs)	t_{rr}	—	415	—	ns
		t_a	—	100	—	
		t_b	—	315	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.8	—	µC

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS

DPAK
CASE 369A–13
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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