CMOS 4-Stage Parallel In/Parallel Out Shift Register

with J-K Serial Inputs and True/ Complement Outputs

Features:

- 4-Stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Static flip-flop operation; Master-slave configuration
- Reset control
- Buffered outputs
- Low power dissipation — 5μW typ. (ceramic)
- High speed — to 5 MHz
- Quiescent current specified to 15 V
- Maximum input leakage current of 1μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

The RCA-CD4035A is a four-stage clocked signal serial register with provision for SYNCHRONOUS PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry via the D line of each register stage is permitted only when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

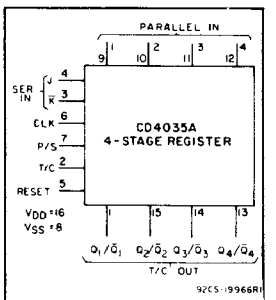
When the TRUE/COMPLEMENT control is high, the TRUE contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal.

J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications

- **Counters, Registers**
  Arithmetic-unit registers
  Shift left — shift right registers
  Serial-to-parallel/parallel-to-serial conversions
- **Sequence generation**
- **Control circuits**
- **Code conversion**



CD4035A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −66 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). 100mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5V

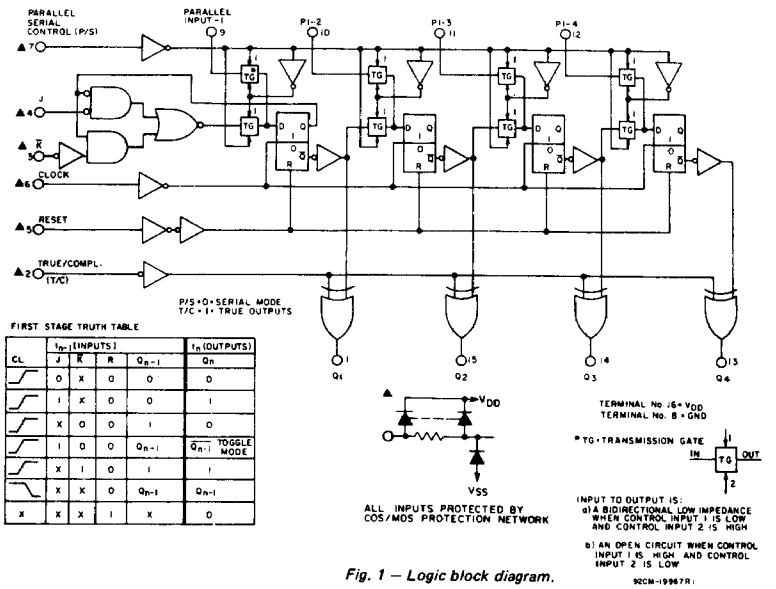
LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, except as noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package-Temperature Range		3	12	3	12	V
Data Setup Time, t_S:						
J/$\overline{K}$ Lines	5	500	–	750	–	ns
	10	200	–	250	–	
Parallel-In Lines	5	350	–	500	–	
	10	80	–	100	–	
Clock Pulse Width, t_W	5	335	–	500	–	ns
	10	165	–	250	–	
Clock Rise and Fall Time, t_rCL,t_fCL	5	–	15	–	15	µs
	10	–	5	–	5	
Reset Pulse Duration, t_W	5	400	–	500	–	ns
	10	175	–	200	–	

CD4035A Types



FIRST STAGE TRUTH TABLE

CL	t_{n-1} (INPUTS) J	K	R	Q_{n-1}	t_n (OUTPUTS) Q_n
⎍⎍	0	X	0	0	0
⎍⎍	1	X	0	0	1
⎍⎍	X	0	0	1	0
⎍⎍	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⎍⎍	X	1	0	1	1
⎍⎍	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

Fig. 1 – Logic block diagram.

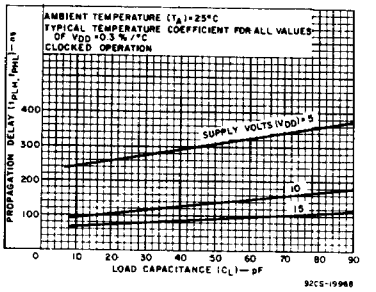


Fig. 2 – Typical propagation delay time vs. load capacitance.

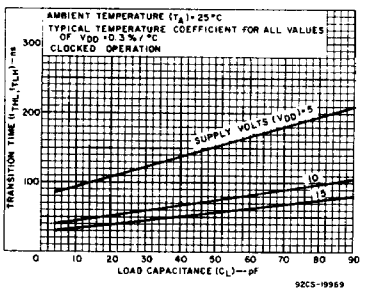


Fig. 3 – Typical transition time vs. load capacitance.

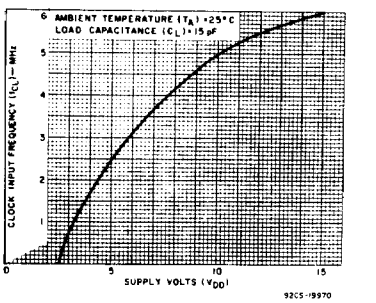


Fig. 4 – Typical clock input frequency vs. supply voltage.

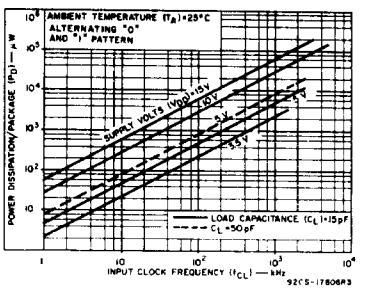


Fig. 5 – Typical dynamic power dissipation characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) D, F, K, H PACKAGES -55	+25 TYP.	+25 LIMIT	+125	E PACKAGE -40	+25 TYP.	+25 LIMIT	+85	UNITS
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	µA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink),	0.5	–	5	0.62	1	0.5	0.35	0.43	1	0.35	0.24	mA
I_DN Min.	0.5	–	10	1.55	2.5	1.25	0.87	1.05	2.5	0.85	0.59	
P-Channel (Source):	4.5	–	5	-0.31	-0.5	-0.25	-0.17	-0.2	-0.5	-0.18	-0.12	
I_DP Min.	9.5	–	10	-0.81	-1.3	-0.65	-0.45	-0.56	-0.31	-0.45	-0.31	
Input Leakage Current,	Any Input											µA
I_{IL}, I_{IH}	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								