High-Speed CMOS 4K x 9 Clocked FIFO with Output Enable

QS7244A

FEATURES/BENEFITS

- Clocked interface FIFOs for high-speed systems
- Data and flags change on rising edge of clocks
- Fully asynchronous read and write
- TTL compatible input and output levels
- Very low power
- Coincidental or different read/write clocks
- 66-MHz cycle time
- Depth and width expandable
- Registered flow-through architecture
- Asynchronous output enable
- Noise filters on input control lines
- Available in 32-pin PLCC & 28-pin SOJ packages

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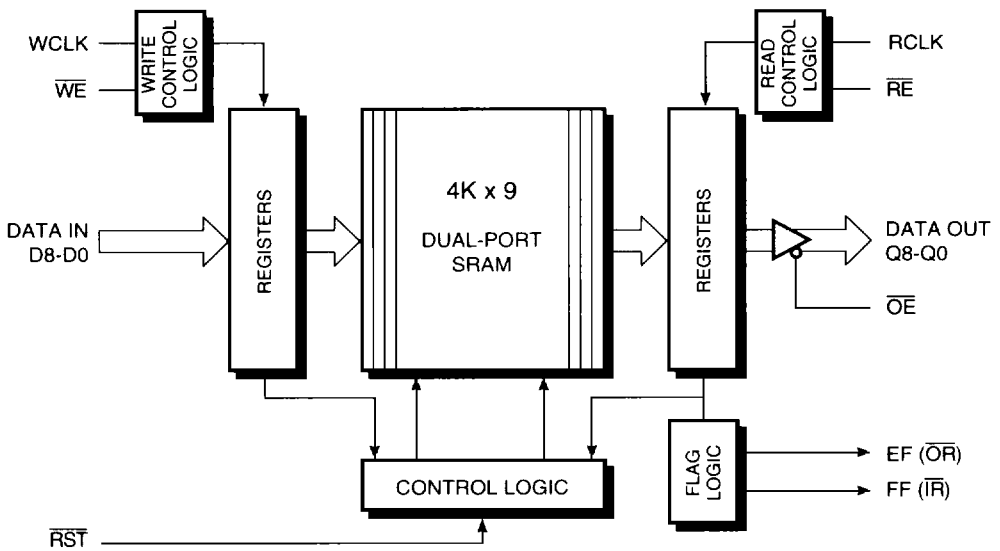
DESCRIPTION

The QS7244A is a 4K x 9 clocked or synchronous FIFO. It has independent clocked interfaces for both read and write, which minimize the potential for noise on the read and write to false trigger and incorrectly advance the pointers. Additional read/write circuitry makes interfacing at high speed much easier as no pulse shaping is required. The part also has an Empty and Full flag EF and FF which can be looked upon as input ready and output ready ($\overline{IR}$ and $\overline{OR}$) for those who are familiar with that nomenclature. An output enable is provided to allow the part to be tristated. This part can be used in high-speed datacomms, data compression, image processing and graphics systems.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



OPERATIONAL DESCRIPTION

These interfaces provide high-speed data buffering in system designs and allow symmetrical clocks at speeds to 66 MHz. The clocks are controlled by read and write enable lines. Write Enable and write data are accepted at the rising edge of the write clock. Read enable is accepted at the rising edge of the read clock and read data changes after the read clock edge. Flag changes occur after either the write clock edge or the read clock edge, depending on the operation being performed. This FIFO uses a dual-port RAM-based architecture with independent read and write pointers. These pointers are set to zero by the reset pulse, creating an empty condition. A Write Enable causes data to be written and the write pointer to be incremented by the rising edge of the write clock. If the FIFO is empty, the write data will flow directly to the outputs, and the empty flag will be cleared to indicate the output data is valid. A Read Enable will cause the read pointer to be incremented to the next word on the rising edge of the read clock. If there is only one word in the FIFO, the Empty flag will be set by this same rising edge. The flag circuitry is based on a reliable sequential design giving precise full and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty.

PIN DESCRIPTIONS

Name	I/O	Description
D	I	Data Inputs
Q	O	Data Outputs
RCLK	I	Read Clock
$\overline{RE}$	I	Read Enable
WCLK	I	Write Clock
$\overline{WE}$	I	Write Enable
$\overline{RS}$	I	Reset
EF($\overline{OR}$)	O	Empty Fag
FF ($\overline{IR}$)	O	Full Flag
$\overline{OE}$	I	Output Enable

FIGURE 2. 32-PIN PLCC PINOUT

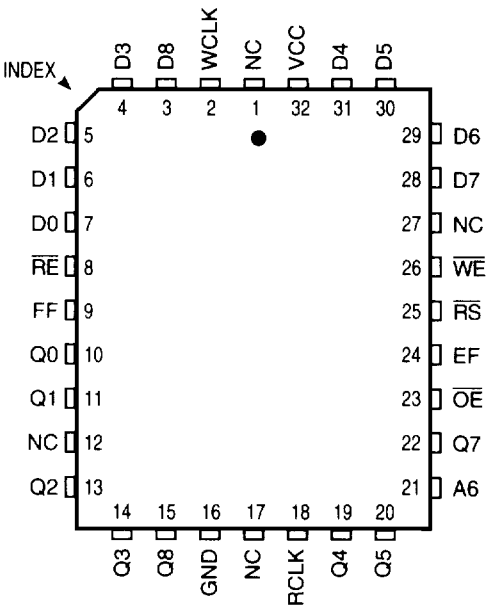
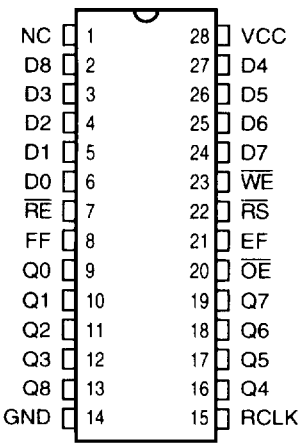


FIGURE 3. 28-PIN SOJ PINOUT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5 to 7.0V
DC Output Voltage V_{OUT}	–0.5 to V_{CC} +0.5V
DC Input Voltage V_{IN}	–0.5 to V_{CC} +0.5V
AC Input Voltage (Pulse Width ≤ 20 ns)	–3.0V
DC Input Diode Current with V_{IN} < 0	–20 mA
DC Output Diode Current with V_{OUT} < 0	–50 mA
DC Output Current with V_{OUT} > V_{CC}	50 mA
DC Output Current Max Sink Current/Pin	+70 mA
DC Output Current Max Source Current/Pin	–30 mA
Total DC Ground Current	(N x I_{OL} + M x ΔI_{CC}) mA
Total DC V_{CC} Power Supply Current	(N x I_{OH} + M x ΔI_{CC}) mA
N = Number of outputs, M = Number of inputs	
Maximum Power Dissipation	
T_{STG} Storage Temperature	–65°C to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device, resulting in functional- or reliability-type failures.

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CAPACITANCE

T_A = 25°C, f = 1.0 MHz JR Package

Name	Description	Conditions	Typ	Max	Units
C_{IN}/C_{OUT}	Input Capacitance	V_{IN} = 0V, f = 1 MHz	5	8	pF

Note: Capacitance is guaranteed but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

T_A = 25°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage	Logic HIGH for All Conditions	2.0	6.0	V
V_{IL}	Input LOW Voltage	Logic LOW for All Conditions	—	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{CC} = Min	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA, V_{CC} = Min	—	0.4	V
$\lvert I_{IL} \rvert$	Input Leakage	V_{CC} = Max, GND < V_{IN} < V_{CC}	—	5	µA
$\lvert I_{OZ} \rvert$	Output Leakage	V_{CC} = 5.5V, V_{OUT} = Vcc or 0V	—	10	µA

POWER SUPPLY CHARACTERISTICS

T_A = 25°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Cycle Time (ns) -15	-20	-25	-30	-40	Units
I_{CC1}	Operating Current V_{CC} = Max, Outputs Open $\overline{RE}$ = $\overline{WE}$ = V_{IL}, f = f_{MAX}	165	150	140	140	135	mA
I_{CC2}	Standby Current $\overline{RE}$ = $\overline{WE}$ = $\overline{RS}$ = V_{CC} – 2.0V Clocks Free Running	15	15	15	15	15	mA

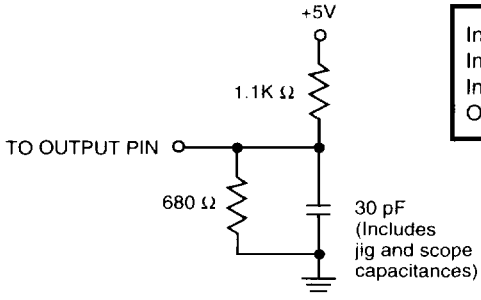
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

V_{CC} = 5V ± 10%, Commercial T_A = 0°C to +70°C

Symbol	Parameter	-15	-20	-25	-30	Units	Type
f_{RC}, f_{WC}	Read or Write Clock, MHz[2]	66.7	50	40	33	MHz	Max
t_{RC}, t_{WC}	Read or Write Cycle Time	15	20	25	30	ns	Min
t_{CW}	Read or Write Clock HIGH or LOW[1]	7	8	10	12	ns	Min
t_S	Setup Time	5	5	6	10	ns	Min
t_H	Hold Time	0	0	0	0	ns	Min
t_{CF}	Clock to Flag Valid Output Delay	7	8	9	10	ns	Max
t_{CD}	Clock to Data Valid Output Delay	9	10	11	12	ns	Min
t_{RS}	Reset Pulse Width[1]	8	10	15	17	ns	Min
t_{EFL}, t_{FFL}	Flag Latency, $\overline{RE} \rightarrow$ EF, $\overline{WE} \rightarrow$ FF[4]	17	18	20	22	ns	Min
t_{OE}	Output Enable to Data Valid	5	6	7	8	ns	Min
t_{OLZ}	Output Enable LOW to Low-Z[2]	2	2	2	2	ns	Min
t_{RSR}	Reset Recovery Time	7	8	10	12	ns	Min
t_{OHZ}	Output Enable HIGH to High-Z[2]	8	9	10	12	ns	Max

Notes: These timings are measured as defined in AC Test Conditions.
1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested.
3. Minimum time to write clock edge for valid write enable to be accepted.
4. Time required from write clock edge to read clock edge for write to turn off empty on next clock. Time required from read clock edge to write clock edge for read to turn off full on next clock.
5. Transition to Hi-Z is measured ± 200 mV from prior steady-state voltage.

FIGURE 4. AC TEST CONDITIONS

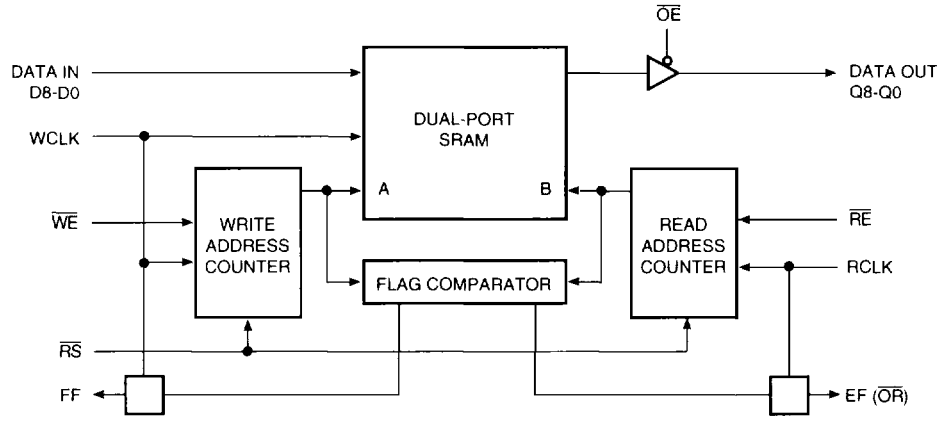


Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

OPERATIONAL DESCRIPTION

The 7244A Clocked FIFO consists of a dual-port RAM, read and write address counters, a flag comparator, and synchronizing flip-flops for the flags. A simplified block diagram of the 7244A Clocked FIFO is shown on page 3-7. Note that the internal design of the 7244A Clocked FIFO is more complex than shown for maximum performance. The simplified block diagram shown is provided for understanding the operation of the FIFO. For detailed timing information, refer to the switching characteristics and timing diagrams.

FIGURE 5. CLOCKED FIFO SIMPLIFIED BLOCK DIAGRAM



The dual-port RAM is a static RAM with two independent sets of addressing logic. Each set of addressing logic can simultaneously and independently address words in the RAM. Each combination of addressing logic and its associated data I/O is called a port, hence the name dual-port RAM. In the FIFO, one port is used only for writing and one port only for reading. If both ports have the same address and data is written by one port, the same data will be read immediately by the other port. The data is said to flow through the RAM.

The read and write address counters address the read and write ports of the dual-port RAM. Each is a binary counter that increments on the rising edge of the clock, and is enabled for counting by a low active enable signal. These counters are asynchronously reset by a reset pulse.

Data is written into the dual-port RAM when each write clock validated by a $\overline{WE}$ increments the write address pointer. If the FIFO is empty, data from the write port will flow through to the read port following three write clock pulses (fall-through mode). No $\overline{RE}$ is necessary to present the first word onto the outputs. Subsequent RCLKs validated by $\overline{RE}$ are needed to update the read pointer and output subsequent data words. The "flow-through" of this initial data word happens regardless of the state of the $\overline{RE}$ input.

The flag comparator continuously compares the contents of the two address counters. If the contents of the two address counters are equal, the FIFO is empty, and the Empty flag is active. This is the case immediately after a reset pulse when both counters have been reset to zero. If the write address counter value is equal to the read address counter value plus the depth of the RAM (e.g., 4096 for a 4K x 9 FIFO), the FIFO is full, and the Full flag is active. The flag outputs from the flag comparator are synchronized in flip-flops by the appropriate read or write clocks, so they change only following the rising edge of a clock.

Read and write enable are inhibited by the Empty and Full flags, respectively. If the FIFO is empty, read enable is inhibited because there is no next word in the FIFO to step to. If the FIFO is full, both the write enable and the write clock to the dual-port RAM are inhibited because there is no place available to write another word. (The gates corresponding to these read and write enable inhibits are not shown on the simplified block diagram.) Note that when there is one word in the FIFO, read enable is allowed because the FIFO is stepping to another word. Write enable and read enable can be considered as "write current word" and "read next word," respectively.

The general operation of the 7244A Clocked FIFO is shown in the following timing diagrams.

TIMING DIAGRAMS

FIGURE 6. SINGLE-READ OPERATION TIMING

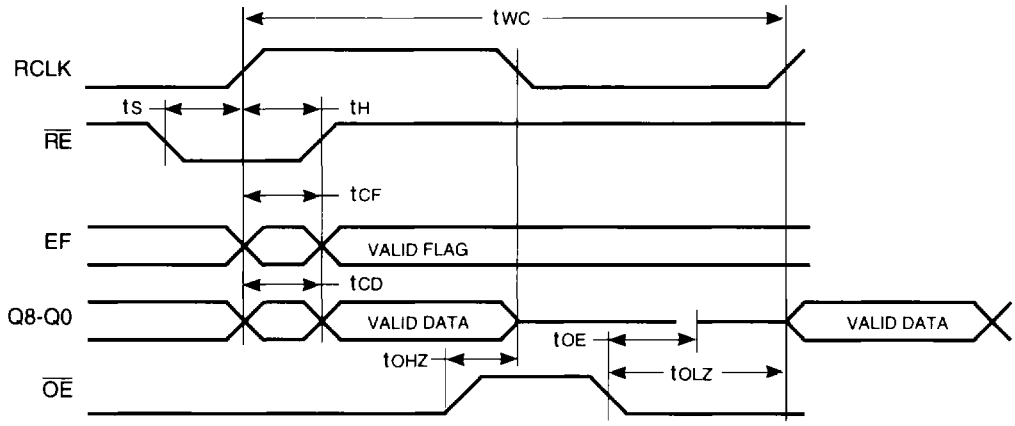


FIGURE 7. WRITE OPERATION TIMING

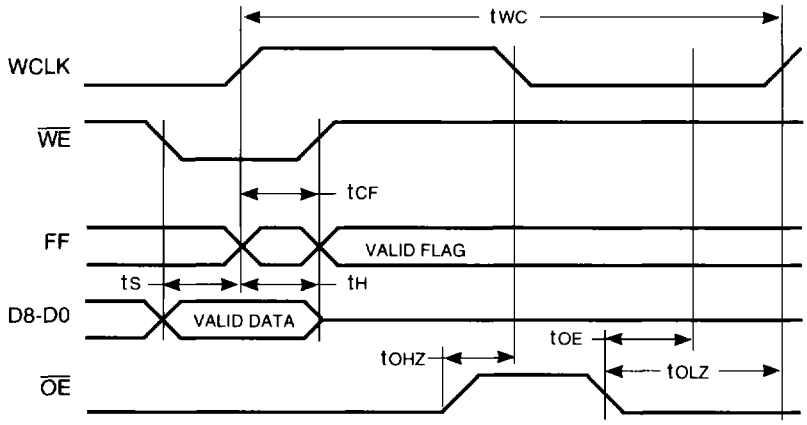
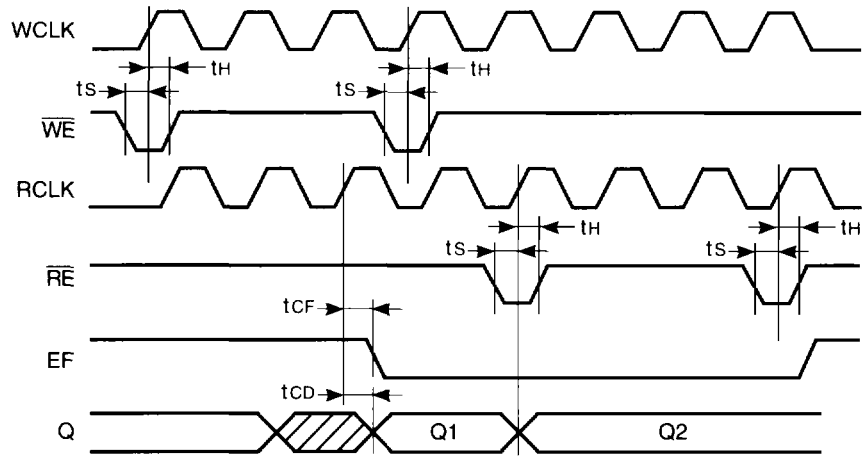
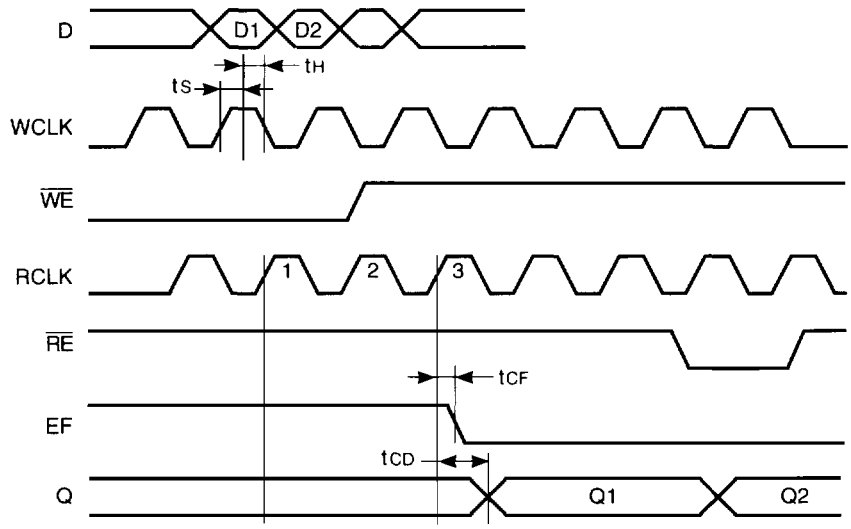


FIGURE 8. OPERATION WITH NO SKEW VIOLATION



Note: Normal operation with no skew violation on the Empty flag boundary.

FIGURE 9. FLOW-THROUGH LATENCY TIMING

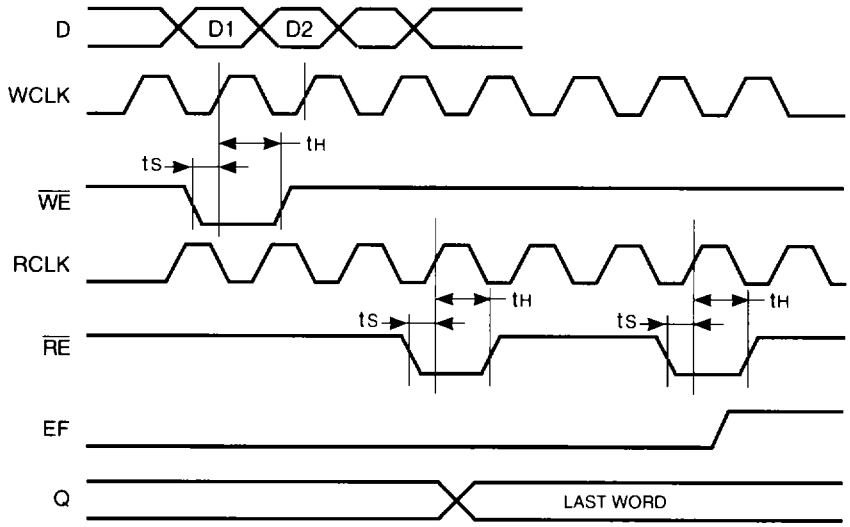


7244A FIRST WORD FALL-THROUGH

Note: Normal operation with no skew violation on the Empty flag boundary.

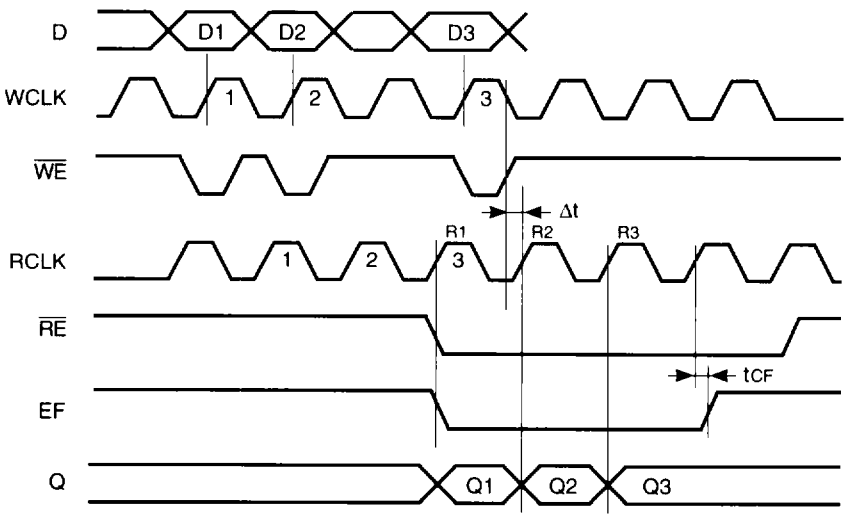
Following a three-read clock latency, valid data appears on the output bus and EF is updated. Under non-t_{SKEW} violations, the EF and the first data word will come out relative to the third read clock. The second data word written in the same cycle (the cycle in which EF goes LOW) will be available when $\overline{RE}$ goes LOW with no latency.

FIGURE 10. LAST-WORD READ OPERATION



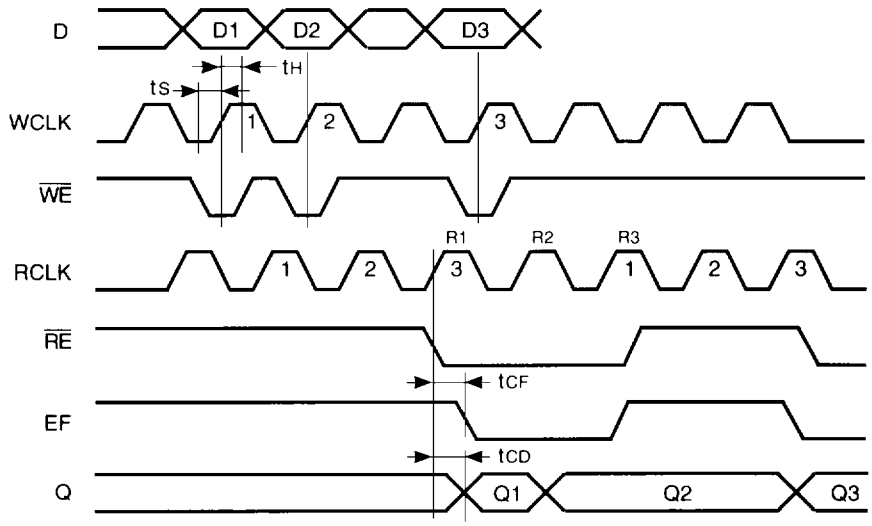
When the last word is read, valid data appears on the output bus. $\overline{RE}$ must be asserted again to update the EF, which will inhibit further reads from the FIFO. This can occur no sooner than one cycle after the last read.

FIGURE 11. THREE WRITES AND THREE READS WITH ASYNCHRONOUS CLOCKS



If the Δt between the falling edge of WCLK3 and the rising edge of R2 is not violated, the 7244A will ouput all three words continuously.

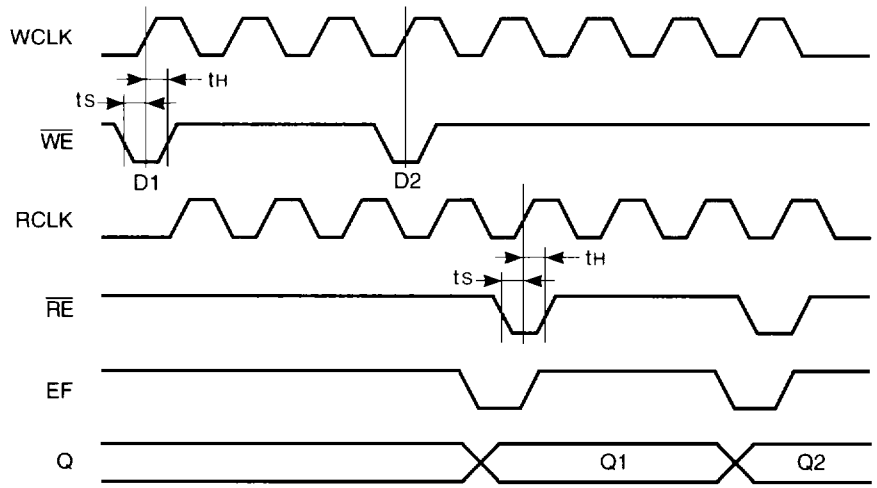
FIGURE 12. THREE WRITES AND THREE READS WITH ASYNCHRONOUS CLOCKS — $f_{WCLK} < f_{RCLK}$ Δt



If the Δt between the falling edge of WCLK3 and the rising edge of RCLK2 is violated, the 7244A will not have enough time to process data word three. Therefore, the 7244A will assert the EF at the next RCLK and the third data word will take another three-clock latency to output. ($\overline{RE}$ not needed to output this word). Word 3 is not lost and is still in sync with EF.

Under this condition, the EF and the first data word will come out relative to the fourth read clock. If a second write operation occurs within the same cycle, the EF will go HIGH when the next $\overline{RE}$ goes LOW. EF will then go LOW with the second data word after another latency of four cycles.

FIGURE 13. t_{SKEW} ON BOUNDARY CONDITIONS



In this condition, the latency is at the boundary between meeting and violating the skew timing. The EF and first data word behave the same as the example above, except the second data word appears with no additional latency.

FIGURE 14. FULL FLAG BOUNDARY

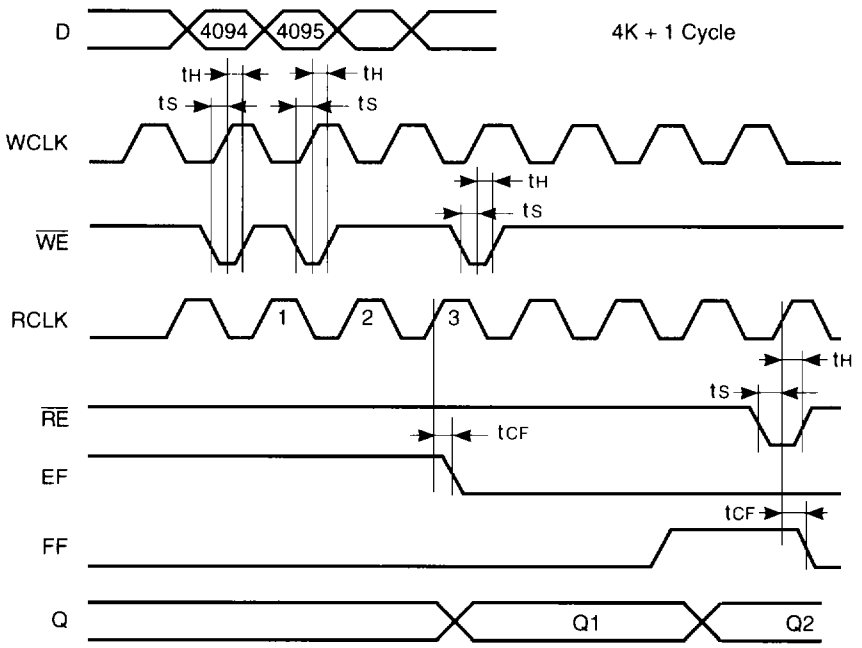
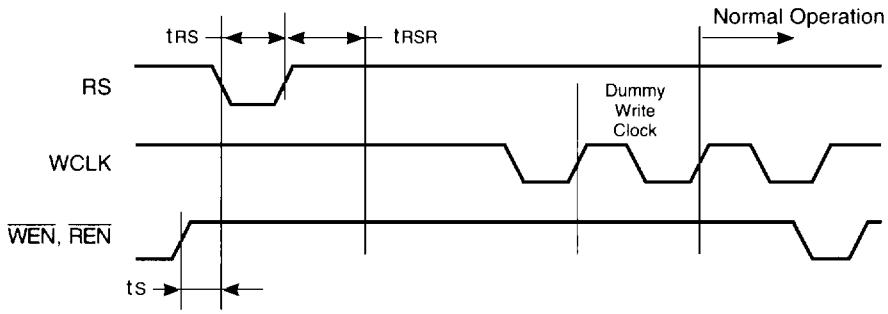


FIGURE 15. RESET OPERATION



After a reset cycle, one dummy write clock is required before the FIFO can resume normal operation.

ORDERING INFORMATION

Example:

QS72 44A - 15 JR

Specialty Memory Product Prefix
(QS72)

Part Number
44A (4Kx 9)

Package
JR (32-Pin PLCC)
V (28-Pin SOJ)

Speed
-15 ns
-20 ns
-25 ns
-30 ns