

# 128K x 8 Static RAM

## Features

- **High speed**  
—  $t_{AA} = 12 \text{ ns}$
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options**
- **Functionally equivalent to CY7C1019**
- **Available in Pb-free and non Pb-free 32-pin TSOP II, non Pb-free 400-mil-wide SOJ packages.**

## Functional Description

The CY7C1019B is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory

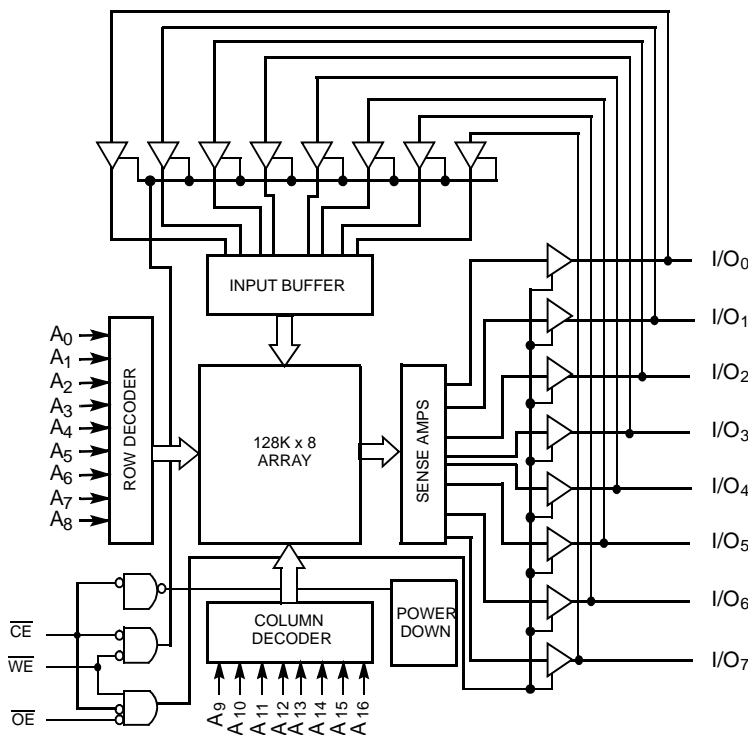
expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

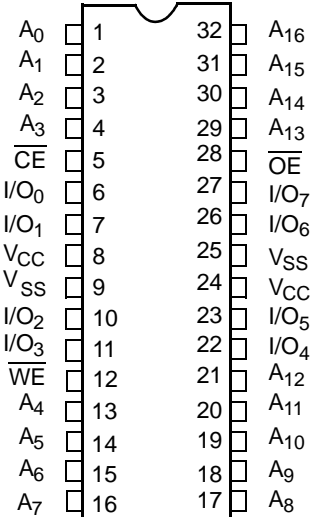
The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

## Logic Block Diagram



## Pin Configurations

### SOJ /TSOPII Top View



## Selection Guide

	-12	-15	Unit
Maximum Access Time	12	15	ns
Maximum Operating Current	140	130	mA
Maximum Standby Current	10	10	mA

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....-65°C to +150°C  
 Ambient Temperature with Power Applied.....-55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> .....-0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[1]</sup>.....-0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

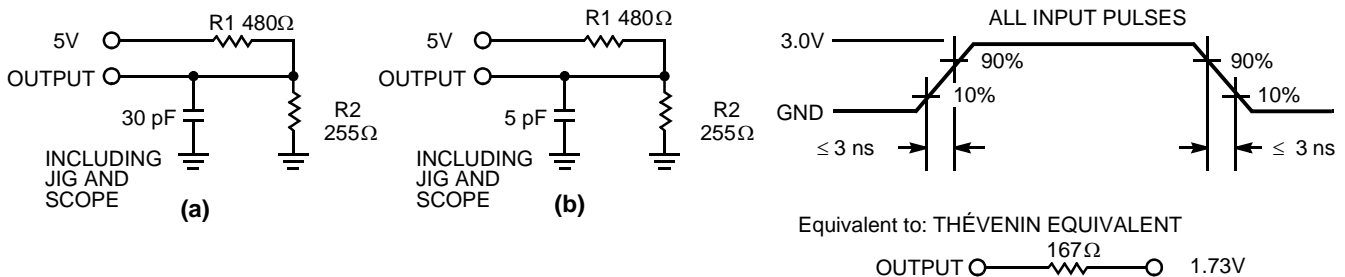
**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	-12		-15		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = - 4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		140		130	mA
I <sub>SB1</sub>	Automatic CE Power- Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40		40	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		10		10	mA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 5.0V		

**AC Test Loads and Waveforms**



**Notes:**

1. V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
2. T<sub>A</sub> is the "Instant On" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

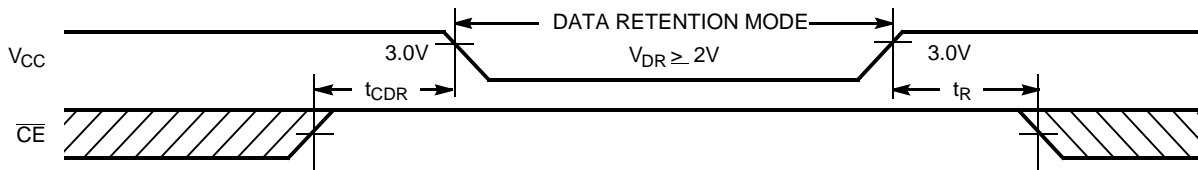
**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

Parameter	Description	-12		-15		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	12		15		ns
t <sub>AA</sub>	Address to Data Valid		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		6		7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		6		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		6		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15	ns
<b>Write Cycle<sup>[7, 8]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	9		10		ns
t <sub>AW</sub>	Address Set-Up to Write End	8		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	8		10		ns
t <sub>SD</sub>	Data Set-Up to Write End	6		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		6		7	ns

**Notes:**

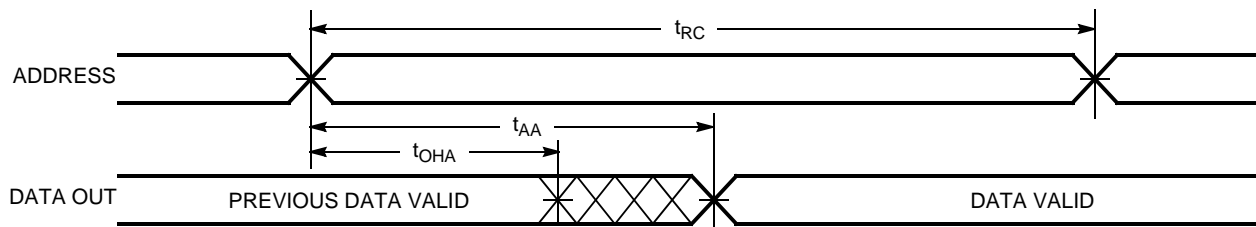
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
5. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
7. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. The minimum write cycle time for Write Cycle no. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Data Retention Waveform**

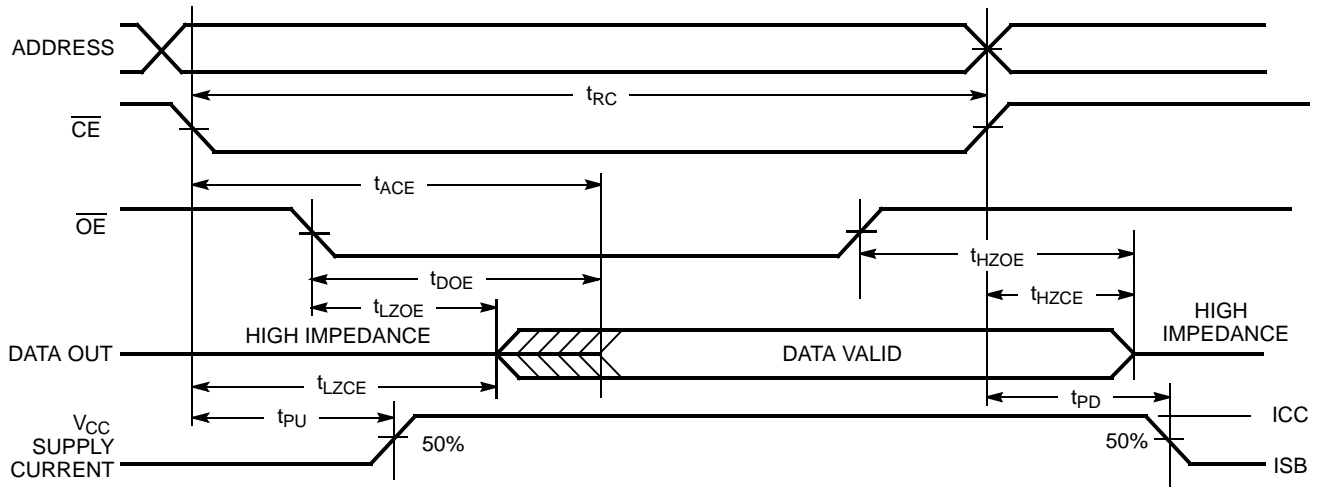


**Switching Waveforms**

**Read Cycle No. 1<sup>[9, 10]</sup>**



**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[10, 11]</sup>**

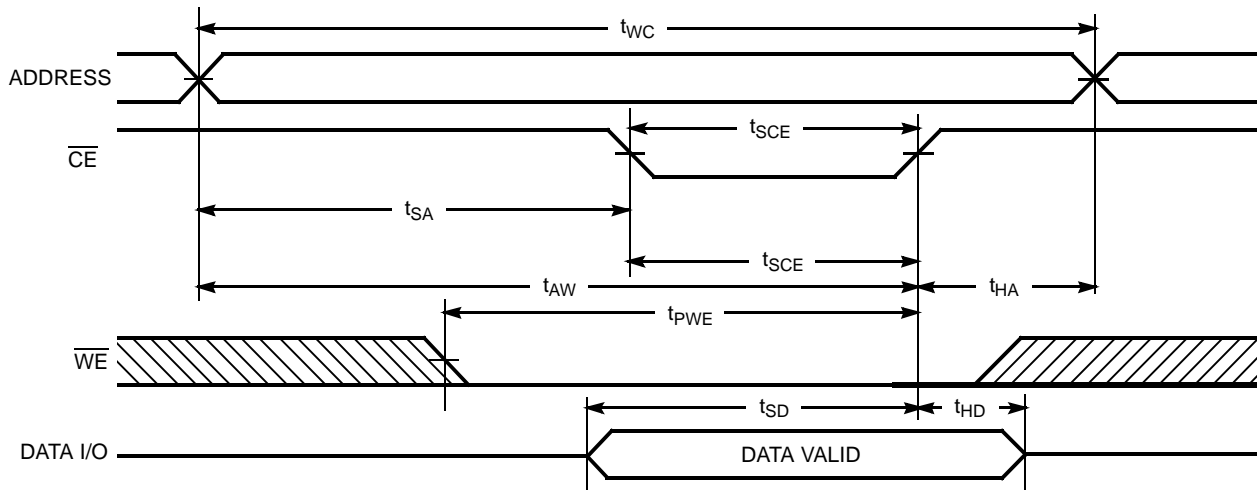


**Notes:**

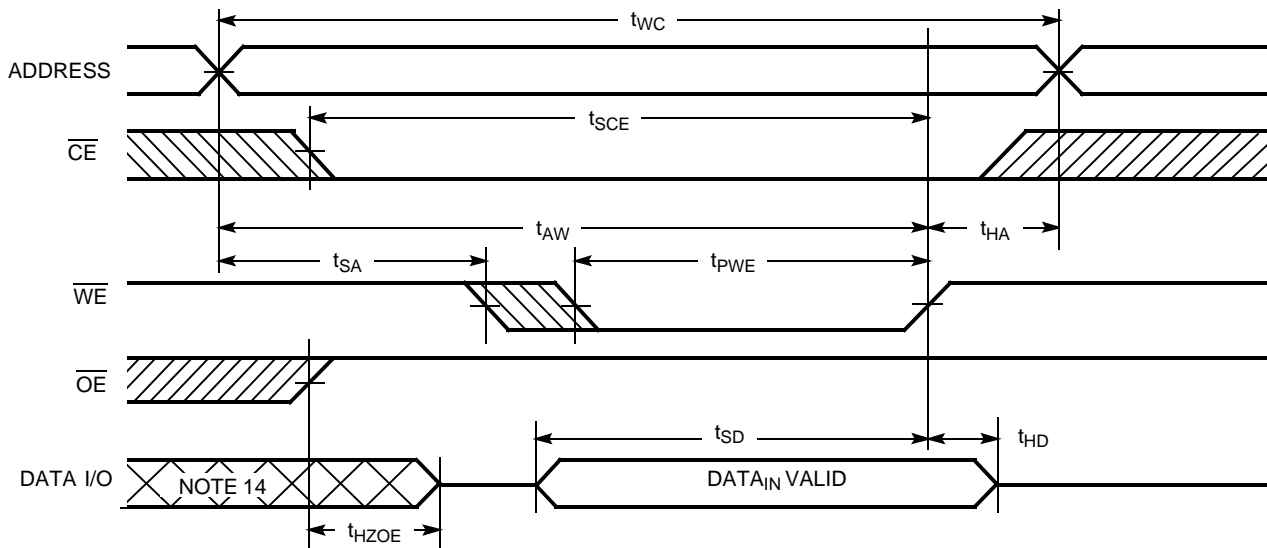
- 9. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
- 10.  $\overline{WE}$  is HIGH for read cycle.
- 11. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[12, 13]</sup>



Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[12, 13]</sup>

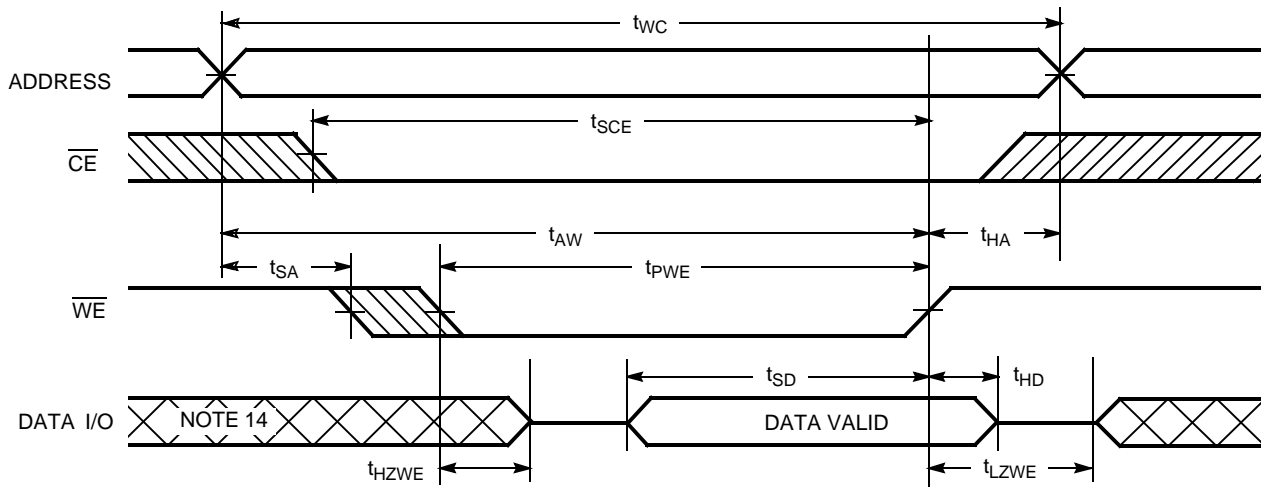


Notes:

- 12. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 13. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[13]</sup>



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

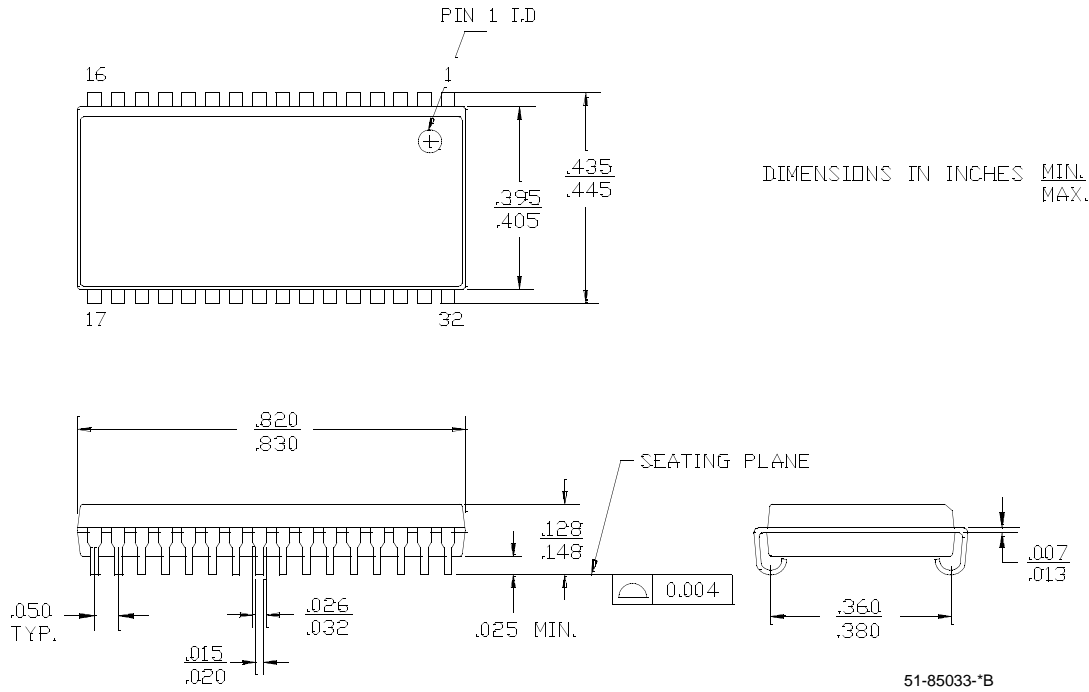
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1019B-12VC	51-85033	32-pin 400-Mil Molded SOJ	Commercial
	CY7C1019B-12ZC	51-85095	32-pin TSOP Type II	
	CY7C1019B-12ZXC		32-pin TSOP Type II (Pb -Free)	
15	CY7C1019B-15VC	51-85033	32-pin 400-Mil Molded SOJ	Commercial
	CY7C1019B-15ZXC	51-85095	32-pin TSOP Type II (Pb -Free)	

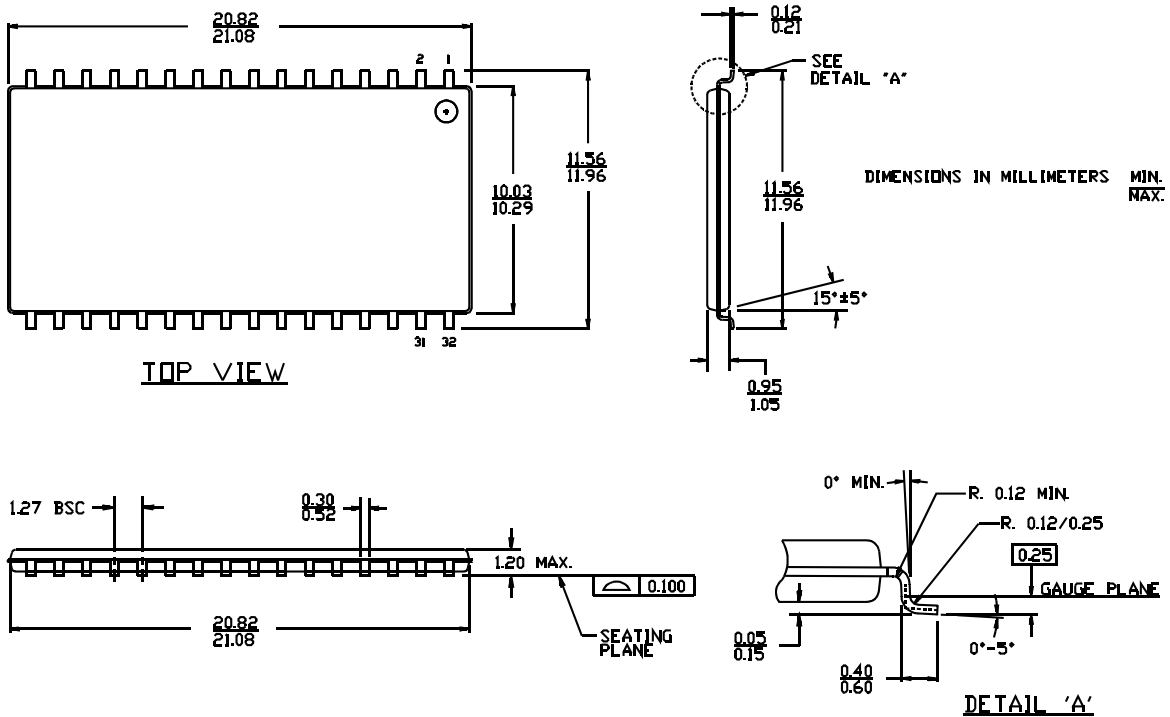
Please contact local sales representative regarding availability of these parts

Package Diagrams

32-pin (400-mil) Molded SOJ (51-85033)



32-pin TSOP II (51-85095)



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**Document History Page**

Document Title: CY7C1019B 128K x 8 Static RAM Document Number: 38-05026				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109949	09/25/01	SZV	Change from Spec number: 38-01115 to 38-05026
*A	116170	08/14/02	HGK	1. SOJ (400-mil) package outline replacing incorrect SOJ package 2. Pin for pin compatible with CY7C1019 3. Industrial packages added to Ordering Information
*B	397875	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Updated the Ordering Information Table on page # 6
*C	493543	See ECN	NXR	Removed CY7C10191B from product offering Removed Industrial Operating Range Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed $I_{OS}$ parameter from DC Electrical Characteristics table Updated Ordering Information table