## Datasheet

## PART NUMBER

## 54LS126ABCA-ROCS

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
- Class Q Military
- Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.
Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

## MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR, LOW-POWER SCHOTTKY TTL, QUADRUPLE BUS BUFFER GATES WITH THREE STATE OUTPUTS, MONOLITHIC SILICON

Inactive for new design after 18 April 1997.
This specification is approved for use by all Departments and Agencies of the Department of Defense.

## 1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, low-power Schottky TTL, quadruple bus buffer gates with three state outputs. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3).
1.2 Part number. The part number should be in accordance with MIL-PRF-38535, and as specified herein.
1.2.1 Device types. The device types should be as follows:

| Device type | $\underline{\text { Circuit }}$ |
| :--- | :--- |
| 01 | Quadruple bus buffer gate (inverting control input) |
| 02 | Quadruple bus buffer gate (noninverting control input) |

1.2.2 Device class. The device class should be the product assurance level as defined in MIL-PRF-38535.
1.2.3 Case outlines. The case outlines should be as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
| :---: | :---: | :---: | :---: |
| A | GDFP5-F14 or CDFP6-F14 | 14 | Flat pack |
| C | GDIP1-T14 or CDIP2-T14 | 14 | Dual-in-line |
| D | GDFP1-F14 or CDFP2-F14 | 14 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43216-5000, by using the self addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

### 1.3 Absolute maximum ratings.

| Supply voltage range | V dc to +7.0 V d |
| :---: | :---: |
| Input voltage range | -1.5 V dc at -18 mA to +5.5 V dc |
| Storage temperature range | $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$ |
| Maximum power dissipation, ( $\mathrm{PD}^{\text {) 1/ }}$ |  |
| Device type 01. | 110 mW dc |
| Device type 02. | 121 mW dc |
| Lead temperature (soldering, 10 seconds) | $+300^{\circ} \mathrm{C}$ |
| Thermal resistance, junction to case ( $\theta_{\mathrm{Jc}}$ ): |  |
| Cases A, C, D, and 2 ........................ | (See MIL-STD-1835) |
| Junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) ${ }^{\text {/ }}$ | $+175^{\circ} \mathrm{C}$ |

### 1.4 Recommended operating conditions.

Low level output current (loL) .................................................................. 12 mA maximum
High level output current (loн) .............................................................. -1.0 mA maximum

2. APPLICABLE DOCUMENTS

### 2.1 Government documents.

2.1.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Departments of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

## SPECIFICATION

## department of defense

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

## STANDARDS

## DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines
(Unless otherwise indicated, copies of the above specifications and standards are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)
2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Must withstand the added $P_{D}$ due to short-circuit test (e.g., los).
2/ Maximum junction temperature shall not be exceeded except in accordance with allowable short duration burn-in screening condition in accordance with MIL-PRF-38535.

## 3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).
3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.
3.3.1 Terminal connections and logic diagrams. The terminal connections and logic diagrams shall be as specified on figure 1 .
3.3.2 Truth tables. The truth tables shall be as specified on figure 2.
3.3.3 Schematic circuits. The schematic circuits shall be_maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.
3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.
3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).
3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.
3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.
3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.
3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 9 (see MIL-PRF-38535, appendix A).

## 4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.
4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:
a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

### 4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).
4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:
a. Tests shall be as specified in table II herein.
b. Subgroups $4,5,6,7$, and 8 shall be omitted.
4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.
4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:
a. End-point electrical parameters shall be as specified in table II herein.
b. Subgroups 3 and 4 shall be added to the group $C$ inspection parameters for class $B$ devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group $A$.
c. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.
4.5 Methods of inspection. Methods of inspection shall be specified and as follows.
4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

MIL-M-38510/323D
TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/$-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C}$ | Device types | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| Input clamp voltage | $V_{\text {IC }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{I}_{\mathrm{IN}}=-18 \mathrm{~mA}, \\ & \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C} \end{aligned}$ | 01, 02 |  | -1.5 | V |
| High level output voltage | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.7 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IH}}=2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=-1 \mathrm{~mA} \end{aligned}$ | 01, 02 | 2.4 |  | V |
| Low level output voltage | $\mathrm{V}_{\mathrm{OL}}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2.0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IL}}=0.7 \mathrm{~V}, \mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA} \end{aligned}$ | 01, 02 |  | 0.4 | V |
| Off state (high impedance state) output current | $\mathrm{l}_{\text {(off) } 1}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=2.4 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IL}}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2.0 \mathrm{~V} \end{aligned}$ | 01, 02 |  | 20 | $\mu \mathrm{A}$ |
| Off state (high impedance state) output current | $\mathrm{l}_{\mathrm{O} \text { (off) } 2}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=0.4 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IL}}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2.0 \mathrm{~V} \end{aligned}$ | 01, 02 |  | -20 | $\mu \mathrm{A}$ |
| High level input current (all inputs) | $\mathrm{I}_{\mathrm{H} 1}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2.7 \mathrm{~V}$ | 01, 02 |  | 20 | $\mu \mathrm{A}$ |
| High level input current (all inputs) | $\mathrm{I}_{1+2}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=5.5 \mathrm{~V}$ | 01, 02 |  | 100 | $\mu \mathrm{A}$ |
| Low level input current at control input | $\mathrm{I}_{\text {LL1 }}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IL}}=0.4 \mathrm{~V}$ | 01, 02 | 0 | -400 | $\mu \mathrm{A}$ |
| Low level input current at data input (control high) (circuit A only) | $\mathrm{I}_{\text {IL2 }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IL}}=0.4 \mathrm{~V} \end{aligned}$ | 01 |  | -40 | $\mu \mathrm{A}$ |
| Low level input current at data input (control low) (circuit A and B only) | $\mathrm{I}_{\text {LL2 }}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ <br> Control: $\mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}$ <br> Data: $\mathrm{V}_{\mathrm{IL}}=0.4 \mathrm{~V}$ | 02 |  | -40 | $\mu \mathrm{A}$ |
| Low level input current at data input (control low) | ILL3 | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ <br> Control: $\mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}$ <br> Data: $\mathrm{V}_{\mathrm{IL}}=0.4 \mathrm{~V}$ | 01 | 0 | -400 | $\mu \mathrm{A}$ |
| Low level input current at data input (control high) | IIL3 | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{H}}=5.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{IL}}=0.4 \mathrm{~V} \end{aligned}$ | 02 | 0 | -400 | $\mu \mathrm{A}$ |
| Supply current | Icc | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} \text {, Control }=4.5 \mathrm{~V} \text {, } \\ & \text { Data }=0 \mathrm{~V} \end{aligned}$ | 01 |  | 20 | mA |
| Supply current | Icc | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} \text {, Control }=0 \mathrm{~V} \text {, } \\ & \text { Data }=0 \mathrm{~V} \end{aligned}$ | 02 |  | 22 | mA |
| Short circuit output current 2 / | los | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ | 01, 02 | -40 | -225 | mA |

See footnotes at end of table.

MIL-M-38510/323D
TABLE I. Electrical performance characteristics.

| Test | Symbol | $\begin{gathered} \text { Conditions } \quad 1 / \\ -55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C} \end{gathered}$ | Device types | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| Propagation delay time (low to high level) | $t_{\text {PLH }}$ | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=110 \Omega \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \end{aligned}$ | 01, 02 | 2 | 20 | ns |
| Propagation delay time (high to low level) | tphL |  | 01, 02 | 2 | 24 | ns |
| Output enable time to high level | $t_{\text {pzH }}$ |  | 01 | 2 | 28 | ns |
|  |  |  | 02 | 2 | 33 |  |
| Output enable time to low level | $t_{\text {PzL }}$ |  | 01 | 2 | 33 | ns |
|  |  |  | 02 | 2 | 46 |  |
| Output disable time from high level | tphz |  | 01 | 2 | 41 | ns |
|  |  |  | 02 | 2 | 48 |  |
| Output disable time from low level | tpLz |  | 01 | 2 | 33 | ns |
|  |  |  | 02 | 2 | 39 |  |

1/ Complete terminal conditions shall be as specified in table III.
2/ Not more than one output should be shorted at a time. The duration of any short circuit should not exceed 5 seconds.

TABLE II. Electrical test requirements.

| MIL-PRF-38535 <br> test requirements | Subgroups (see table III) |  |
| :--- | :--- | :---: |
|  | Class S <br> devices | Class B <br> devices |
| Interim electrical parameters | 1 | 1 |
| Final electrical test parameters | $1^{*}, 2,3$, <br> $9,10,11$ | $1^{*}, 2,3,9$ |
| Group A test requirements | $1,2,3,9$, | $1,2,3,9$ |
|  | 10,11 | $\mathrm{~N} / \mathrm{A}$ |
| Group B electrical test parameters |  |  |
| when using the method 5005 QCI option | $1,2,3,9$, | 10,11 |

*PDA applies to subgroup 1.

$$
\frac{\text { DEVICE TYPE } 01}{\text { CASES C AND D }}
$$



Positive logic: $\mathrm{Y}=\mathrm{A}$
Output is off (disabled) when $C$ is high.

$$
\frac{\text { DEVICE TYPE } 02}{\text { CASES C AND D }}
$$



Positive logic: $\mathrm{Y}=\mathrm{A}$
Output is off (disabled) when C is low.

FIGURE 1. Terminal connections and logic diagram.


FIGURE 1. Terminal connections and logic diagram - Continued.
Device type 01

| INPUTS |  |  |
| :---: | :---: | :---: |
| $\bar{E} \bar{E}$ | D | OUTPUT |
| L | L | L |
| L | H | H |
| H | X | Z |

Device type 02

| INPUTS |  |  |
| :---: | :---: | :---: |
| E | D |  |
| $H$ | L | L |
| $H$ | $H$ | $H$ |
| L | X | Z |

[^0]FIGURE 2. Truth tables.


NOTES:

1. $C_{L}=50 \mathrm{pF} \pm 10 \%$ minimum for all tests. $C_{L}$ includes scope probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{t}_{\mathrm{p}}=500 \mathrm{~ns}$, $Z_{\text {OUt }} \approx 50 \Omega, \mathrm{~V}_{\text {gen }}=3.0 \mathrm{~V}, \mathrm{t}_{\mathrm{r}} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}$ between 0.7 V and 2.7 V .

FIGURE 3. Switching time test circuit and waveforms.
MIL-M-38510/323D

alternate load circuit


> ALTERNATE VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

ALTERNATE VOLTAGE WAVEFORMS $S_{1}$ AND $S_{2}$ CLOSED FOR TRI-STATE SWITCHING

## NOTES:

1. Diodes are 1 N 3064 or equivalent.
2. $C_{L}=50 \mathrm{pF} \pm 10 \%$ for $t_{\text {PLH, }} t_{\text {PHL }}, t_{\text {PZL }}$ and $t_{\text {PzH }} ; C_{L}=15 \mathrm{pF}$ minimum for $t_{\text {PHz }}$ and $t_{\text {PLZ }} C_{L}$ includes probe and jig capacitance.

FIGURE 3. Switching time test circuit and waveforms - Continued.
TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be high $\geq 2.0 \mathrm{~V}$, or low

See footnotes at end of device type 01.
See footnotes at end of device type 01.
TABLE III. Group A inspection for device type 01 - Continued.

TABLE III. Group A inspection for device type 02.

1/ Pins not referenced are NC.

2/ For circuits $A$ and $B$, pin conditions shall be high $\geq 2.0 \mathrm{~V}$, or open.
3/ Minimum and maximum test limits for $I_{\mathrm{IL} 1}$ and $\mathrm{I}_{\mathrm{LL} 3}$ shall be as follows:

| Tests | Circuits |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | A | B | C | D | E |
|  | $-150 /-380$ | $-120 /-360$ | $0 /-200$ | $-160 /-400$ | $-140 /-370$ |
| IIL3 | $-150 /-380$ | $-160 /-400$ | $0 /-200$ | $0 /-100$ | $-140 /-370$ |

## 5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)
6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
6.2 Acquisition requirements. Acquisition documents should specify the following:
a. Title, number, and date of the specification.
b. Complete part number (see 1.2).
c. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
d. Requirements for certificate of compliance, if applicable.
e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
g. Requirements for product assurance options.
h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
j. Requirements for "JAN" marking.
6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.
6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.
6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

| GND | Ground zero voltage potential |
| :---: | :---: |
| $\mathrm{V}_{\text {IN }}$......................................... ${ }^{\text {a }}$ | Voltage level at an input terminal |
| 1 N | Current flowing into an input terminal |
| tphz $^{\text {....................................... }}$ | Output disable time from high level. The time between the specified reference points on the input and output voltage waveforms with the three state output changing from the defined high level to a high impedance (off) state. |
| tplz ........................................ | Output disable time from low level. The time between the specified reference points on the input and output voltage waveforms with the three state output changing from the defined low level to a high impedance (off) state. |
| tpzH ........................................ | Output enable time to high level. The time between the specified reference points on the input and output voltage waveforms with the three state output changing from a high impedance (off) state to the defined high level. |
| r | Output enable time to low level. The time between the specified reference points on the input and output voltage waveforms with the three state output changing from a high impedance (off) state to the defined low level. |

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.
6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

| Military device <br> type | Generic-industry <br> type |
| :---: | :---: |
| 01 | 54 LS 125 A |
| 02 | 54 LS 126 |

6.8 Manufacturers' designation. Manufacturers' circuits which form a part of this specification are designated with an " X " as shown in table IV herein.

TABLE IV. Manufacturers' designations.

| $\begin{array}{c}\text { Device } \\ \text { type }\end{array}$ | Circuits |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | A | B | C | D | E |
|  |  |  |  |  |  | \(\left.\begin{array}{c}Signetics <br>

Corp.\end{array} $$
\begin{array}{c}\text { National } \\
\text { Semiconductor } \\
\text { Corp. }\end{array}
$$ \quad $$
\begin{array}{c}\text { Motorola } \\
\text { Inc. }\end{array}
$$ \quad $$
\begin{array}{c}\text { Fairchild } \\
\text { Semiconductor }\end{array}
$$\right]\)
6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

| Custodians: | Preparing activity: |
| :--- | :---: |
| Army - CR | DLA - CC |
| Navy - EC |  |
| Air Force -11 | (Project 5962-1970) |
| DLA - CC |  |

Review activities:
Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force-03, 19, 99

## STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

## INSTRUCTIONS

1. The preparing activity must complete blocks $1,2,3$, and 8 . In block 1 , both the document number and revision letter should be given.
2. The submitter of this form must complete blocks $4,5,6$, and 7 , and send to preparing activity.
3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

| I RECOMMEND A CHANGE: | 1. DOCUMENT NUMBER <br> MIL-M-38510/323D | 2. DOCUMENT DATE (YYYYMMDD) <br> $2003-07-14$ |
| :--- | :--- | :--- |
| 3. DOCUMENT TITLE <br>  <br> MICROCIRCUITS, DIGITAL, BIPOLAR, LOW-POWER SCHOTTKY TTL, QUADRUPLE BUS BUFFER GATES WITH 3 <br> STATE OUTPUTS, MONOLITHIC SILICON |  |  |

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)
5. REASON FOR RECOMMENDATION

| a. NAME (Last, First Middle Initial) | b. ORGANIZATION |
| :---: | :---: |
| c. ADDRESS (Inc/ude Zip Code) | d. TELEPHONE (Include Area Code) 7. DATE SUBMITTED <br> (1) Commercial  <br> (YYYYMMDD)  <br> (2) DSN  <br>  (If applicable) |
| 8. PREPARING ACTIVITY |  |
| a. NAME <br> Defense Supply Center, Columbus | b. TELEPHONE (Include Area Code <br> (1) Commercial 614-692-0536 <br> (2) DSN 850-0536 |
| c. ADDRESS (Include Zip Code) DSCC-VA <br> P. O. Box 3990 <br> Columbus, Ohio 43216-5000 | IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: <br> Defense Standardization Program Office (DLSC-LM) <br> 8725 John J. Kingman Road, Suite 2533 <br> Fort Belvoir, Virginia 22060-6221 <br> Telephone (703)767-6888 DSN 427-6888 |


[^0]:    $\mathrm{H}=$ high level logic
    L = low level logic
    X = Doesn't matter
    $Z=$ High impedance (off)

