FAIRCHILD
A Schlumberger Company

93415/93L415
1024 x 1-Bit Static Random Access Memory

Memory and High Speed Logic

Description

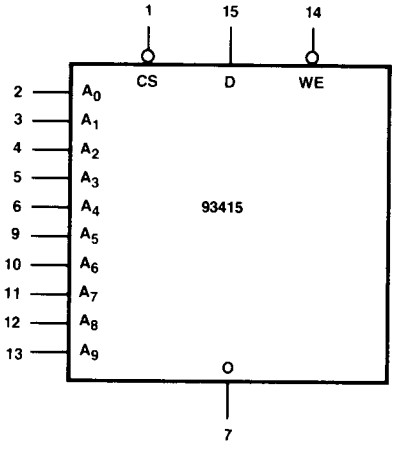
The 93415 is a 1024-bit read/write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

- **Commercial Address Access Time**
  93415 — 25 to 60 ns Max
- **Military Address Access Time**
  93415 — 30 to 70 ns Max
- **Low Power Version Also Available (93L415)**
- **Features Open Collector Output**
- **Power Dissipation — 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable Input (Active LOW)
D	Data Input
O	Data Output

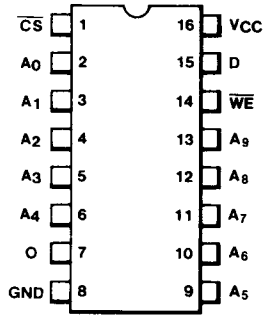
Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram

16-Pin DIP (Top View)



Note:
The 16-pin Flatpak version has the same pinout connections as the Dual In-line package.

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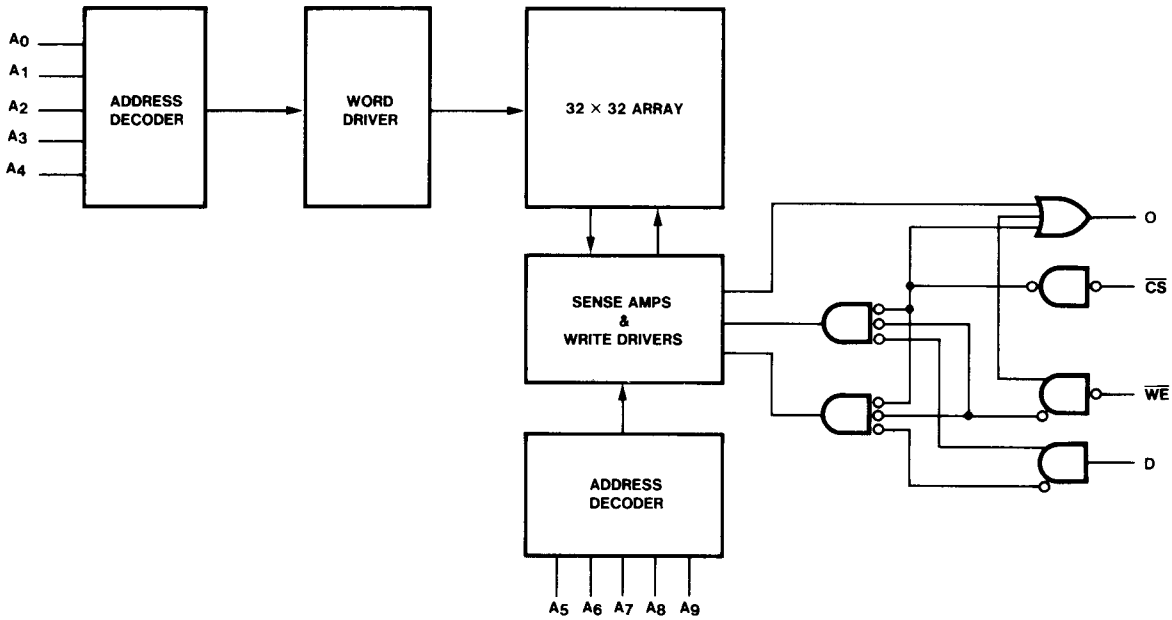
Logic Diagram



Functional Description

The 93415 is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93415 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at A_0 through A_9. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output (O).

An open collector output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output

when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(Max)}{I_{OL} - FO(1.6)} \leq R_L \leq \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by the output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.
One Unit Load = 40 μA HIGH/1.6 mA LOW.
FO_{MAX} = 5 UL.

Truth Table

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D	O	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)

DC Characteristics: Over operating temperature ranges (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs[5]
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for All Inputs[5]
I_{IL}	Input LOW Current		−250	−400[7]	μA	V_{CC} = Max, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5 V
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = Max, V_{OUT} = 4.5 V
I_{CC}	Power Supply Current			65	mA	93L415-35, 93L415-45, 93L415-60 (commercial)
				75	mA	93L415-40, 93L415-50, 93L415-70 (military)
				125	mA	93415-25, 93415-30 (commercial)
				135	mA	93415-30, 93415-40 (military)
				155	mA	93415A, 93415-45 (commercial)
				170	mA	93415-60 (military)
						V_{CC} = Max, Note 6

Notes
1. Typical values are at V_{CC} = 5.0 V, T_C = +25° C and maximum loading.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. Short circuit to ground not to exceed one second.
4. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.
5. Tested under static condition only.
6. All inputs GND
   Output open
7. I_{IL} = −300 μA for 93L415

Commercial

AC Performance Characteristics: $V_{CC} = 5.0 \pm 5\%$, GND = 0 V, $T_C = 0°$ C to $+75°$ C

Symbol	Characteristic	93415-25 Min	93415-25 Max	93415-30 93415A Min	93415-30 93415A Max	93415-45 Min	93415-45 Max	Unit	Condition
	Read Timing								
t_{ACS}	Chip Select Access Time		15		20		35	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		20		20		35	ns	
t_{AA}	Address Access Time[2]		25		30		45	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	15		20		35		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		5		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{WS}	Write Enable to Output Disable		15		20		35	ns	
t_{WR}	Write Recovery Time		15		20		40	ns	
t_{WR}	Write Recovery Time (93415A)				25			ns	

Military

AC Performance Characteristics: $V_{CC} = 5.0$ V $\pm$ 10%, GND = 0 V, $T_C = -55°$C to $+125°$C

Symbol	Characteristic	93415-30 Min	93415-30 Max	93415-40 Min	93415-40 Max	93415-60 Min	93415-60 Max	Unit	Condition
	Read Timing								
t_{ACS}	Chip Select Access Time		20		25		45	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		20		25		50	ns	
t_{AA}	Address Access Time[2]		30		40		60	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	20		25		40		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		10		15		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{WS}	Write Enable to Output Disable		20		25		45	ns	
t_{WR}	Write Recovery Time		20		25		50	ns	

Notes on page 4-7

Commercial

AC Performance Characteristics: $V_{CC} = 5.0 \pm 5\%$, GND = 0 V, T_C = 0° C to +75° C

Symbol	Characteristic	93L415-35		93L415-45		93L415-60		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		25		30		40	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		25		30		40	ns	
t_{AA}	Address Access Time[2]		35		45		60	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	30		35		45		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	5		5		10		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		5		ns	
t_{WS}	Write Enable to Output Disable		20		25		45	ns	
t_{WR}	Write Recovery Time		30		35		45	ns	

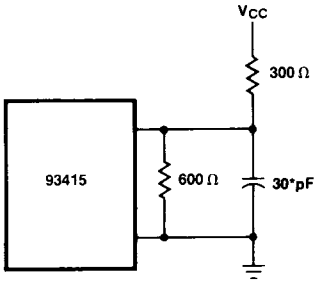
Military

AC Performance Characteristics: $V_{CC} = 5.0\ V \pm 10\%$, GND = 0 V, T_C = -55° C to +125° C

Symbol	Characteristic	93L415-40		93L415-50		93L415-70		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Read Timing								
t_{ACS}	Chip Select Access Time		30		35		45	ns	*Figures 3a, 3b*
t_{RCS}	Chip Select Recovery Time		25		30		50	ns	
t_{AA}	Address Access Time[2]		40		50		70	ns	
	Write Timing								
t_W	Write Pulse Width to Guarantee Writing[4]	35		40		50		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		10		ns	
t_{WHD}	Data Hold Time after Write	5		5		10		ns	
t_{WSA}	Address Setup Time Prior to Write[4]	10		10		10		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		10		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		10		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		10		ns	
t_{WS}	Write Enable to Output Disable		25		30		45	ns	
t_{WR}	Write Recovery Time		30		40		55	ns	

Notes on preceding page

Fig. 1 AC Test Circuit



*Includes jig and probe capacitance

Fig. 2 AC Test Input Levels

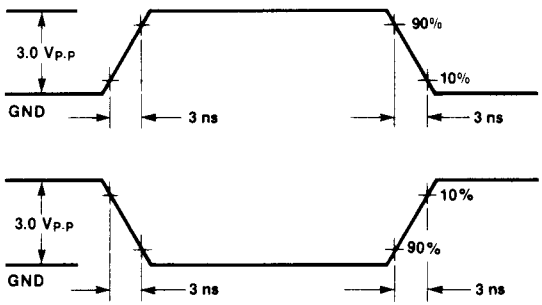
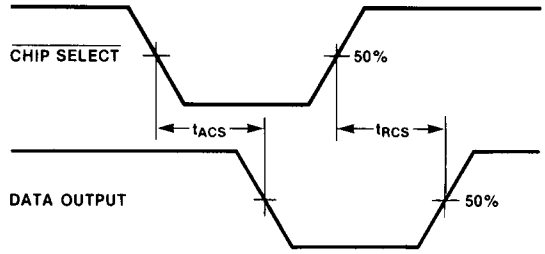


Fig. 3 Read Mode Timing

3a Read Mode Propagation Delay from Chip Select



3b Read Mode Propagation Delay from Address

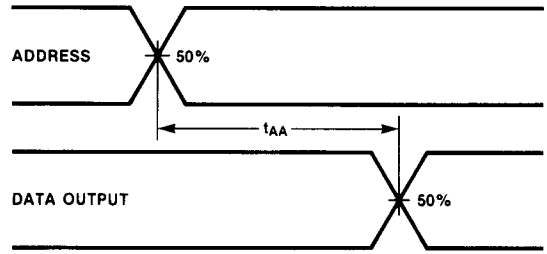
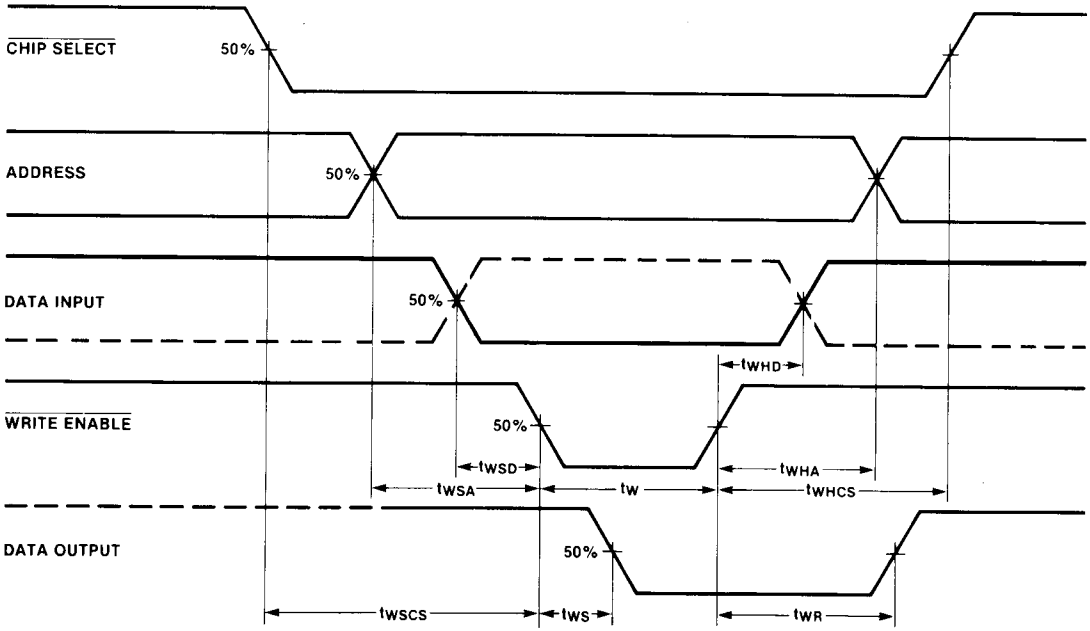


Fig. 4 Write Mode Timing



Notes

1. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.
2. Input voltage levels for worst case AC test are 3.0/0.0 V.

Ordering Information

Part Number	Access Time (ns)	Power (mA)	Temperature Range	Package	Order Code
93415-25	25	125	0° C to +75° C	XX	93415XX25
93415A	30	155	0° C to +75° C	XX	93415AXX
93415-30	30	125	0° C to +75° C	XX	93415XX30
93415-30	30	135	−55° C to +125° C	YY	93415YY30
93L415-35	35	65	0° C to +75° C	XX	93L415XX35
93415-40	40	135	−55° C to +125° C	YY	93415YY40
93L415-40	40	75	−55° C to +125° C	YY	93L415YY40
93415-45	45	155	0° C to +75° C	XX	93415XX
93L415-45	45	65	0° C to +75° C	XX	93L415XX45
93L415-50	50	75	−55° C to +125° C	YY	93L415YY50
93L415-60	60	65	0° C to +75° C	XX	93L415XX
93415-60	60	170	−55° C to +125° C	YY	93415YY
93L415-70	70	75	−55° C to +125° C	YY	93L415YY

Packages and Optional Processing (See Section 9)

XX — Commercial

Without Optional Processing	With Optional Processing
DC	DCQR — Ceramic Dip
FC	FCQR — Cerpak
PC	PCQR — Plastic Dip

YY — Military

Without Optional Processing	With Optional Processing
DM	DMQB — Ceramic Dip
FM	FMQB — Cerpak

Optional Processing

QB = Mil Std 883
Method 5004 and 5005, Level B
QR = Commercial Device with
160 Hour Burn in or Equivalent

Note:
Because every combination of packaging, speed, temperature, and optional processing is not in stock, availability of some combinations is not on an immediate basis.