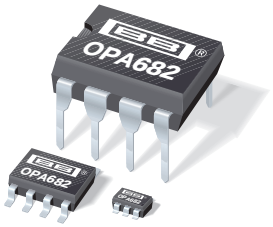
BURR - BROWN®



OPA682

SpeedPlus™ Wideband, Fixed Gain BUFFER AMPLIFIER With Disable

FEATURES

- INTERNALLY FIXED GAIN: +2 OR ±1
- HIGH BANDWIDTH (G = +2): 240MHz
- LOW SUPPLY CURRENT: 6mA
- LOW DISABLED CURRENT: 320µA
- HIGH OUTPUT CURRENT: 150mA
- OUTPUT VOLTAGE SWING: ±4.0V
- ±5V OR SINGLE +5V OPERATION
- SOT23-6 AVAILABLE

APPLICATIONS

- BROADBAND VIDEO LINE DRIVERS
- VIDEO MULTIPLEXERS
- MULTIPLE LINE VIDEO DA
- PORTABLE INSTRUMENTS
- ADC BUFFERS
- ACTIVE FILTERS

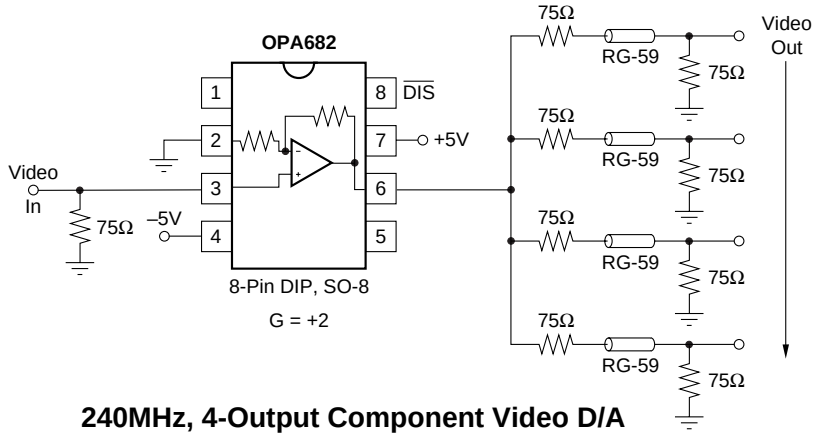
DESCRIPTION

The OPA682 provides an easy to use, broadband fixed gain buffer amplifier. Depending on the external connections, the internal resistor network may be used to provide either a fixed gain of +2 video buffer or a gain of +1 or –1 voltage buffer. Operating on a very low 6mA supply current, the OPA682 offers a slew rate and output power normally associated with a much higher supply current. A new output stage architecture delivers high output current with a minimal headroom and crossover distortion. This gives exceptional single supply operation. Using a single +5V supply, the OPA682 can deliver a 1V to 4V output swing with over 100mA drive current and 200MHz bandwidth. This combination of features makes the OPA682 an ideal RGB line driver or single supply ADC input driver.

The OPA682's low 6mA supply current is precisely trimmed at 25°C. This trim, along with low drift over temperature, guarantees lower maximum supply current than competing products that report only a room temperature nominal supply current. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it high, gives normal operation. If pulled low, the OPA682 supply current drops to less than 320µA while the output goes into a high impedance state. This feature may be used for either power savings or for video MUX applications.

OPA682 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage Feedback	OPA680	OPA2680	OPA3680
Current Feedback	OPA681	OPA2681	OPA3681
Fixed Gain	OPA682	OPA2682	OPA3682



240MHz, 4-Output Component Video D/A

nternational Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS: $V_S = \pm 5V$

G = +2 (–IN grounded) and R_L = 100Ω (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA682P, U, N						
		TYP	GUARANTEED[1]					
		+25°C	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL[2]
AC PERFORMANCE (Figure 1)								
Small-Signal Bandwidth (V_O < 0.5Vp-p)	G = +1	330				MHz	typ	C
	G = +2	240	220	210	190	MHz	min	B
	G = –1	220				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5Vp-p	150	50	45	45	MHz	min	B
Peaking at a Gain of +1	V_O < 0.5Vp-p	0.8	2	4		dB	max	B
Large-Signal Bandwidth	G = +2, V_O = 5Vp-p	210				MHz	typ	C
Slew Rate	G = +2, 4V Step	2100	1600	1600	1200	V/µs	min	B
Rise/Fall Time	G = +2, V_O = 0.5V Step	1.7				ns	typ	C
	G = +2, V_O = 5V Step	2.0				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd Harmonic	R_L = 100Ω	–69	–62	–59	–57	dBc	max	B
	R_L ≥ 500Ω	–79	–70	–67	–65	dBc	max	B
3rd Harmonic	R_L = 100Ω	–84	–75	–71	–69	dBc	max	B
	R_L ≥ 500Ω	–95	–82	–76	–74	dBc	max	B
Input Voltage Noise	f > 1MHz	2.2	3.0	3.4	3.6	nV/√Hz	max	B
Non-Inverting Input Current Noise	f > 1MHz	12	14	15	15	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	15	18	18	19	pA/√Hz	max	B
Differential Gain	NTSC, R_L = 150Ω	0.001				%	typ	C
	NTSC, R_L = 37.5Ω	0.008				%	typ	C
Differential Phase	NTSC, R_L = 150Ω	0.01				deg	typ	C
	NTSC, R_L = 37.5Ω	0.05				deg	typ	C
DC PERFORMANCE[3]								
Gain Error	G = +1	±0.2				%	typ	C
	G = +2	±0.3	**±1.5**			%	max	A
	G = –1	±0.2	±1.5			%	max	B
Internal R_F and R_G								
Maximum		400	**480**	510	520	Ω	max	A
Minimum		400	**320**	310	290	Ω	min	A
Average Drift			0.13	0.13	0.13	%/C°	max	B
Input Offset Voltage	V_{CM} = 0V	±1.3	**±5**	±6.5	±7.5	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			+35	+40	µV/°C	max	B
Non-Inverting Input Bias Current	V_{CM} = 0V	+30	**+55**	±65	±85	µA	max	A
Average Non-Inverting Input Bias Current Drift	V_{CM} = 0V			–400	–450	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±10	**±40**	±50	±55	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			–125	–150	nA°C	max	B
INPUT								
Common-Mode Input Range		±3.5	**±3.4**	±3.3	±3.2	V	min	A
Non-Inverting Input Impedance		100 || 2				kΩ || pF	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**	±3.7	±3.6	V	min	A
	100Ω Load	±3.9	**±3.7**	±3.6	±3.3	V	min	A
Current Output, Sourcing		+190	**+160**	+140	+80	mA	min	A
Sinking		–150	**–135**	–130	–80	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.03				Ω	typ	C

SPECIFICATIONS: V_S = ±5V (Cont.)

G = +2 (–IN grounded) and R_L = 100Ω (Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA682P, U, N						TEST LEVEL(2)
		TYP	GUARANTEED(1)					
		+25°C	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	
DISABLE/POWER DOWN ($\overline{DIS}$ Pin)								
Power Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–320				µA	typ	C
Disable Time		100				ns	typ	C
Enable Time		25				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω	±50				mV	typ	C
Turn Off Glitch	G = +2, R_L= 150Ω	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current	$V_{\overline{DIS}}$ = 0	100	**160**	160	160	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Max Quiescent Current	V_S = ±5V	6	**6.4**	6.5	6.6	mA	max	A
Min Quiescent Current	V_S = ±5V	6	**5.6**	5.5	5.0	mA	min	A
Power Supply Rejection Ratio (–PSRR)	Input Referred	58	52	50	49	dB	min	A
TEMPERATURE RANGE								
Specification: P, U, N		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
P 8-Pin DIP		100				°C/W	typ	C
U SO-8		125				°C/W	typ	C
N SOT23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and 25°C guaranteed specifications. Junction temperature = ambient temperature +23°C at high temperature limit guaranteed specifications. (2) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

SPECIFICATIONS: V_S = +5V

G = +2 (–IN grounded though 0.1µF) and R_L = 100Ω to V_S/2 (Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA682P, U, N						TEST LEVEL[2]
		TYP	GUARANTEED[1]					
		+25°C	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	
AC PERFORMANCE (Figure 2)								
Small-Signal Bandwidth (V_O < 0.5Vp-p)	G = +1	290				MHz	typ	C
	G = +2	220	180	140	110	MHz	min	B
	G = –1	200				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5Vp-p	100	50	35	23	MHz	min	B
Peaking at a Gain of +1	V_O < 0.5Vp-p	0.4	2	4		dB	max	B
Large-Signal Bandwidth	G = +2, V_O = 2Vp-p	210				MHz	typ	C
Slew Rate	G = +2, 2V Step	830	700	680	570	V/µs	min	B
Rise/Fall Time	G = +2, V_O = 0.5V Step	1.5				ns	typ	C
	G = +2, V_O = 2V Step	2.0				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	14				ns	typ	C
0.1%	G = +2, V_O = 2V Step	9				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd Harmonic	R_L = 100Ω to V_S/2	–62	–56	–55	–53	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–69	–62	–61	–59	dBc	max	B
3rd Harmonic	R_L = 100Ω to V_S/2	–71	–64	–63	–61	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–73	–68	–67	–65	dBc	max	B
Input Voltage Noise	f > 1MHz	2.2	3.0	3.4	3.6	nV/√Hz	max	B
Non-Inverting Input Current Noise	f > 1MHz	12	14	14	15	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	15	18	18	19	pA/√Hz	max	B
DC PERFORMANCE[3]								
Gain Error	G = +1	±0.2				%	typ	C
	G = +2	±0.3	**±1.5**			%	max	A
	G = –1	±0.2	±1.5			%	max	B
Internal R_F and R_G								
Maximum		400	480	510	520	Ω	max	B
Minimum		400	320	310	290	Ω	min	B
Average Drift			0.13	0.13	0.13	%/C°	max	B
Input Offset Voltage	V_{CM} = 2.5V	±1	**±5**	±6	±7	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			+15	+20	µV/°C	max	B
Non-Inverting Input Bias Current	V_{CM} = 2.5V	+40	**+65**	+75	+95	µA	max	A
Average Non-Inverting Input Bias Current Drift	V_{CM} = 2.5V			–300	–350	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 2.5V	±5	**±20**	±25	±35	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 2.5V			–125	–175	nA°C	max	B
INPUT								
Least Positive Input Voltage		1.5	1.6	1.7	1.8	V	max	B
Most Positive Input Voltage		3.5	3.4	3.3	3.2	V	min	B
Non-Inverting Input Impedance		100 || 2				kΩ || pF	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4.0	**3.8**	3.7	3.5	V	min	A
	R_L = 100Ω	3.9	**3.7**	3.6	3.4	V	min	A
Least Positive Output Voltage	No Load	1.0	**1.2**	1.3	1.5	V	max	A
	R_L = 100Ω	1.1	**1.3**	1.4	1.6	V	max	A
Current Output, Sourcing		+150	**+110**	+110	+60	mA	min	A
Sinking		–110	**–75**	–70	–50	mA	min	A
Output Impedance	G = +2, f = 100kHz	0.03				Ω	typ	C

SPECIFICATIONS: V_S = +5V (Cont.)

G = +2 (–IN grounded though 0.1µF) and R_L = 100Ω to V_S/2 (Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA682P, U, N						TEST LEVEL(2)
		TYP	GUARANTEED(1)					
		+25°C	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	
DISABLE/POWER DOWN ($\overline{DIS}$ Pin)								
Power Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–270				µA	typ	C
Disable Time		100				ns	typ	C
Enable Time		25				ns	typ	C
Off Isolation	G = +2, 5MHz	65				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = 2.5V	±50				mV	typ	B
Turn Off Glitch	G = +2, R_L = 150Ω, V_{IN} = 2.5V	±20				mV	typ	B
Enable Voltage		3.3	3.5	3.6	3.7	V	min	B
Disable Voltage		1.8	1.7	1.6	1.5	V	max	B
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	100				µA	typ	C
POWER SUPPLY								
Specified Single Supply Operating Voltage		5				V	typ	C
Maximum Single Supply Operating Voltage			**12**	12	12	V	max	A
Max Quiescent Current	V_S = +5V	4.8	**5.3**	5.4	5.4	mA	max	A
Min Quiescent Current	V_S = +5V	4.8	**4.1**	3.7	3.6	mA	min	A
Power Supply Rejection Ratio (+PSRR)	Input Referred	50				dB	typ	C
TEMPERATURE RANGE								
Specification: P, U, N		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
P 8-Pin DIP		100				°C/W	typ	C
U SO-8		125				°C/W	typ	C
N SOT23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and 25°C guaranteed specifications. Junction temperature = ambient temperature +23°C at high temperature limit guaranteed specifications. (2) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

ABSOLUTE MAXIMUM RATINGS

Power Supply	±6.5VDC
Internal Power Dissipation[1]	See Thermal Information
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, U, N	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

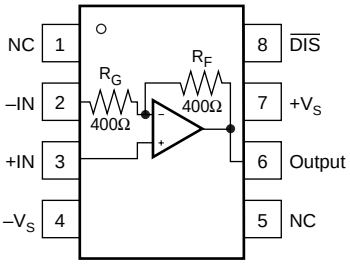
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

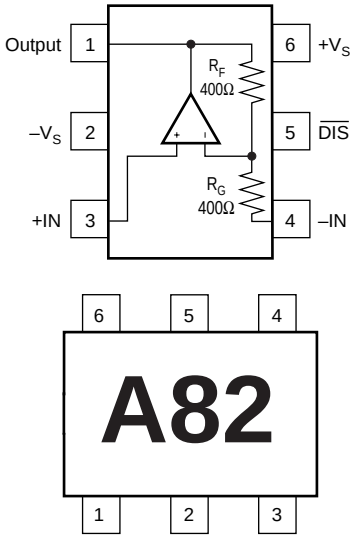
PIN CONFIGURATION

Top View **DIP/SO-8**



NC: No Connection

Top View **SOT23-6**



Pin Orientation/Package Marking

PACKAGE/ORDERING INFORMATION

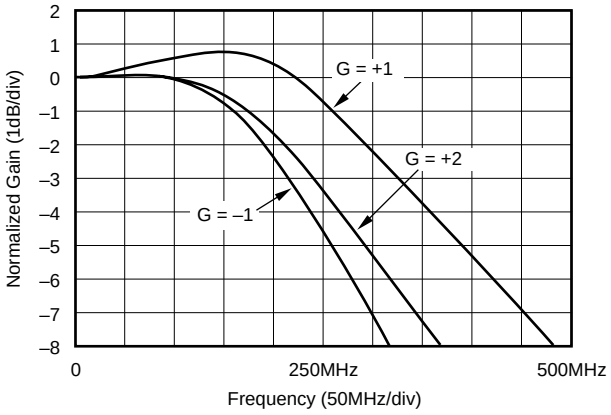
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[2]	TRANSPORT MEDIA
OPA682P	8-Pin Plastic DIP	006	–40°C to +85°C	OPA682P	OPA682P	Rails
OPA682U	SO-8 Surface Mount	182	–40°C to +85°C	OPA682U	OPA682U	Rails
"	"	"	"	"	OPA682U/2K5	Tape and Reel
OPA682N	6-Lead SOT23	332	–40°C to +85°C	A82	OPA682N/250	Tape and Reel
"	"	"	"	"	OPA682N/3K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "OPA682U/2K5" will get a single 2500-piece Tape and Reel.

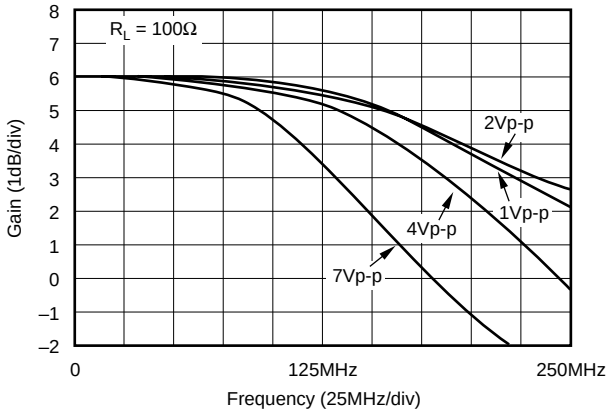
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$

G = +2 and R_L = 100Ω, unless otherwise noted (see Figure 1).

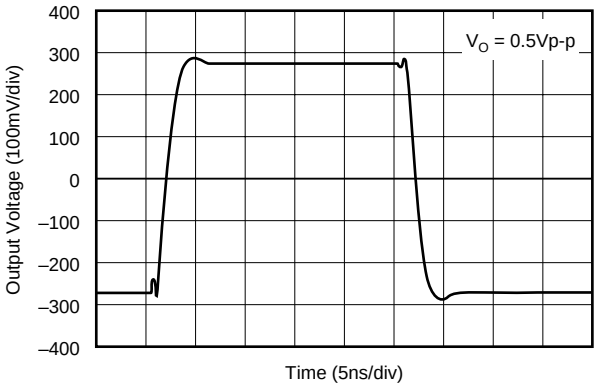
SMALL-SIGNAL FREQUENCY RESPONSE



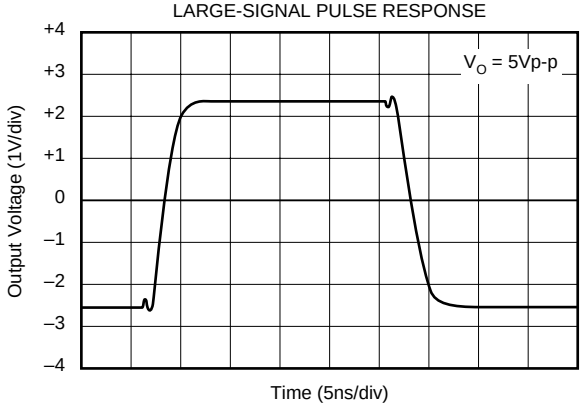
LARGE-SIGNAL FREQUENCY RESPONSE



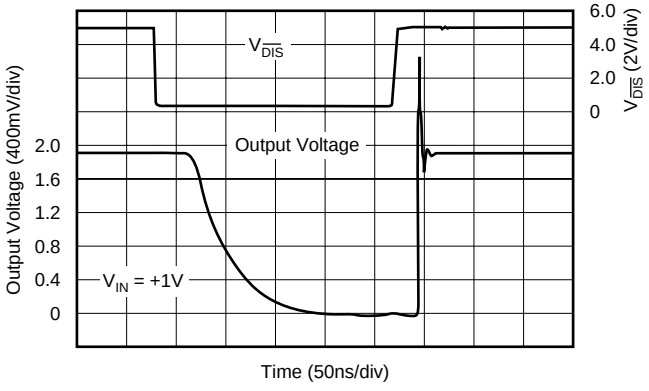
SMALL-SIGNAL PULSE RESPONSE



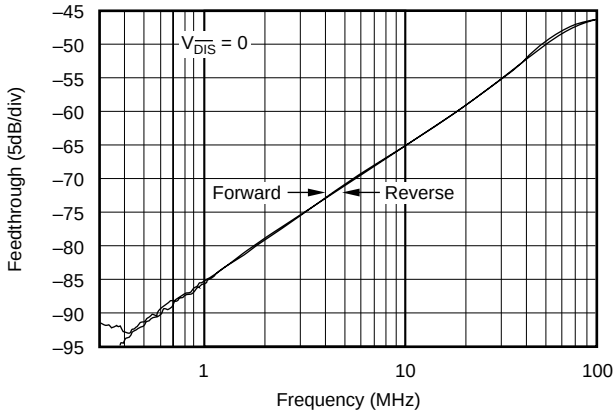
LARGE-SIGNAL PULSE RESPONSE



LARGE-SIGNAL DISABLE/ENABLE RESPONSE



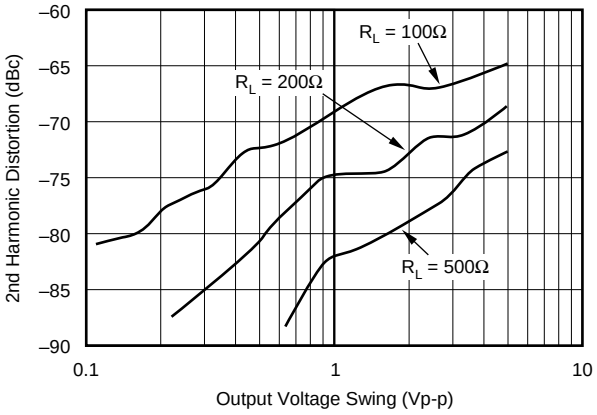
DISABLED FEEDTHROUGH vs FREQUENCY



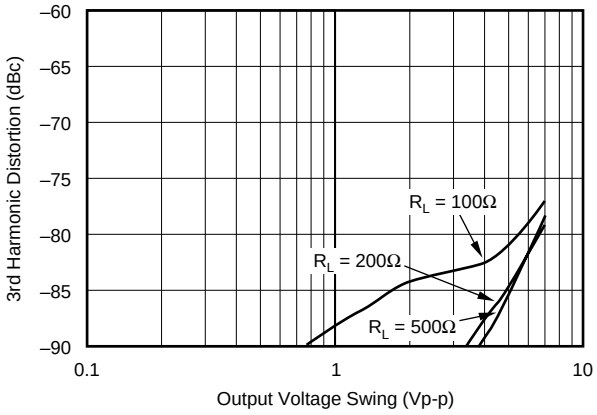
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

G = +2 and $R_L = 100\Omega$, unless otherwise noted (see Figure 1).

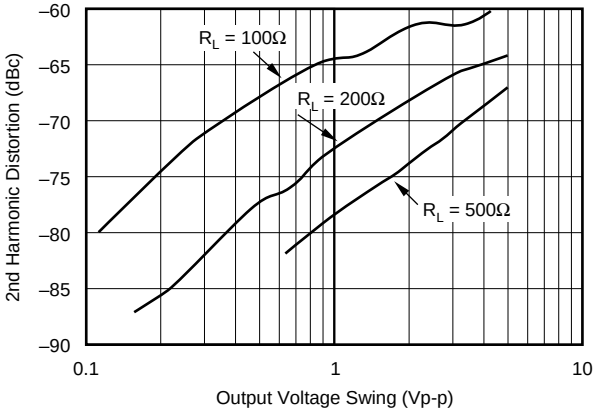
5MHz 2nd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



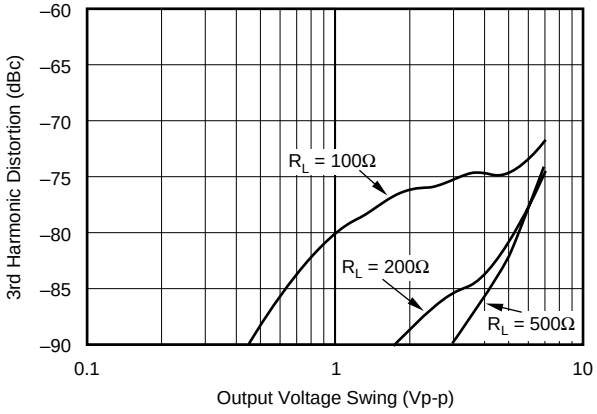
5MHz 3rd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



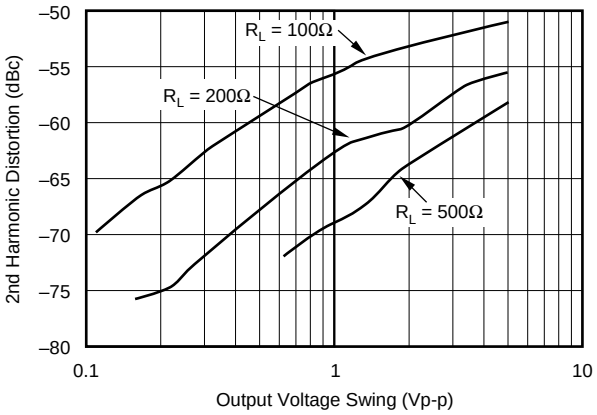
10MHz 2nd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



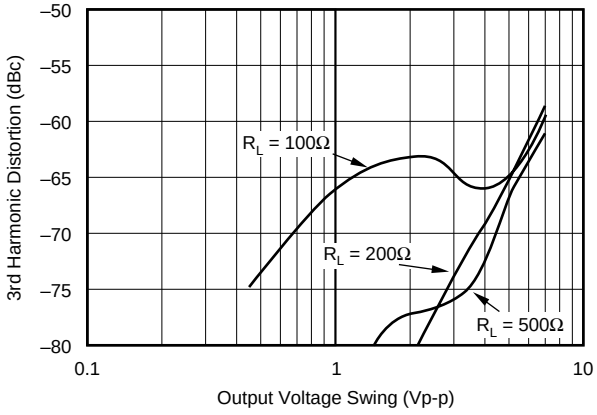
10MHz 3rd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



20MHz 2nd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



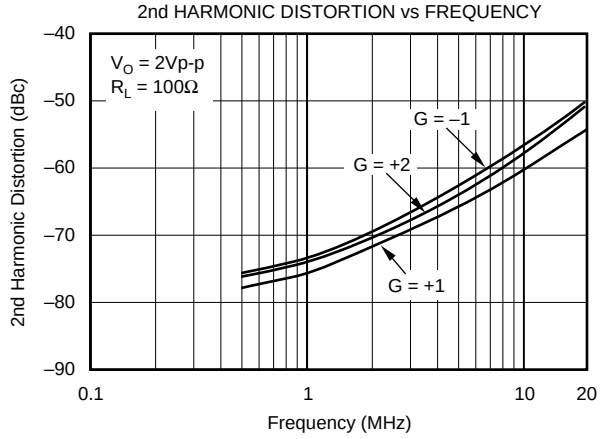
20MHz 3rd HARMONIC DISTORTION
vs OUTPUT VOLTAGE



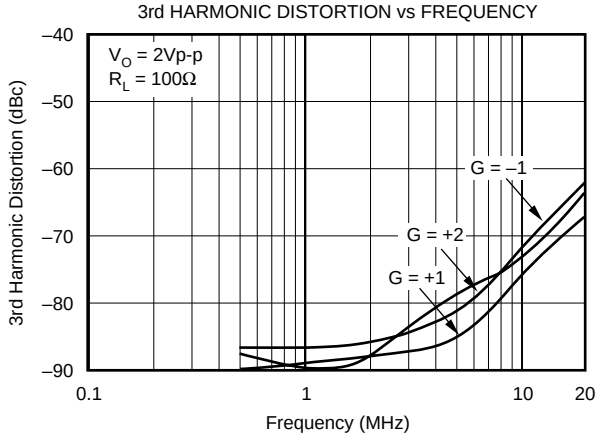
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

G = +2 and R_L = 100Ω, unless otherwise noted (see Figure 1).

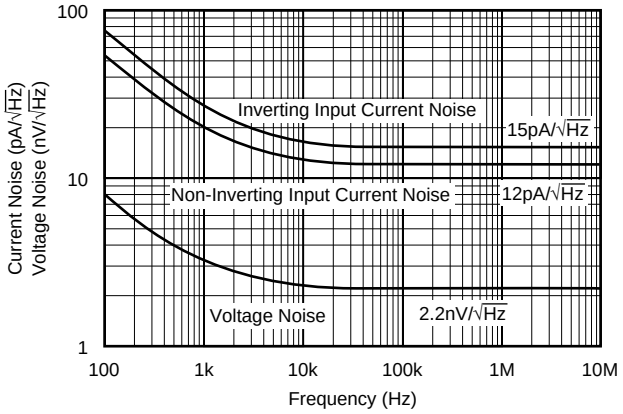
2nd HARMONIC DISTORTION vs FREQUENCY



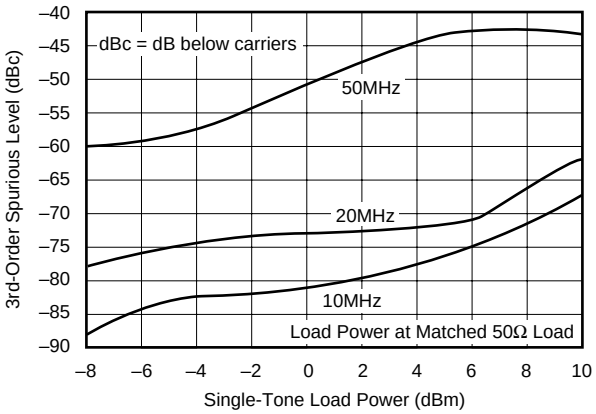
3rd HARMONIC DISTORTION vs FREQUENCY



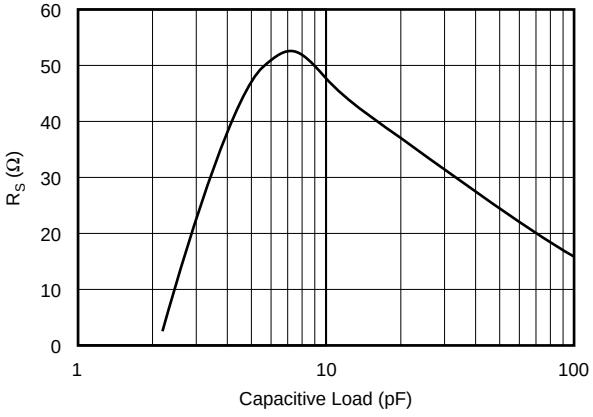
INPUT VOLTAGE AND CURRENT NOISE DENSITY



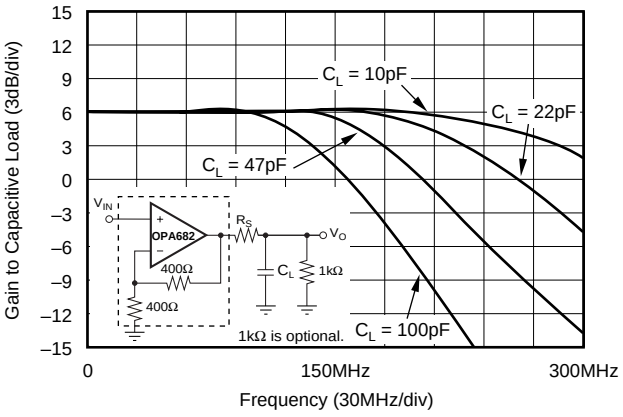
TWO-TONE, 3rd-ORDER
INTERMODULATION SPURIOUS



RECOMMENDED R_S vs CAPACITIVE LOAD



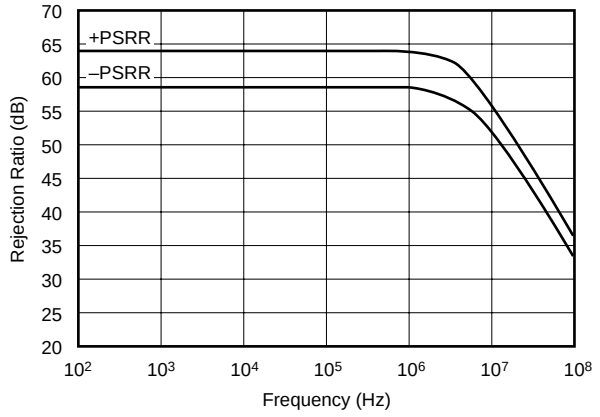
FREQUENCY RESPONSE vs CAPACITIVE LOAD



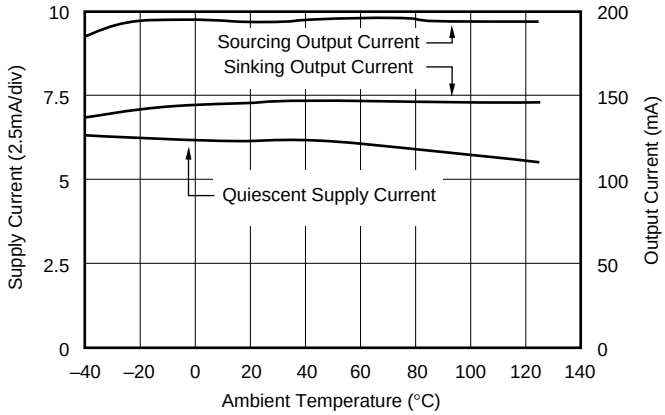
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

G = +2 and R_L = 100Ω, unless otherwise noted (see Figure 1).

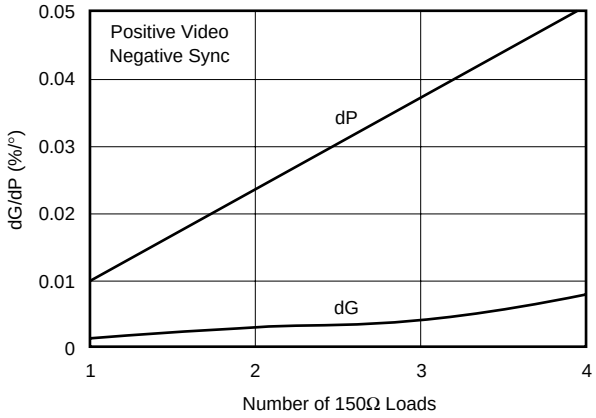
POWER SUPPLY REJECTION RATIO vs FREQUENCY



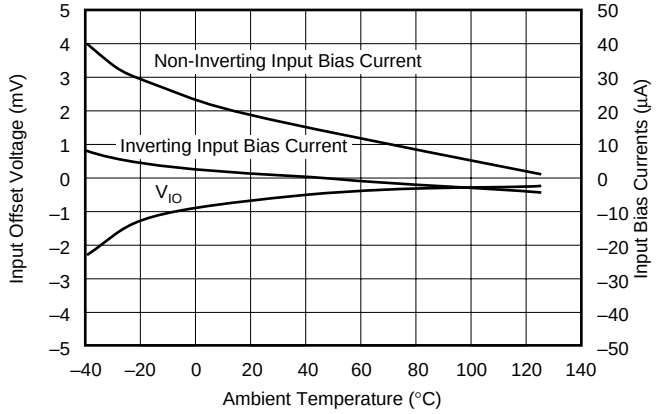
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



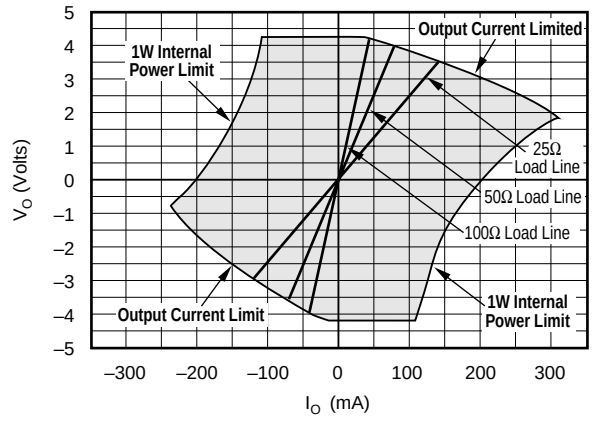
COMPOSITE VIDEO dG/dP



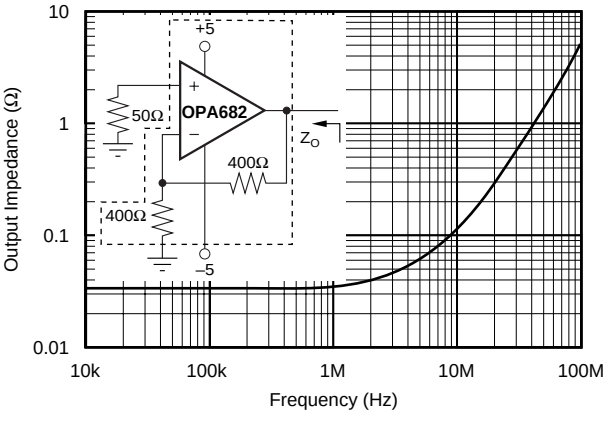
TYPICAL DC DRIFT OVER TEMPERATURE



OUTPUT VOLTAGE AND CURRENT LIMITATIONS



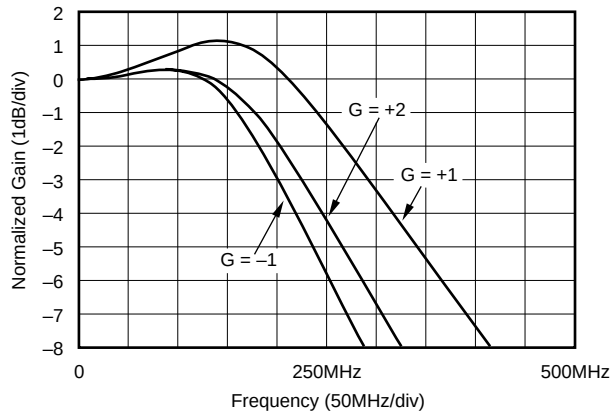
CLOSED-LOOP OUTPUT IMPEDANCE



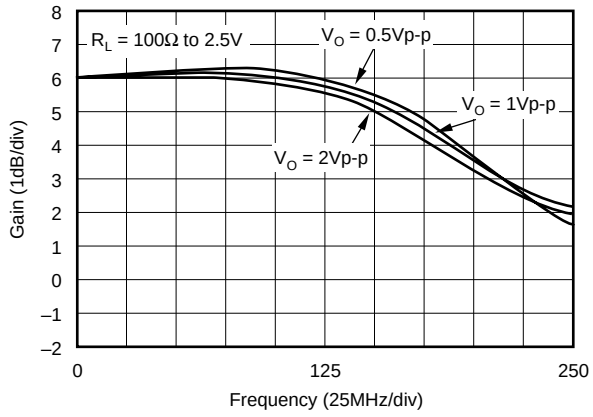
TYPICAL PERFORMANCE CURVES: V_S = +5V

G = +2 and R_L = 100Ω to V_{CM} = +2.5V, unless otherwise noted (see Figure 2).

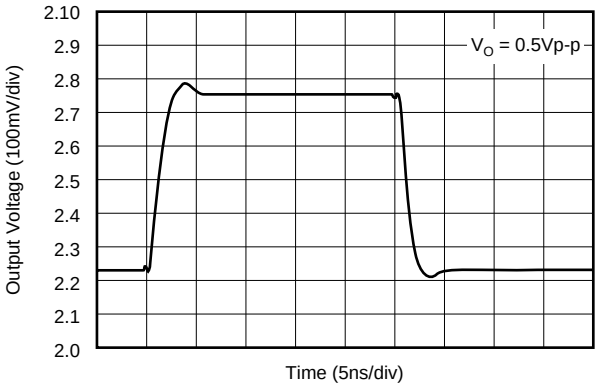
SMALL-SIGNAL FREQUENCY RESPONSE



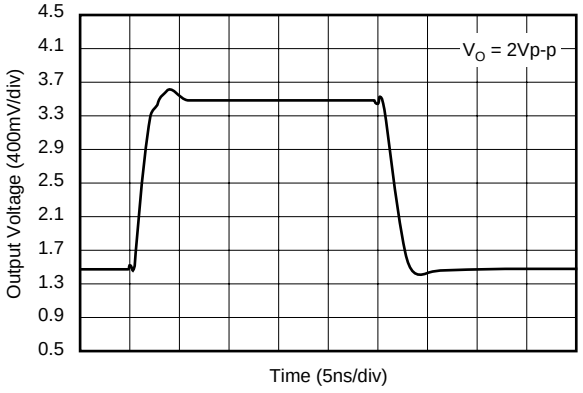
LARGE-SIGNAL FREQUENCY RESPONSE



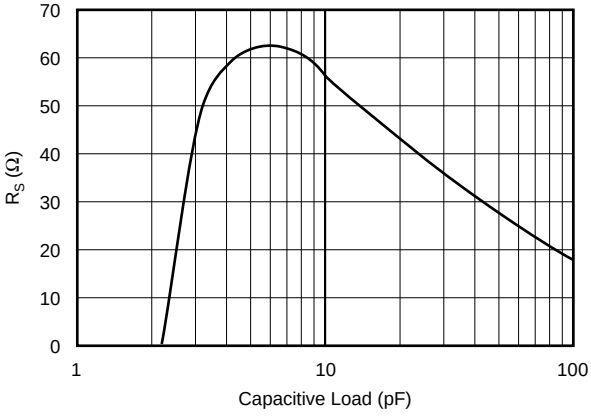
SMALL-SIGNAL PULSE RESPONSE



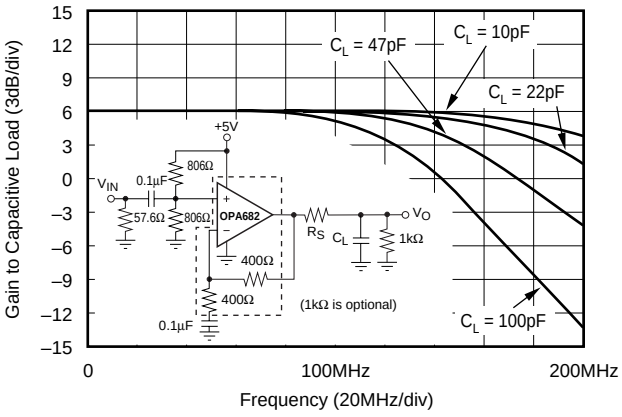
LARGE-SIGNAL PULSE RESPONSE



RECOMMENDED R_S vs CAPACITIVE LOAD



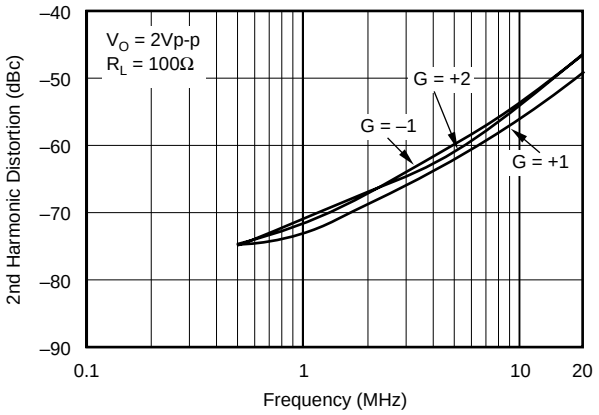
FREQUENCY RESPONSE vs CAPACITIVE LOAD



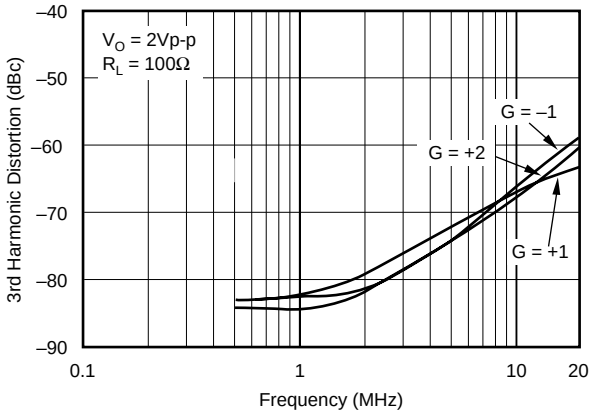
TYPICAL PERFORMANCE CURVES: V_S = +5V (Cont.)

G = +2 and R_L = 100Ω to V_{CM} = +2.5V, unless otherwise noted (see Figure 2).

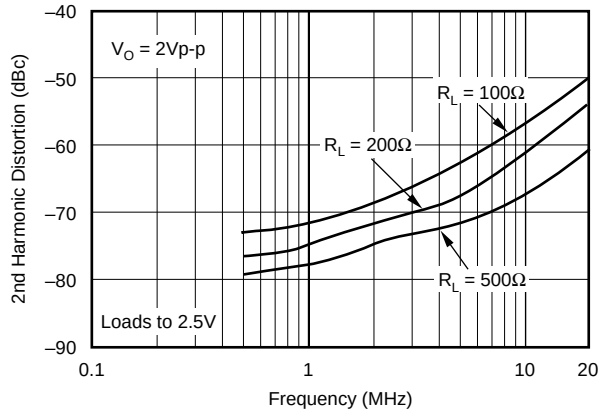
2nd HARMONIC DISTORTION vs FREQUENCY



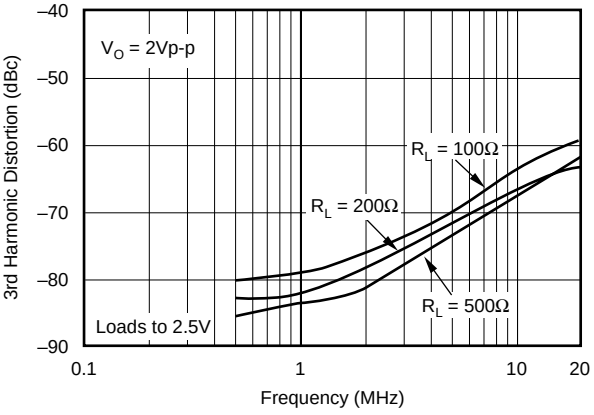
3rd HARMONIC DISTORTION vs FREQUENCY



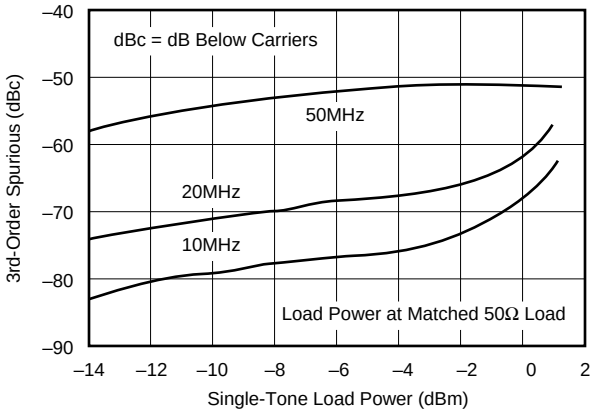
2nd HARMONIC DISTORTION vs FREQUENCY



3rd HARMONIC DISTORTION vs FREQUENCY



TWO-TONE, 3rd-ORDER SPURIOUS LEVEL



APPLICATIONS INFORMATION

WIDEBAND BUFFER OPERATION

The OPA682 gives the exceptional AC performance of a wideband current feedback op amp with a highly linear, high power output stage. It features internal R_F and R_G resistors which make it easy to select a gain of +2, +1 or –1 without any external resistors. Requiring only 6mA quiescent current, the OPA682 will swing to within 1V of either supply rail and deliver in excess of 135mA guaranteed at room temperature. This low output headroom requirement, along with supply voltage independent biasing, gives remarkable single (+5V) supply operation. The OPA682 will deliver greater than 200MHz bandwidth driving a 2Vp-p output into 100Ω on a single +5V supply. Previous boosted output stage amplifiers have typically suffered from very poor crossover distortion as the output current goes through zero. The OPA682 achieves a comparable power gain with much better linearity. The primary advantage of a current feedback op amp over a voltage feedback op amp is that AC performance (bandwidth and distortion) is relatively independent of signal gain.

Figure 1 shows the DC coupled, gain of +2, dual power supply circuit configuration used as the basis of the ±5V Specifications and Typical Performance Curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 800Ω = 89Ω. The disable control line (DIS) is typically left open to guarantee normal amplifier operation. In addition to the usual power supply decoupling capacitors to ground, a 0.1µF capacitor can be included between the two power supply pins. This optional added capacitor will typically improve the 2nd harmonic distortion performance by 3dB to 6dB.

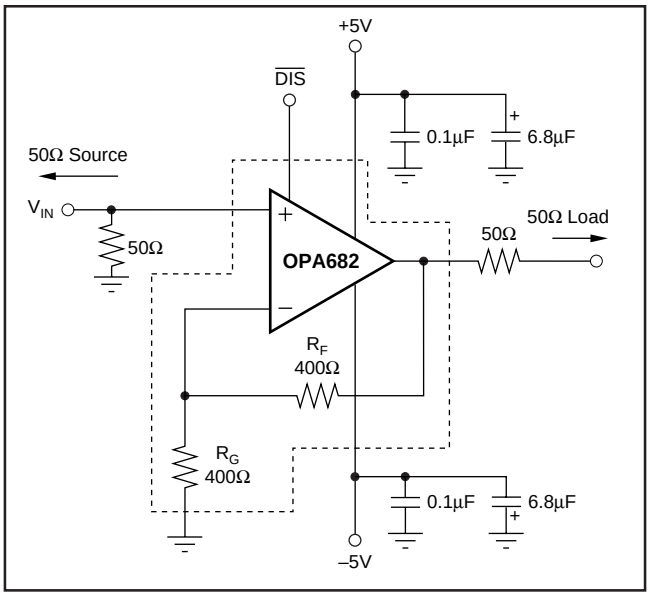


FIGURE 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit.

Figure 2 shows the AC coupled, gain of +2, single-supply circuit configuration used as the basis of the +5V Specifications and Typical Performance Curves. Though not a "rail-to-rail" design, the OPA682 requires minimal input and output voltage headroom compared to other very wideband current feedback op amps. It will deliver a 3Vp-p output swing on a single +5V supply with greater than 150MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 2 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a 2Vp-p input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1—which puts the input DC bias voltage (2.5V) on the output as well. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 80mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA682 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown by the +5V supply, 3rd harmonic distortion plots.

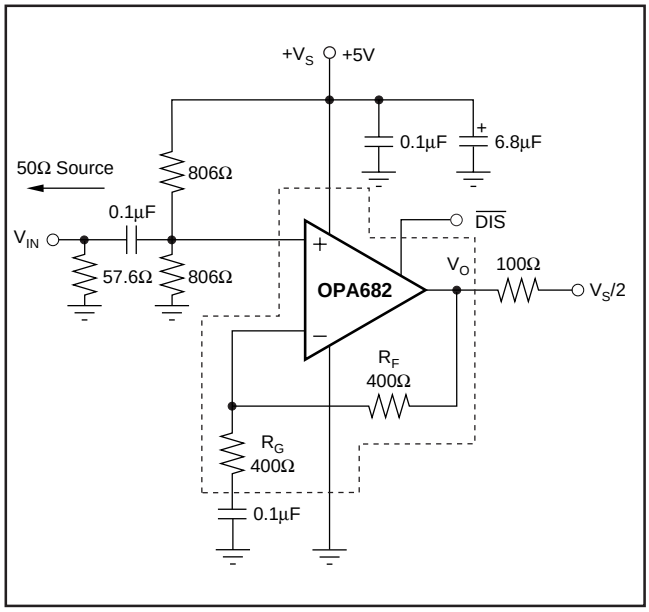


FIGURE 2. AC-Coupled, G = +2, Single Supply Specification and Test Circuit.

SINGLE-SUPPLY A/D CONVERTER INTERFACE

Most modern, high performance A/D converters (such as the Burr-Brown ADS8xx and ADS9xx series) operate on a single +5V (or lower) power supply. It has been a considerable challenge for single-supply op amps to deliver a low distortion input signal at the ADC input for signal frequen-

cies exceeding 5MHz. The high slew rate, exceptional output swing and high linearity of the OPA682 make it an ideal single-supply ADC driver. Figure 3 shows an example input interface to a very high performance 10-bit, 60MSPS CMOS converter.

The OPA682 in the circuit of Figure 3 provides 240MHz bandwidth operating at a signal gain of +2 with a 2Vp-p output swing. The non-inverting input bias voltage is referenced to the midpoint of the ADC signal range by dividing off the top and bottom of the internal ADC reference ladder. With the gain resistor (R_G) AC-coupled, this bias voltage has a gain of +1 to the output, centering the output voltage swing as well. Tested performance at a 20MHz analog input frequency and a 60MSPS clock rate on the converter gives > 58dBc SFDR.

WIDEBAND VIDEO MULTIPLEXING

One common application for video speed amplifiers which include a disable pin is to wire multiple amplifier outputs together, then select which one of several possible video inputs to source onto a single line. This simple "Wired-OR Video Multiplexer" can be easily implemented using the OPA682 as shown in Figure 4.

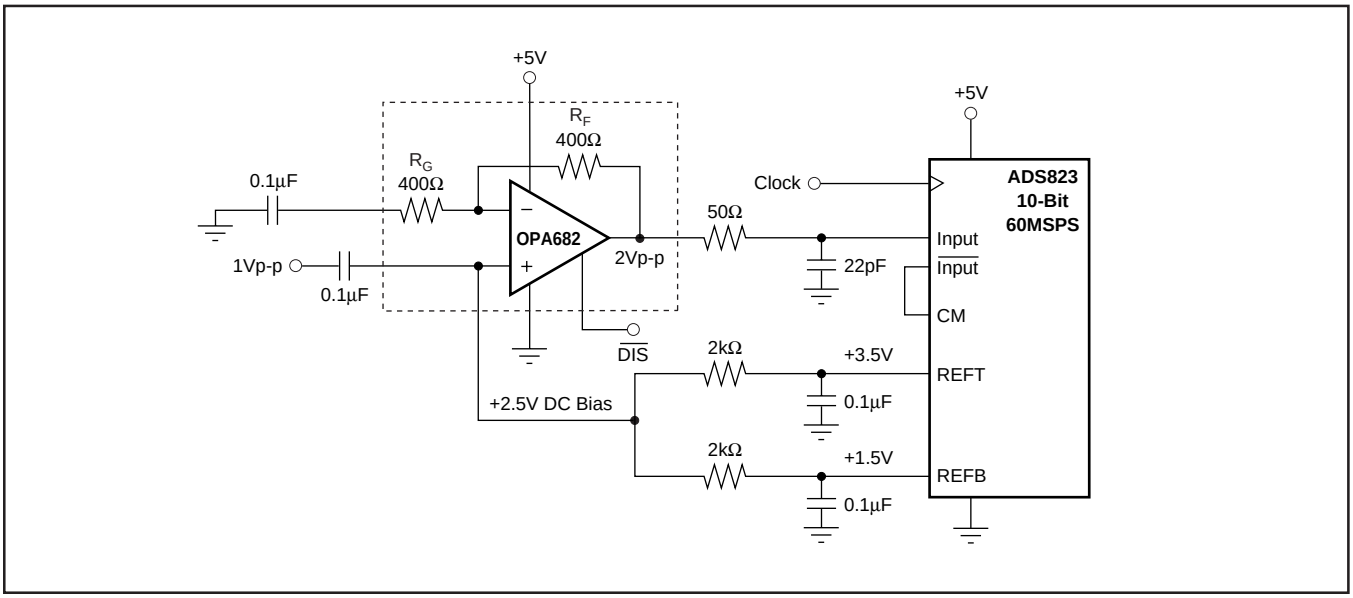


FIGURE 3. Wideband, AC-Coupled, Single-Supply A/D Driver.

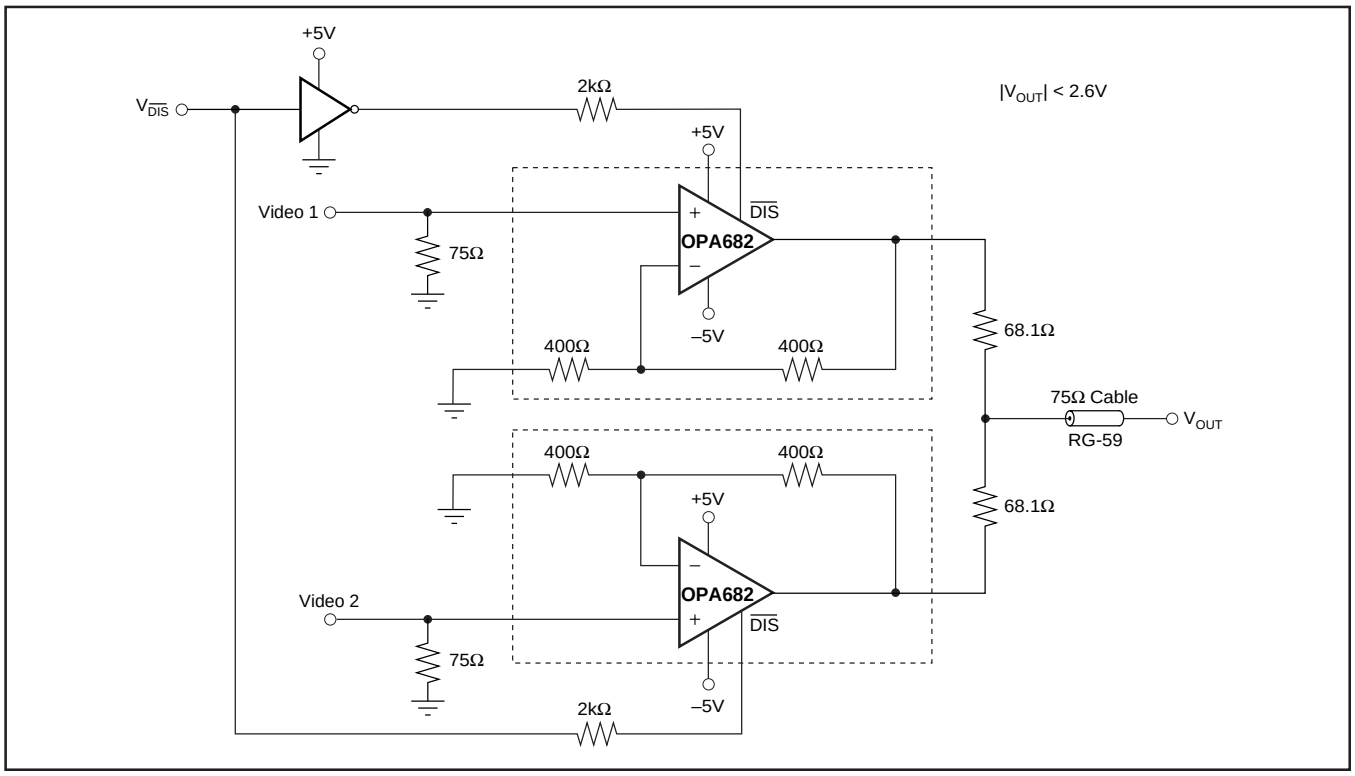


FIGURE 4. Two-Channel Video Multiplexer.

Typically, channel switching is performed either on sync or retrace time in the video signal. The two inputs are approximately equal at this time. The "make-before-break" disable characteristic of the OPA682 ensures that there is always one amplifier controlling the line when using a wired-OR circuit like that shown in Figure 4. Since both inputs may be on for a short period during the transition between channels, the outputs are combined through the output impedance matching resistors (68.1Ω in this case). When one channel is disabled, its feedback network forms part of the output impedance and slightly attenuates the signal in getting out onto the cable. The matching resistors have been set to get a signal gain of +1 at the load while providing > 20dB return loss at the load.

The video multiplexer connection (Figure 4) also insures that the maximum differential voltage across the inputs of the unselected channel do not exceed the rated ±1.2V maximum for standard video signal levels. In any case, V_{OUT} *must* be < ±2.6Vp-p in order to not exceed the absolute maximum differential input voltage (±1.2V) on the disabled part.

The section on Disable Operation shows the turn-on and turn-off switching glitches using a grounded input for a single channel is typically less than ±50mV. Where two outputs are switched (as shown in Figure 4), the output line is always under the control of one amplifier or the other due to the "make-before-break" disable timing. In this case, the switching glitches for two 0V inputs drop to < 20mV.

DELAY-EQUALIZED LOWPASS FILTER

The circuit in Figure 5 realizes a 5th-order Butterworth lowpass filter with a –3dB bandwidth of 20MHz and group delay equalization. This filter is based on the KRC active filter topology using amplifiers with a fixed positive gain ≥ 1.

The OPA682 makes a good amplifier for this type of filter. The first stage is the group delay equalizer, which is based on a gain of –1. The second stage has a high-Q pole, and uses a gain of +2 for minimum component sensitivity. The second stage also produces a real pole. The last stage has a low-Q pole, and uses a gain of +1 for minimum component sensitivity.

The component values have been pre-distorted to compensate for the op amps's parasitic effects. The low-Q pole section was placed last to minimize noise peaking in the passband, while maintaining good dynamic range performance.

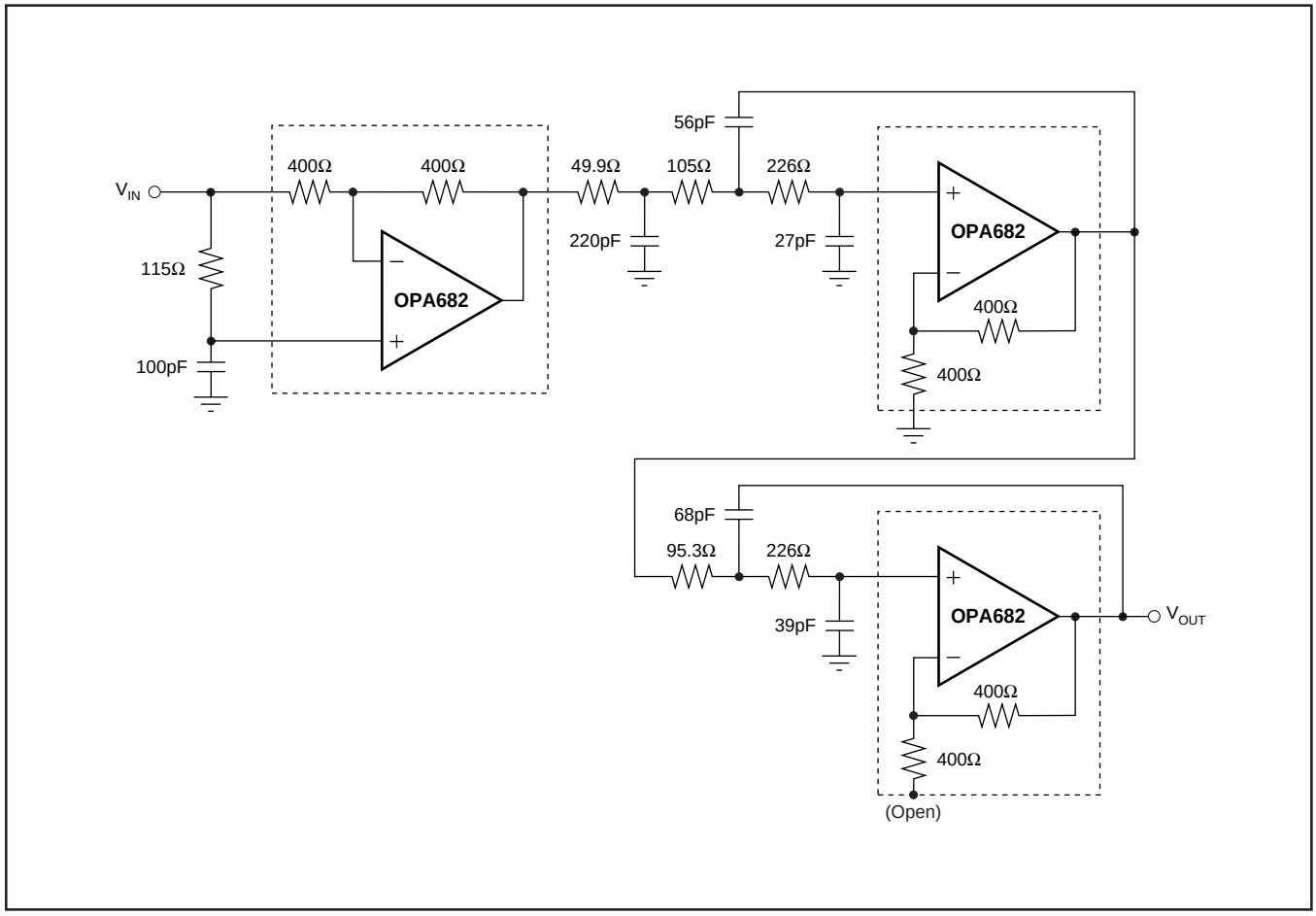


FIGURE 5. Butterworth LP Filter with Delay Equalization.

PRECISION VOLTAGE BUFFER

The precision buffer in Figure 6 combines the DC precision and low 1/f noise of the OPA227 with the high speed performance of the OPA682. The 80.6kΩ resistor makes the high frequency and low frequency nominal gains equal. The OPA682 takes over from the OPA227 at approximately 32kHz.

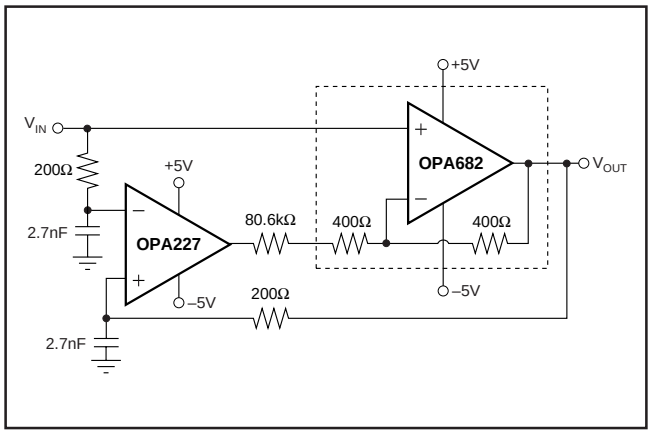


FIGURE 6. Precision Wideband, Unity Gain Buffer.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Several PC boards are available to assist in the initial evaluation of circuit performance using the OPA682 in its three package styles. All of these are available free as an unpopulated PC board delivered with descriptive documentation. The summary information for these boards is shown in the table below.

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA682P	8-Pin DIP	DEM-OPA68xP	MKT-350
OPA682U	8-Lead SO-8	DEM-OPA68xU	MKT-351
OPA682N	6-Lead SOT23-6	DEM-OPA68xN	MKT-348

Contact the Burr-Brown applications support line to request any of these boards.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA682 is available through the Burr-Brown Internet web page (http://www.burr-brown.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortions, temperature or dG/dϕ characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

GAIN SETTING

Setting the gain with the OPA682 is very easy. For a gain of +2, ground the –IN pin and drive the +IN pin with the signal. For a gain of +1, leave the –IN pin open and drive the +IN pin with the signal. For a gain of –1, ground the +IN pin and drive the –IN pin with the signal. Since the internal resistor values (but not their ratio) change significantly over temperature and process, external resistors should not be used to modify the gain.

OUTPUT CURRENT AND VOLTAGE

The OPA682 provides output voltage and current capabilities that are unsurpassed in a low cost monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1V to either supply rail; the guaranteed swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is guaranteed to deliver more than ±135mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage x current, or V-I product, which is more relevant to circuit operation. Refer to the "Output Voltage and Current Limitations" plot in the Typical Performance Curves. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA682's output drive capabilities, noting that the graph is bounded by a "Safe Operating Area" of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA682 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability, as shown in the Typical Specifications.

The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the guaranteed tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their VBE's (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power supply pin will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power supply

leads. This will, under heavy output loads, reduce the available output voltage swing. A 5Ω series resistor in each power supply lead will limit the internal power dissipation to less than 1W for an output short circuit while decreasing the available output voltage swing only 0.5V for up to 100mA desired load currents. Always place the 0.1µF power supply decoupling capacitors after these supply current limiting resistors directly on the supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter—including additional external capacitance which may be recommended to improve A/D linearity. A high-speed amplifier like the OPA682 can be very susceptible to decreased stability and frequency response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Performance Curves show the recommended R_S vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA682. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA682 output pin (see Board Layout Guidelines).

DISTORTION PERFORMANCE

The OPA682 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +5V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd harmonic will dominate the distortion with a negligible 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network-in the non-inverting configuration (Figure 1) this is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Performance Curves show the 2nd harmonic increasing at a little less than the expected 2X rate while the 3rd harmonic increases at a little less than the expected 3X rate. Where the test power doubles, the difference between it and the 2nd harmonic decreases less than the expected 6dB while the difference between it and the 3rd decreases by less than the expected 12dB. This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Performance Curves show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (i.e., 2Vp-p for each tone at the load, which requires 8Vp-p for the overall 2-tone envelope at the output pin), the Typical Performance Curves show 62dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies.

NOISE PERFORMANCE

The OPA682 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (15pA/$\sqrt{\text{Hz}}$) is significantly lower than earlier solutions while the input voltage noise (2.2nV$\sqrt{\text{Hz}}$) is lower than most unity gain stable, wideband, voltage feedback op amps. This low input voltage noise was achieved at the price of higher non-inverting input current noise (12pA/$\sqrt{\text{Hz}}$). As long as the AC source impedance looking out of the non-inverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise for the gain settings, available using the OPA682. Figure 7 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{\text{Hz}}$ or pA/$\sqrt{\text{Hz}}$.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 7.

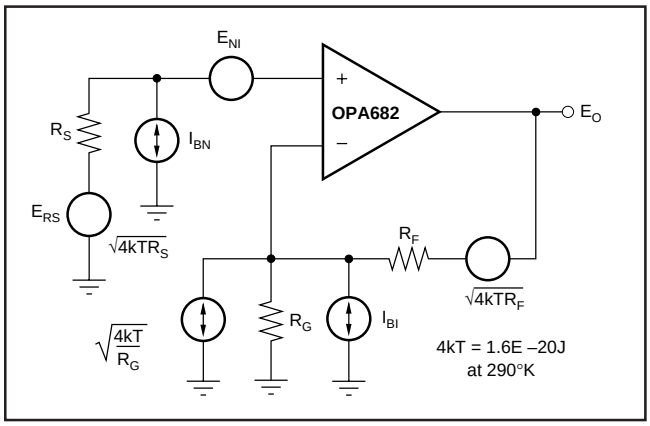


FIGURE 7. Noise Model.

Eq.1

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain (NG = $(1+R_F/R_G)$) will give the equivalent input-referred spot noise voltage at the non-inverting input as shown in Equation 2.

Eq. 2

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Evaluating these two equations for the OPA682 circuit and component values shown in Figure 1 will give a total output spot noise voltage of 8.4nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 4.2nV/$\sqrt{Hz}$. This total input-referred spot noise voltage is higher than the 2.2nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor.

DC ACCURACY

The OPA682 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Typical Specifications show an input offset voltage comparable to high speed voltage feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Bias current cancellation techniques will not reduce the output DC offset for OPA682. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$\pm(NG \cdot V_{OS}(max)) + (I_{BN} \cdot R_S/2 \cdot NG) \pm (I_{BI} \cdot R_F)$

where NG = non-inverting signal gain

$= \pm(2 \cdot 5.0mV) + (55\mu A \cdot 25\Omega \cdot 2) \pm (480\Omega \cdot 40\mu A)$

$= \pm 10mV + 2.8mV \pm 19.2mV$

$= -26.4mV \rightarrow +32.0mV$

Minimizing the resistance seen by the non-inverting input will give the best DC offset performance.

For significantly improved DC accuracy, consider the precision buffer circuit shown in Figure 6.

DISABLE OPERATION

The OPA682 provides an optional disable feature that may be used either to reduce system power or to implement a simple channel multiplexing operation. If the DIS control pin is left unconnected, the OPA682 will operate normally. To disable, the control pin must be asserted low. Figure 8 shows a simplified internal circuit for the disable control feature.

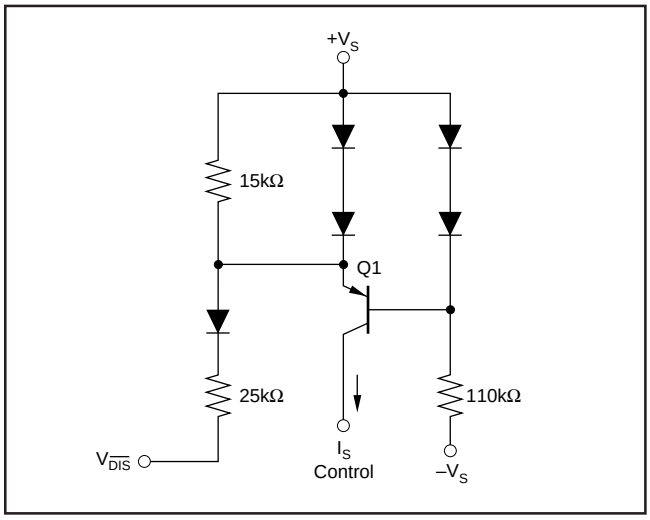


FIGURE 8. Simplified Disable Control Circuit.

In normal operation, base current to Q1 is provided through the 110kΩ resistor while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 15kΩ resistor eventually turning on these two diodes (≈ 100µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately zero volts. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode is only that required to operate the circuit of Figure 8. Additional circuitry ensures that turn-on time occurs faster than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high impedance state. If the OPA682 is operating in a gain of +1, this will show a very high impedance (4pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain of +2, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured at a gain of –1 the input and output will be connected through the feedback network resistance ($R_F + R_G$) giving relatively poor input to output isolation.

One key parameter in disable operation is the output glitch when switching in and out of the disabled mode. Figure 9 shows these glitches for the circuit of Figure 1 with the input signal set to zero volts. The glitch waveform at the output pin is plotted along with the $\overline{DIS}$ pin voltage.

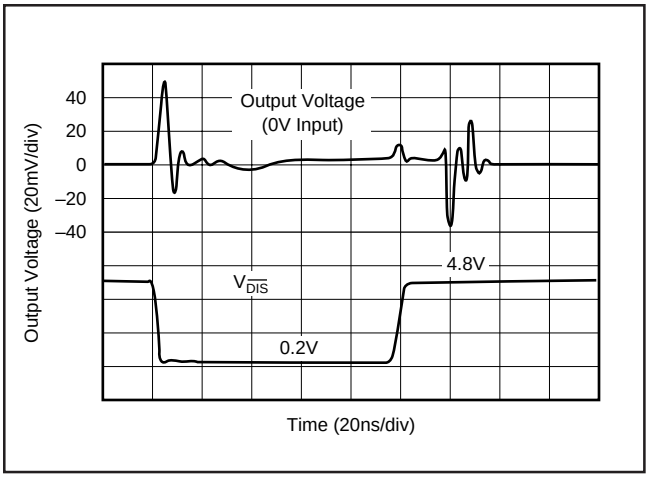


FIGURE 9. Disable/Enable Glitch.

The transition edge rate (dV/dt) of the $\overline{DIS}$ control line will influence this glitch. For the plot of Figure 9, the edge rate was reduced until no further reduction in glitch amplitude was observed. This approximately 1V/ns maximum slew rate may be achieved by adding a simple RC filter into the V_{DIS} pin from a higher speed logic line. If extremely fast transition logic is used, a 2kΩ series resistor between the logic gate and the $\overline{DIS}$ input pin will provide adequate bandlimiting using just the parasitic input capacitance on the $\overline{DIS}$ pin while still ensuring an adequate logic level swing.

THERMAL ANALYSIS

Due to the high output power capability of the OPA682, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA682N (SOT23-6 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 20Ω load to +2.5V DC:

$P_D = 10V \bullet 7.2mA + 5^2/(4 \bullet (20\Omega \parallel 800\Omega)) = 392mW$

Maximum $T_J = +85°C + (0.39W \bullet 150°C/W) = 144°C$

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower guaranteed junction temperatures. Remember, this is a worst-case internal power dissipation-use your actual signal and load to compute P_{DL}. The highest possible internal dissipation will occur if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors. The Output Voltage and Current Limitations plot shown in the Typical Performance Curves include a boundary for 1W maximum internal power dissipation under these conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high frequency amplifier like the OPA682 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output pin can cause instability: on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections (on pins 4 and 7) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA682. Any external resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound type resistors in a high frequency application. All external components should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA682 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the Distortion vs Load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA682 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA682 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive Load. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high speed part like the OPA682 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA682 onto the board. If socketing for the DIP package is desired, high frequency flush-mount pins (e.g., McKenzie Technology #710C) can give good results.

INPUT AND ESD PROTECTION

The OPA682 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins have limited ESD protection using internal diodes to the power supplies as shown in Figure 10.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA682), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

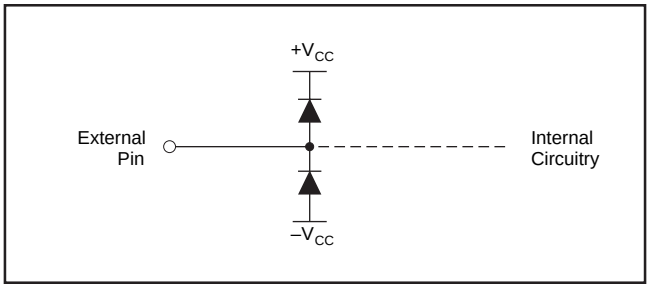


FIGURE 10. Internal ESD Protection.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA682N/250	OBSOLETE	SOT-23	DBV	6		TBD	Call TI	Call TI
OPA682N/3K	OBSOLETE	SOT-23	DBV	6		TBD	Call TI	Call TI
OPA682P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA682U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
OPA682U/2K5	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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