8-Mbit (512K x 16) Static RAM

Features

- **Very high speed: 45 ns**
- **Wide voltage range: 1.65V–2.25V**
- **Pin Compatible with CY62157DV18 and CY62157DV20**
- **Ultra-low standby power**
  - **— Typical Standby current: 2µA**
  - **— Maximum Standby current: 8µA**
- **Ultra-low active power**
  - **— Typical active current: 1.8 mA @ f = 1 MHz**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in lead-free 48-ball VFBGA package**

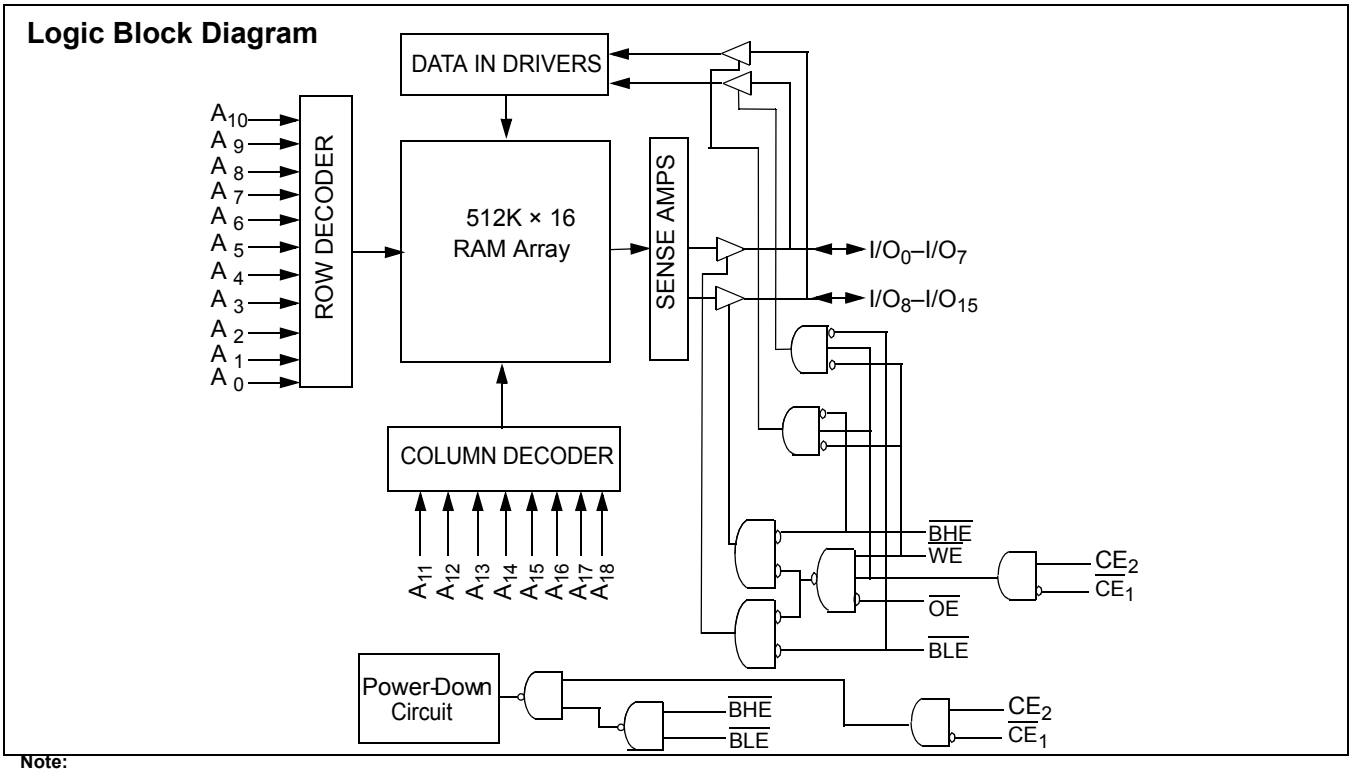
Functional Description[1]

The CY62157EV18 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this datasheet for a complete description of read and write modes.

Logic Block Diagram

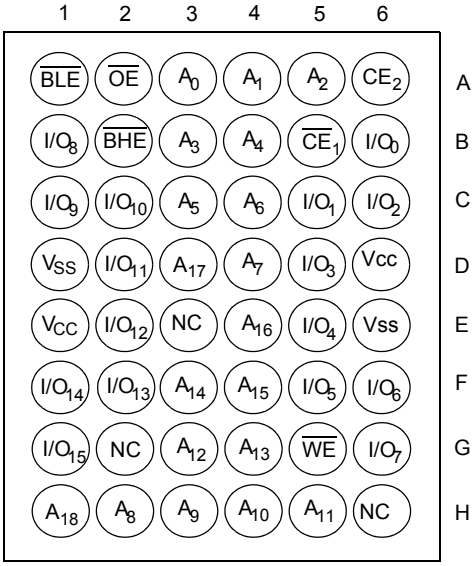


Note:
1. For best practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration[2]

FBGA

Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
					f = 1MHz		f = f_{max}			
	Min.	Typ.[3]	Max.		Typ.[3]	Max.	Typ.[3]	Max.	Typ.[3]	Max.
CY62157EV18	1.65	1.8	2.25	45	1.8	3	18	25	2	8

Notes:
2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied .....–55°C to + 125°C

Supply Voltage to Ground Potential .....–0.2V to 2.45V (V_{CCMAX} + 0.2V)

DC Voltage Applied to Outputs in High Z State[4, 5] .....–0.2V to 2.45V (V_{CCMAX} + 0.2V)

DC Input Voltage[4, 5] ..... –0.2V to 2.45V (V_{CCMAX} + 0.2V)

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62157EV18LL	Industrial	–40°C to +85°C	1.65V to 2.25V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min.	Typ.[3]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 1.65V	1.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 1.65V			0.2	V
V_{IH}	Input HIGH Voltage	V_{CC} = 1.65V to 2.25V		1.4		V_{CC} + 0.2V	V
V_{IL}	Input LOW Voltage	V_{CC} = 1.65V to 2.25V		–0.2		0.4	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels		18	25	mA
		f = 1 MHz			1.8	3	mA
I_{SB1}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC}–0.2V or CE_2 ≤ 0.2V V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V) f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$), V_{CC} = V_{CC} (max).			2	8	µA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = V_{CC} (max).			2	8	µA

Capacitance[7]

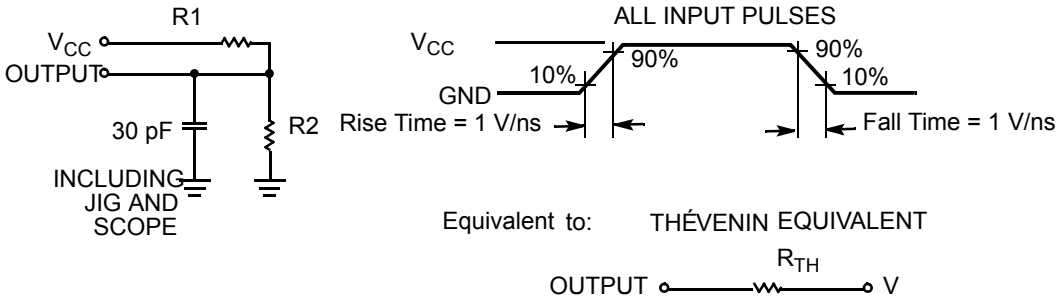
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
4. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
5. $V_{IH(max.)}$ = V_{CC} + 0.5V for pulse durations less than 20 ns.
6. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
7. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[7]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	72	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[7]		8.86	°C/W

AC Test Loads and Waveforms

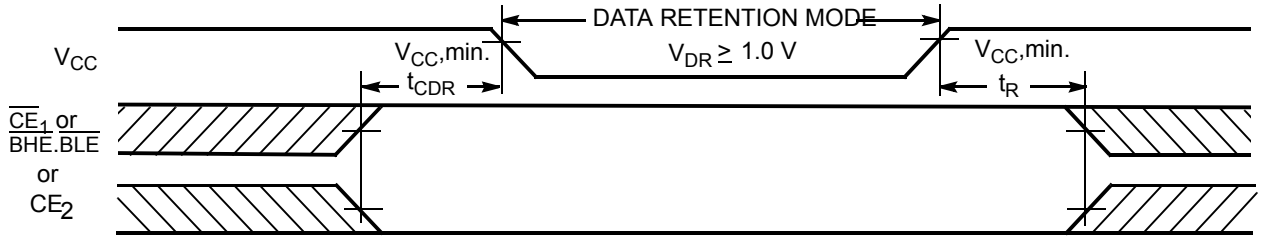


Parameters	Value	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics[9] (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0			V
I_{CCDR}	Data Retention Current	V_{CC}= V_{DR} $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	3	µA
t_{CDR}[7]	Chip Deselect to Data Retention Time		0			ns
t_R[8]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform[9]



Note:
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.
9. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

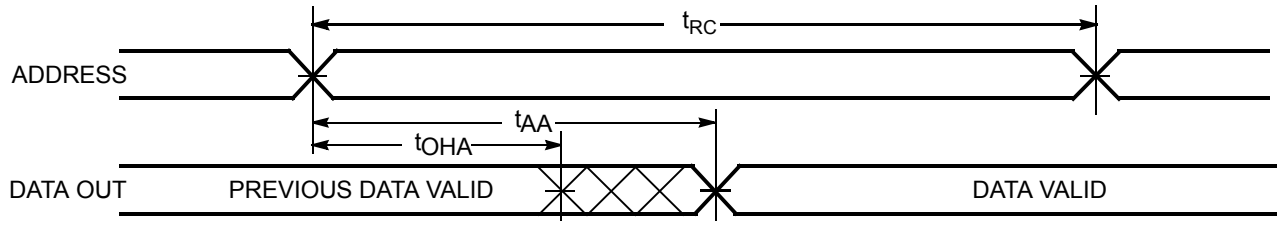
Switching Characteristics Over the Operating Range [10]

Parameter	Description	45 ns		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[11]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 12]		18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[11]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[11, 12]		18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power-Down		45	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45	ns
t_{LZBE}[13]	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[11]	5		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[11, 12]		18	ns
Write Cycle[14]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35		ns
t_{AW}	Address Set-Up to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35		ns
t_{SD}	Data Set-Up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[11, 12]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11]	10		ns

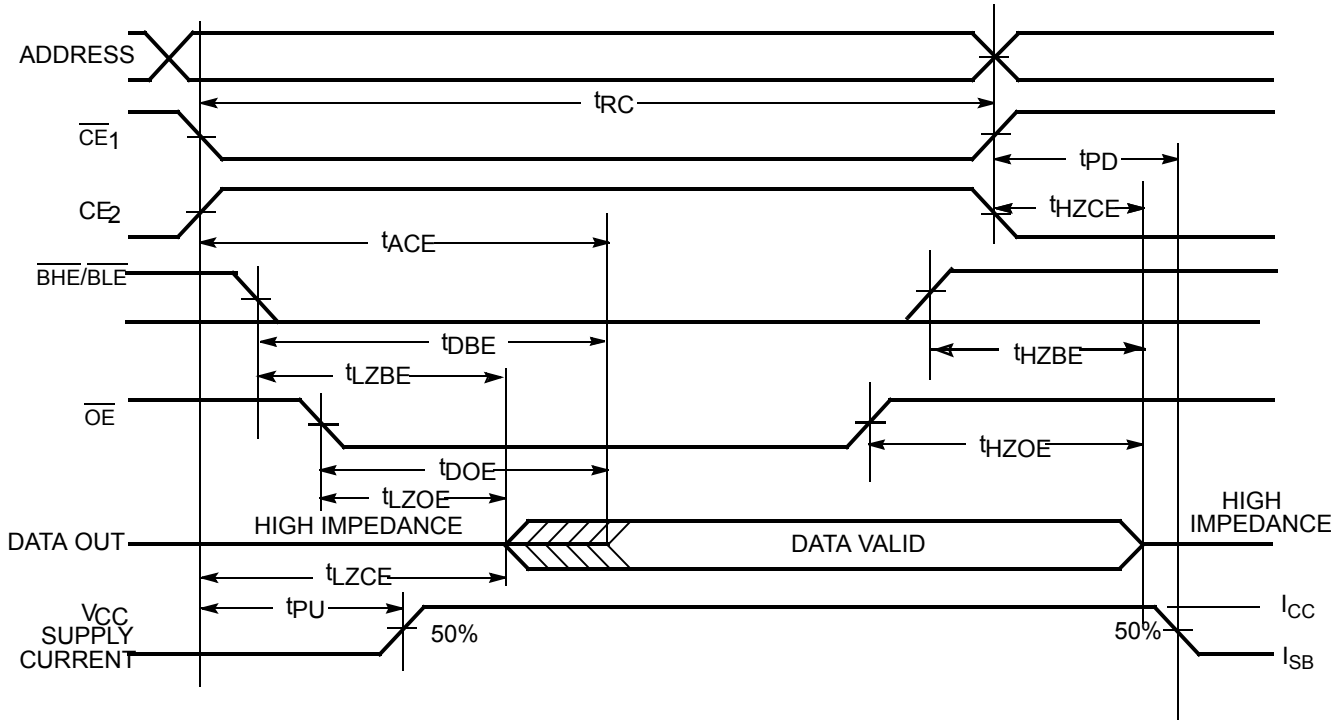
Notes:
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the “AC Test Loads and Waveforms” section.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
13. If both byte enables are toggled together, this value is 10 ns.
14. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[15, 16]



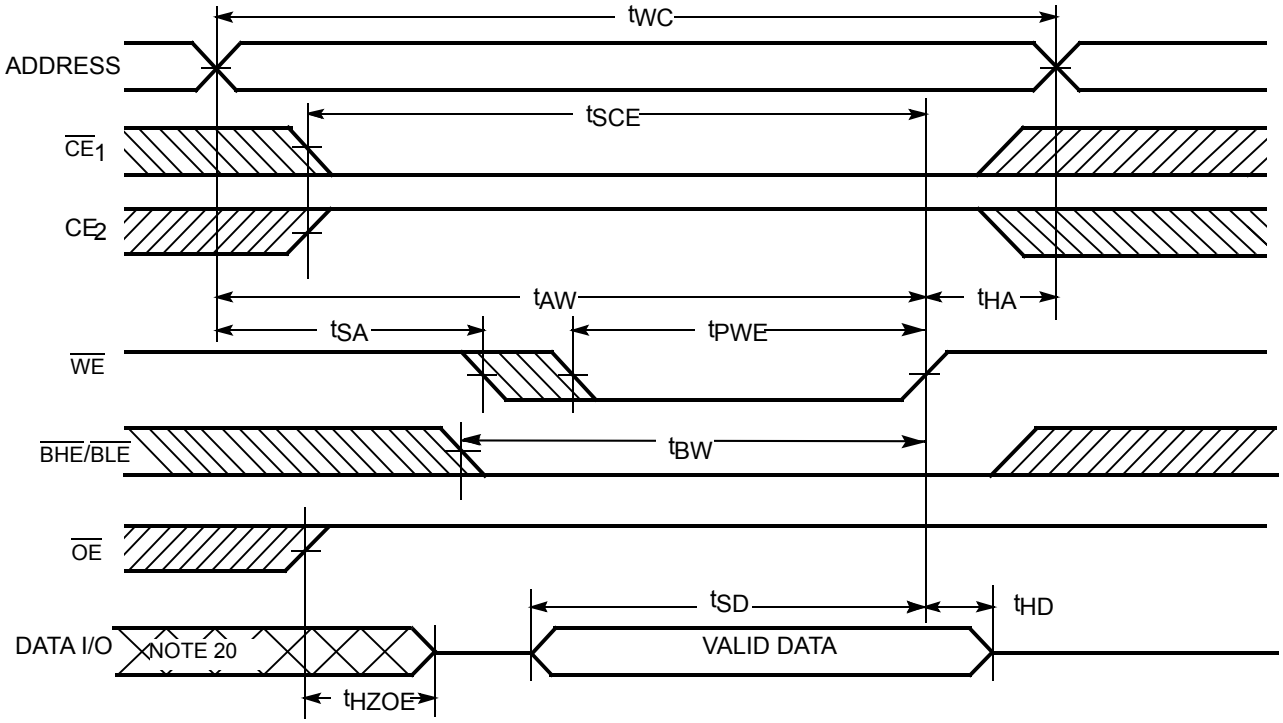
Read Cycle 2 (OE Controlled)[16, 17]



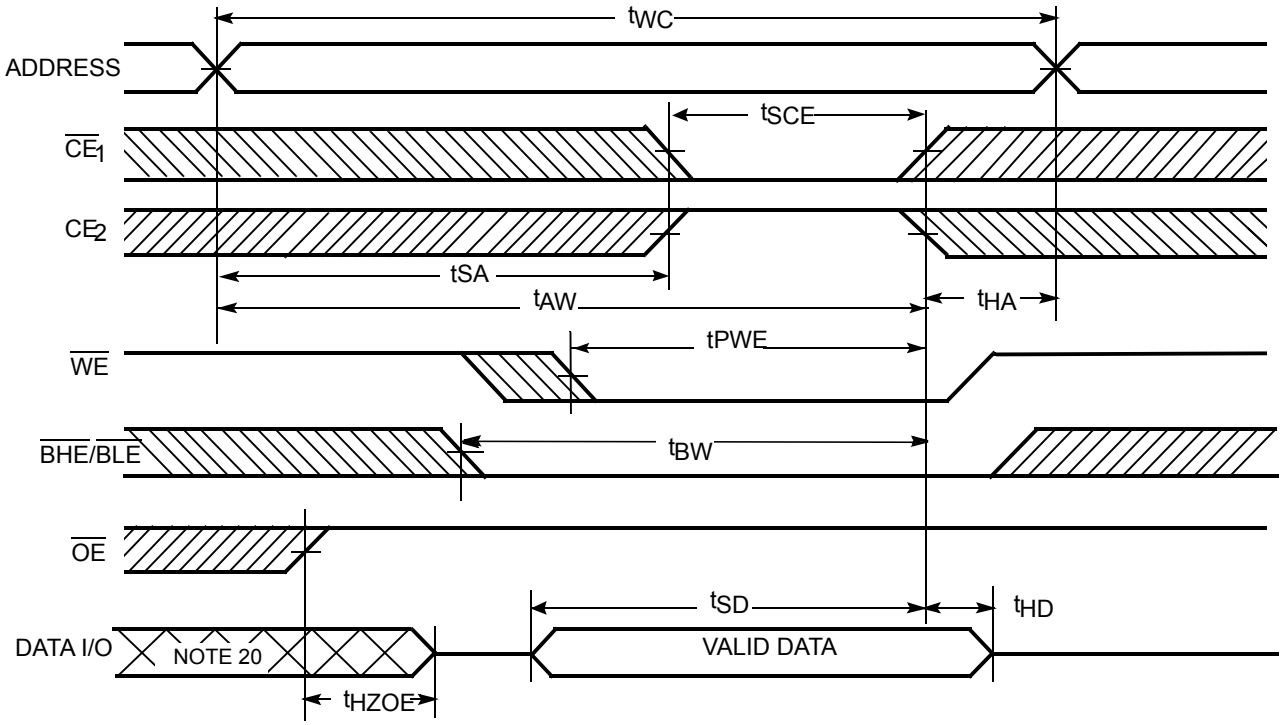
Notes:
15. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle 1 ($\overline{WE}$ Controlled)[14, 18, 19, 20]



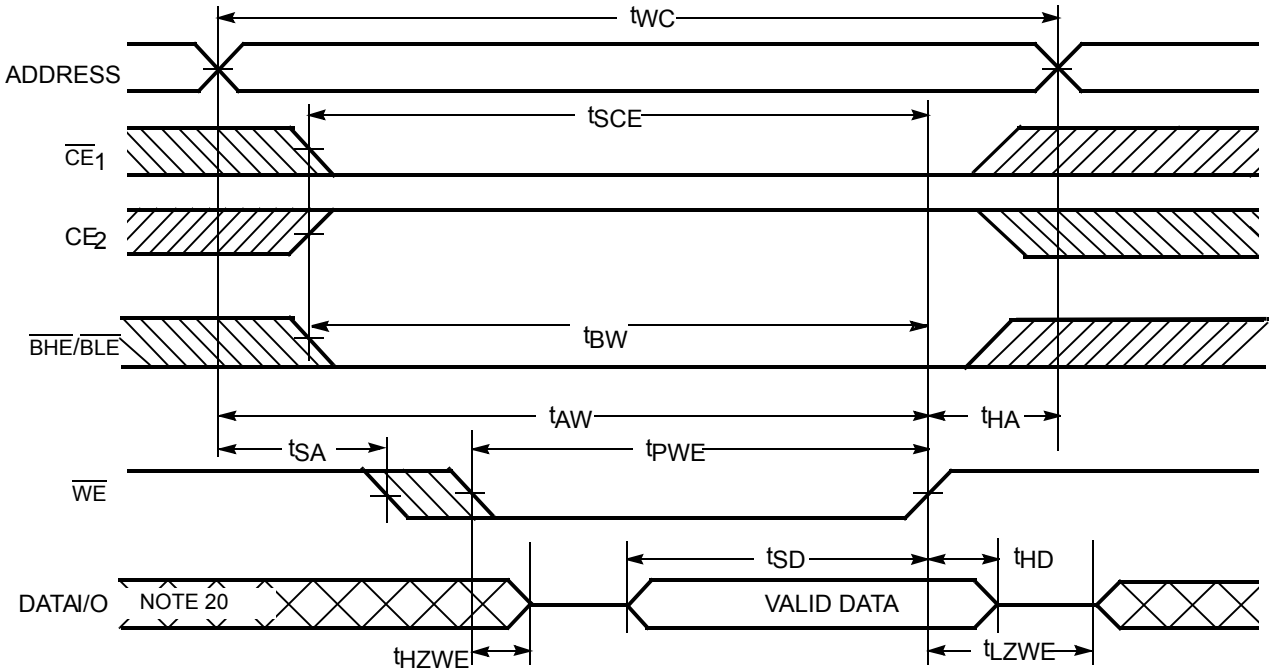
Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled)[14, 18, 19, 20]



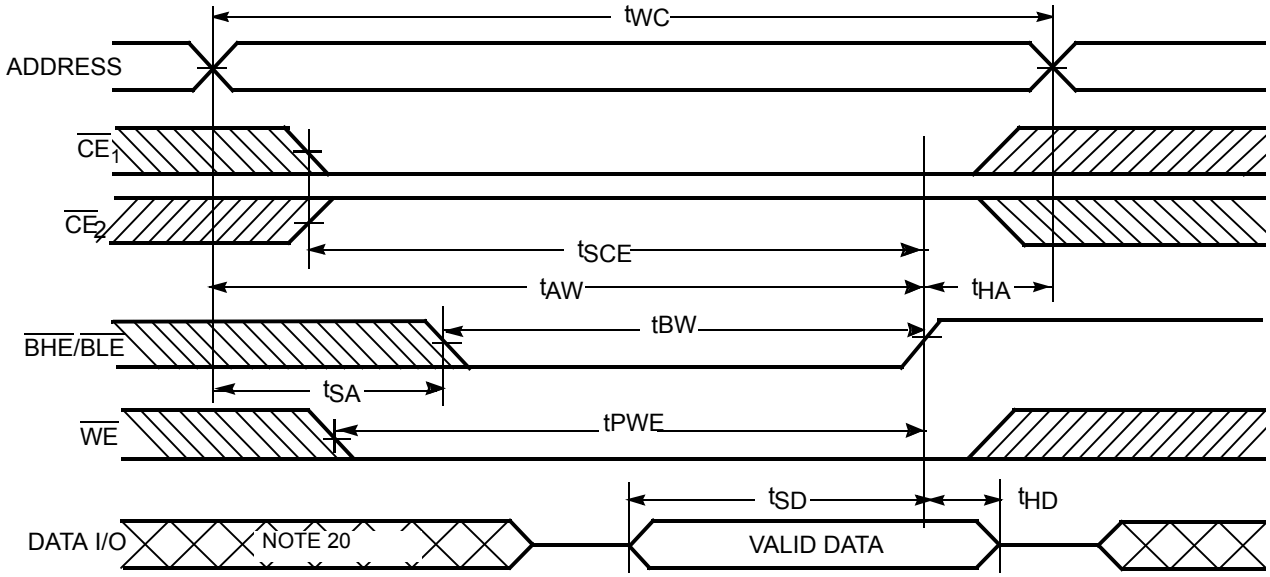
Notes:
18. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
19. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high-impedance state.
20. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 (WE Controlled, OE LOW)[19, 20]



Write Cycle 4 (BHE/BLE Controlled, OE LOW)[19, 20]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

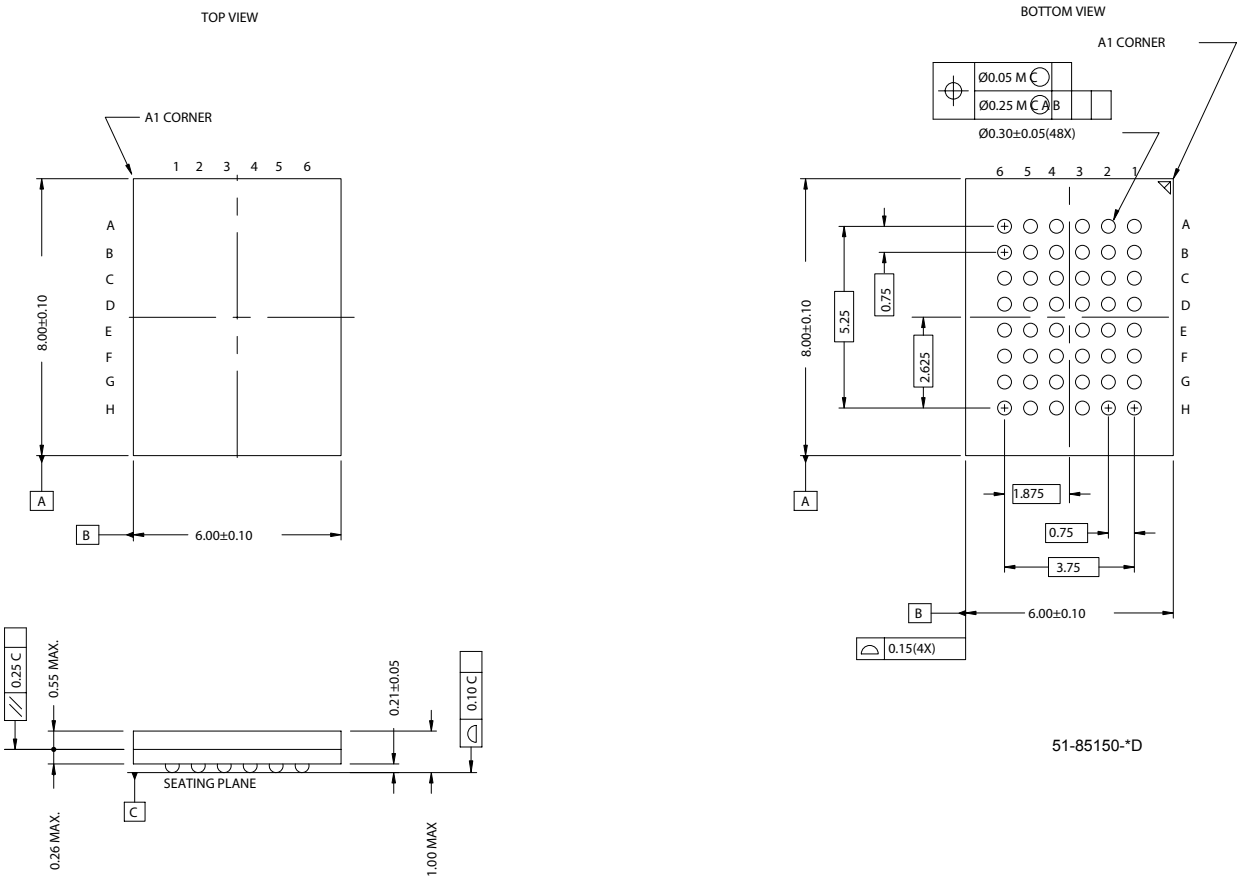
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157EV18LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Industrial

Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



Document History Page

Document Title: CY62157EV18 MoBL® 8-Mbit (512K x 16) Static RAM Document Number:38-05490				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	202862	See ECN	AJU	New Data Sheet
*A	291272	See ECN	SYT	Converted from Advance Information to Preliminary Changed V_{CC} Max from 2.20 to 2.25 V Changed V_{CC} stabilization time in footnote #7 from 100 μs to 200 μs Changed I_{CCDR} from 4 to 4.5 μA Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bins Changed t_{DOE} from 15 and 22 ns to 18 and 22 ns for the 35 and 45 ns Speed Bins respectively Changed t_{HZOE}, t_{HZBE} and t_{HZWE} from 12 and 15 ns to 15 and 18 ns for the 35 and 45 ns Speed Bins respectively Changed t_{HZCE} from 12 and 15 ns to 18 and 22 ns for the 35 and 45 ns Speed Bins respectively Changed t_{SCE}, t_{AW} and t_{BW} from 25 and 40 ns to 30 and 35 ns for the 35 and 45 ns Speed Bins respectively Changed t_{SD} from 15 and 20 ns to 18 and 22 ns for the 35 and 45 ns Speed Bins respectively Added Lead-Free Package Information
*B	444306	See ECN	NXR	Converted from Preliminary to Final. Removed 35 ns speed bin Removed “L” bin Changed ball E3 from DNU to NC Removed redundant footnote on DNU. Modified Maximum Ratings spec for Supply Voltage and DC Input Voltage from 2.4V to 2.45V Changed the I_{CC} Typ. value from 16 mA to 18 mA and I_{CC} Max. value from 28 mA to 25 mA for test condition f = fax = $1/t_{RC}$. Changed the I_{CC} Max. value from 2.3 mA to 3 mA for test condition f = 1MHz. Changed the I_{SB1} and I_{SB2} Max. value from 4.5 μA to 8 μA and Typ. value from 0.9 μA to 2 μA respectively. Updated Thermal Resistance table Changed Test Load Capacitance from 50 pF to 30 pF. Added Typ. value for I_{CCDR} . Changed the I_{CCDR} Max. value from 4.5 μA to 3 μA Corrected t_R in Data Retention Characteristics from 100 μs to t_{RC} ns Changed t_{LZOE} from 3 to 5 Changed t_{LZCE} from 6 to 10 Changed t_{HZCE} from 22 to 18 Changed t_{LZBE} from 6 to 5 Changed t_{PWE} from 30 to 35 Changed t_{SD} from 22 to 25 Changed t_{LZWE} from 6 to 10 Added footnote #13 Updated the ordering Information and replaced the Package Name column with Package Diagram.