Features

Harris FCT is a broad family of 8-bit, 9-bit and 10-bit computer-bus interface logic ICs. Harris FCT BiCMOS Bus-Interface ICs are designed to satisfy four major requirements of modern bus-oriented computer systems, namely:

- High Speed/Low Propagation Delay
- High Drive, to Meet Specified Bus-Interface Requirements for Clock and Data Lines
- Low Power Consumption (CMOS-Like)
- Minimization of Switching Noise

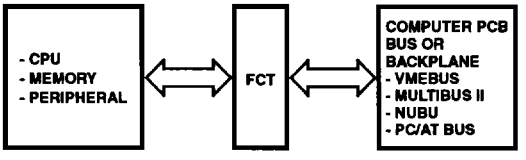


FIGURE 1. FCT AS BUS-INTERFACE ICs

NOTE: Harris offers FCT products in two speed grades: base speed (equal to FAST speeds) and higher speed (on average, 30% faster). The base speed version of each type is designated as either FCT or FCTXXXA, and the higher speed version, FCTXXXAT. The "T" was added to the suffix in order to highlight the fact that Harris FCT devices have a TTL-like output swing. Throughout this technical overview, FCT, FCTXXXA, FCTXXXAT are referred to collectively as FCT.

Clearly there is no other bus-interface logic family that meets all four of these system requirements as well as Harris FCT does. Other bus-interface families such as AS, F (FAST), BCT, and BC have higher power consumption (See Figure 2) and lower speed (See Figure 3). Also, the Harris BiCMOS technology, being CMOS based with only modest additional complexity for the bipolar circuitry, has lower manufacturing costs than other more complex BiCMOS processes.

For non-8-bit, non-9-bit and non-10-bit bus-interface functions, the logic family of choice for low-power, advanced high speed performance is the Harris AC/ACT family.

The many excellent features of the new Harris FCT BiCMOS bus-interface logic family are detailed in Table 1.

TABLE 1. FEATURES OF THE HARRIS FCT FAMILY

FEATURES		
High Speed, Typical Delay = 3.5ns FCTXXXAT is faster than FAST		
Low Power	Typical Power/Function	
Quiescent	0mW	
5MHz	5.6mW	
10MHz	11.2mW	
Output Sink Current		
Buffers	64mA, +70°C	
FF/Latches	48mA, +70°C	
Limited Output Voltage Swing (for reduced noise generation) 3.5V Typical		
No Diode Clamps from Inputs or Outputs to V_{CC}		
Minimized Switching Noise Design, Layout, and Packaging		
Low Ground Bounce - Typically 1.2V		
Reduced EMI Due to Slowed Output Edges		
Good Input Dynamic Noise Immunity (via isolated ground system and input hysteresis)		
ESD: ±2kV (HBM)		
Not Latch-Up to Above ±300mA		
Variety of Bus-Interface Functions		
Buffers	Octal	
	10-Bit	
Flip-Flops/Registers	Octal	
	9-Bit	
	10-Bit	
	Special Registers	
Transceivers	Octal	
	9-Bit	
	10-Bit	
Latches	Octal	
	9-Bit	
	10-Bit	

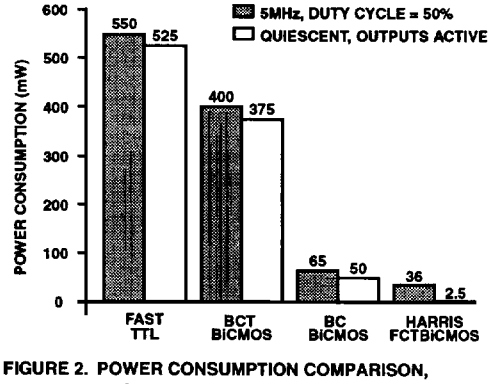


FIGURE 2. POWER CONSUMPTION COMPARISON, BUS-INTERFACE LOGIC FAMILIES

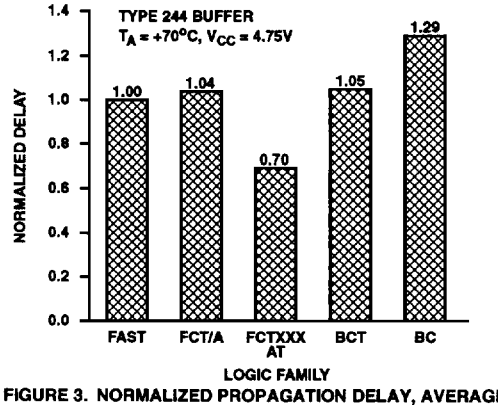


FIGURE 3. NORMALIZED PROPAGATION DELAY, AVERAGE OF t_{PLH}, t_{PHL}, t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH} MAXIMUMS (ADJUSTED FOR TEMPERATURE AND VOLTAGE WHERE NECESSARY)

Applications

Meeting Bus Standards

As illustrated in Table 2, Harris FCT bus-interface ICs match up ideally to the popular VMEbus, Multibus II, and other open or proprietary bus standards that require similar high speed performance and high sink-current capability.

TABLE 2. 32-BIT COMPUTER BUS STANDARDS

BUS	IEEE STD. NO.	DRIVER TECHNOLOGY
VMEbus	1014	TTL/FCT
NuBus	1196	TTL/FCT
Multibus II	1296	TTL/FCT
IBM Micro Channel Architecture (MCA)	None	TTL/FCT
Extended Industry Standard Architecture (EISA)	None	TTL/FCT
Sun Microsystems Sbus	None	CMOS/FCT

FCT vs AC/ACT Use

The new Harris FCT bus-interface products complement the existing popular Harris AC/ACT logic family. The fundamental difference between these two families is that FCT is capable of sinking the 48mA or 64mA required for back-plane interface, while the AC/ACT family parts provide a balanced ±24mA output drive current capability in all logic and bus-interface family members. Table 3 describes the application of FCT vs AC/ACT.

FCT IC Process Technology

Harris FCT devices are fabricated in a 1.5µm BiCMOS process (See Figure 4). The basis of this process is a silicon-gate CMOS, double-level-metal, N-well configuration. To this, the necessary steps are added to create an additional physical layer called P ISO. The P ISO layer is used to construct uncommitted diodes and uncommitted bipolar NPN transistors. (Intrinsic diodes and bipolar transistors exist in processes that lack this additional layer, i.e. pure CMOS processes, but these devices are not uncommitted).

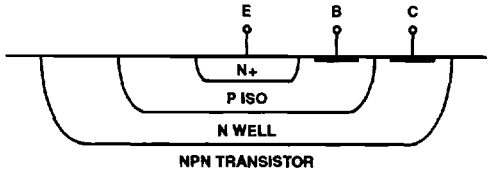
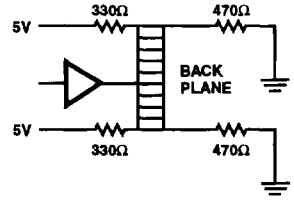
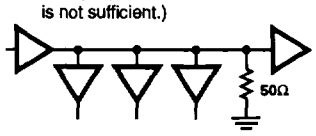


FIGURE 5. SIMPLIFIED DRAWING OF BIPOLAR NPN TRANSISTOR

A heavily doped P substrate is topped with a thin epitaxial layer of lightly doped P material. The heavy doping of the substrate and small geometries within the epitaxial layer minimize the resistances encountered in these regions, thereby virtually eliminating the occurrence of latch-up. Injected currents flow through the low impedance substrate to ground without triggering any parasitic SCRs (See Latch-Up Sensitivity in this section).

The self-aligning nature of the silicon-gate process serves to reduce parasitic capacitance associated with the CMOS transistors, thereby increasing performance of the circuitry. Two levels of metallization provide for more efficient routing of interconnect, power and ground lines.

TABLE 3. FCT vs AC/ACT APPLICATION

APPLICATION	FCT	AC/ACT
1. Drive Worst Case VME, Multibus II, or other backplane specified around higher power FAST TTL bus drivers. Requires 64mA sink current for clocks and strobes. 	Yes	No
2. Drive 50Ω PCB trace, coax, twisted pair, flat cable, etc. Maintain incident edge switching at both ends or any tap. (Source current of FCT is not sufficient.) 	No	Yes
3. Highest speed, lowest power, most noise immune logic system or bus interface system without line terminations	No	Yes (AC)
4. Driving memory input or CMOS Logic/ASIC inputs that require a balanced rail-to-rail logic swing	No	Yes
5. Bus Interfaces that need 24mA or less sink current	Yes	Yes
6. Interfaces between equipment with separate power supplies	Yes (No I/O Clamp Diodes)	No
7. Complete logic family including SSI (Gates) and MSI logic functions	No	Yes

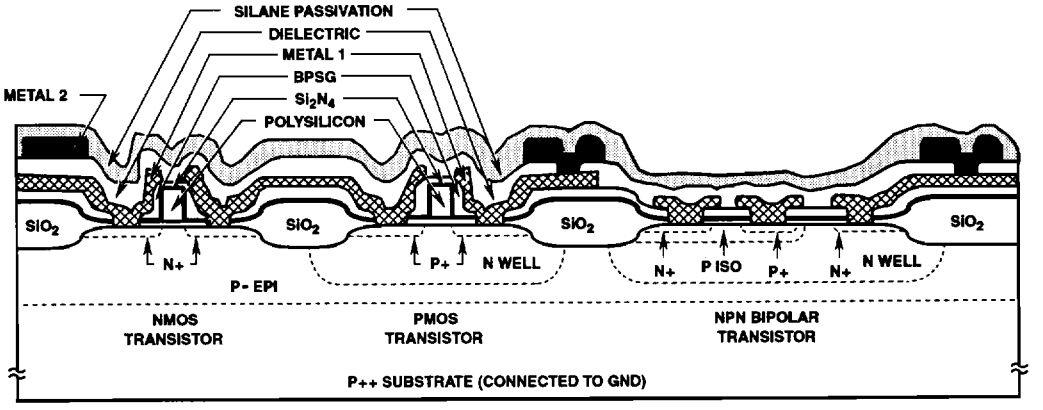


FIGURE 4. HARRIS FCT BiCMOS 1.5µm PROCESS CROSS SECTION

Input Protection

FCT device inputs are protected by the network shown in Figure 6. This network protects the device against electrostatic discharge (up to at least 2kV for the human body model), which occurs in the normal handling of such components, as well as transients associated with normal operation in a system environment.

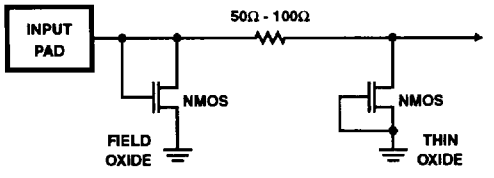


FIGURE 6. FCT INPUT PROTECTION NETWORK

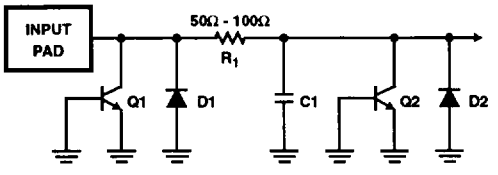


FIGURE 7. PARASITIC ELEMENTS IN THE CIRCUIT OF FIGURE 6

The operative elements in the protection mechanism are actually parasitic devices that exist in the network. These are shown in Figure 7. Whenever two N-type regions are formed within a P-type material to create an NMOS transistor, a parasitic NPN bipolar transistor results. The P-material, which is tied to ground, acts as the base. Q1 in Figure 7 is the NPN device associated with the field oxide NMOS transistor in Figure 6, and Q2 results from the construction of the thin oxide NMOS device. Diode D1 and Diode D2 are actually the base-collector junctions of transistor Q1 and transistor Q2, respectively, but are drawn separately for illustration. Primary protection is provided by Q1, which will go into breakdown for positive input voltages greater than about 15V. (The gate oxide of the input inverter that follows the protection can withstand up to about 25V to 30V). For negative input voltages, diode D1 simply conducts in the forward region. Secondary protection is provided by the remaining components, R1, C1, Q2 and D2. The combination of R1 and C1 will attenuate high speed transients, and Q2/D2 will behave in a similar manner to Q1/D1. The field oxide NMOS device itself would turn on if the input reached a level of about 18V.

Input Structure

The circuit diagram for the input structure of Harris FCT devices is shown in Figure 8.

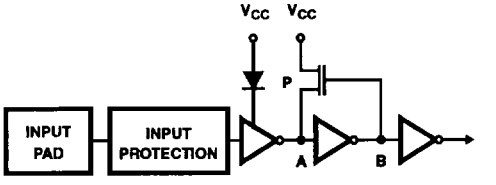


FIGURE 8. FCT INPUT STRUCTURE

The details of the input protection circuit are discussed in the preceding section. Following the input protection network is an inverter stage designed for TTL level inputs. The switchpoint of the inverter is lowered from the typical $V_{CC}/2$ value for CMOS level inputs to a value near the middle of the range between the TTL V_{IH} and V_{IL} limits. A simple method for lowering the switchpoint of an inverter is to increase the width of the N-transistor. However, using this method alone requires a considerable increase in the size of the N-transistor. The total increase in chip area becomes significant when this is done for all inputs. So, instead of using all of this chip area, Harris has added a diode to the V_{CC} line of the inverter. The diode itself lowers the switchpoint by one diode drop, thereby allowing for a much smaller increase in the width of the N-transistor.

The diode also lowers the output high level of the input inverter by one diode drop. So, in order to reduce flow-through current in the next stage, a P-transistor pull-up is used. This device turns on after node A switches high and node B switches low, and then pulls node A all the way up to the rail.

An additional benefit of the P-transistor is that it requires a slightly higher input voltage to switch node A back low again. This input hysteresis provides added immunity against ground bounce and other similar transients on the inputs.

Output Structure

The circuit diagram for the output stage used in Harris FCT devices is shown in Figure 9.

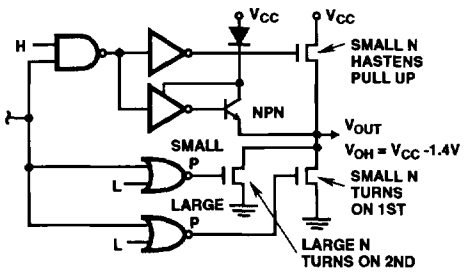


FIGURE 9. HARRIS FCT OUTPUT STAGE

Output Source Structure

The pull-up structure of FCT outputs is designed to eliminate the intrinsic protection diode from the output to V_{CC}, and to limit the output high voltage (V_{OH}) to 2 diode drops below V_{CC}.

The intrinsic protection diode to V_{CC} is removed by eliminating the P-transistor that would appear in a pure CMOS output structure. Instead of a P-channel pull-up, a bipolar NPN transistor in an emitter follower configuration is used. A small N-transistor is also used in parallel with the NPN, but the former drops out as the output voltage rises (i.e. as its gate to source voltage decreases). The benefits of eliminating the intrinsic diode to V_{CC} are ease of application in bus systems utilizing multiple power supplies, and in battery backed-up systems or other systems that are partially powered down. To provide protection for the outputs, a protection network is used that is similar to the input protection network, but without the series resistor.

The supply level for the collector of the NPN transistor and the inverter preceding the transistor is one diode drop below the V_{CC} level for the rest of the chip. The high level output of the inverter (i.e. the base of the NPN) is thus limited to one diode drop below V_{CC}. In turn, the high level voltage at the output pin, from the emitter of the NPN transistor, follows the base voltage minus the diode drop across the base emitter junction. The advantages of a reduced output swing are reduced ground bounce and reduced EMI generation. Both of these result from the slower edge rate produced by decreasing the change in voltage for a given change in time. More information on ground bounce and EMI is available in other sections of this overview and in the references listed at the end of the overview.

Output Sink Structure

The pull-down structure of FCT outputs (also shown in Figure 9) is designed to sink 48mA/64mA under static conditions (more on a dynamic basis), and to spread out over time the transient current associated with switching the outputs.

The distribution of transient current is achieved through the use of two, differently sized N-transistors in parallel. The logic gates driving the N-transistors are designed such that the smaller N turns on first. This smaller N-transistor discharges the capacitive load at a slower rate than the larger device, resulting in lower ground bounce. The larger N-transistor, which is needed to provide the bulk of the static drive capability, turns on after the transient current (and V_{OLP}) have already peaked (See Figure 10). For more information on ground bounce/V_{OLP} see the following section entitled Ground Bounce and Simultaneous Switching Transients.

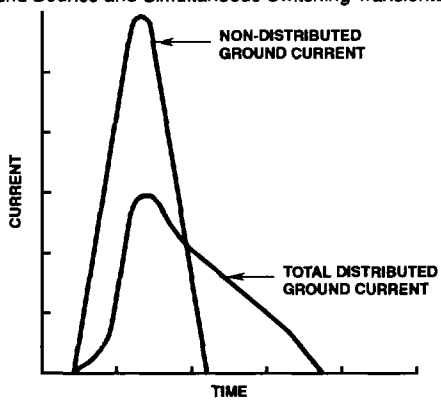


FIGURE 10A. NON-DISTRIBUTED vs TOTAL DISTRIBUTED

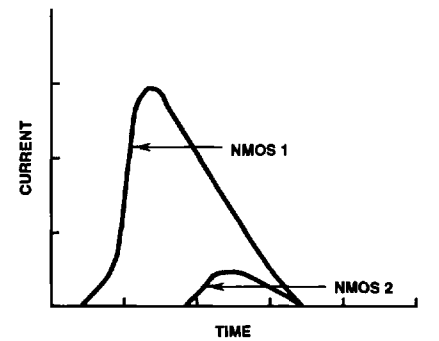


FIGURE 10B. COMPONENTS OF TOTAL DISTRIBUTED CURRENT

FIGURE 10. TRANSIENT SINK CURRENT

Ground Bounce and Simultaneous Switching Transients

Ground bounce and V_{CC} bounce are caused by the transient currents associated with switching capacitive loads. These transient currents cause voltage spikes across intrinsic inductances in the output source and sink paths of digital logic devices (See Figure 11).

Figure 12 shows the case of an FCT output switching from high to low. Transient current i flows through the total intrinsic inductance to system ground, causing a peak voltage differential (V_{LMAX}) between the on-chip ground and the system ground.

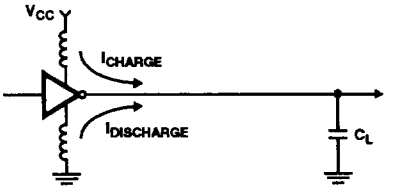


FIGURE 11. OUTPUT TRANSIENTS DUE TO LOAD CAPACITANCE

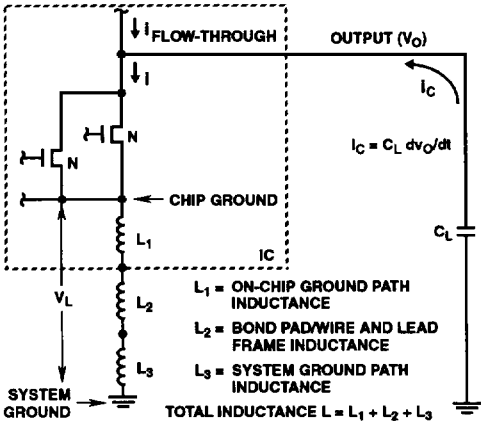


FIGURE 12. INDUCTANCES AND TRANSIENT CURRENTS RELATED TO GROUND BOUNCE

V_{LMAX} is seen as the positive peak value of the voltage waveform appearing across the inductance. This waveform (V_L) is shown in Figure 13 and is described by the following equation:

$$V_L = L\frac{di}{dt} \qquad \text{(EQ. 1)}$$

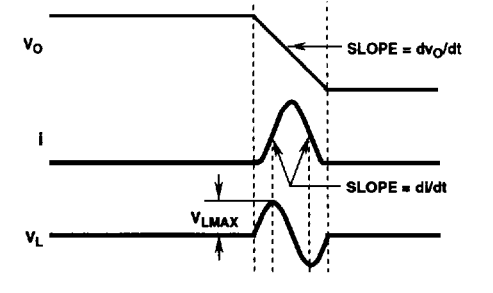


FIGURE 13. WAVEFORMS FOR CIRCUIT OF FIGURE 12

This internal ground bounce is coupled through the chip to the other outputs of the device, where the peak is measured as V_{OLP}. The magnitude of V_{OLP} for a given output depends on the magnitude of V_{LMAX} and the characteristics of the signal path for that particular output.

Since all of the device outputs have a common ground, the transient currents, and hence the likelihood of higher internal ground bounce, will increase with the number of outputs switching simultaneously. Also, there is mutual coupling among output signal paths which causes varying levels of V_{OLP} for a given output, depending on the particular combination of outputs that are switching simultaneously.

Worst case V_{OLP} for ICs with end pin V_{CC} and GND is measured at the output located farthest from the GND pin with all other outputs switching simultaneously from high to low. See Application Note AN9001, "Measurement of Ground and V_{CC} bounce in Advanced High Speed (AC/ACT/FCT) CMOS Logic ICs". See Section 8, "How to Use AnswerFAX" of this selection guide.

Reducing Ground Bounce

Taking another look at Equation 1 and noting that (i) itself is a function of dv_O/dt, it is seen that either a reduction in total inductance (L) or a reduction in the rate of change of the output edge (dv_O/dt) will result in decreased internal ground bounce. Harris has taken steps in both of these directions to reduce ground/V_{CC} bounce and simultaneous switching transients in FCT devices.

1. Layout techniques are used to reduce on-chip inductance in the V_{CC} and ground paths, especially for the segments that are common to all outputs. (See L1 in Figure 12).
2. Multiple bond-pads and bond-wires are used for V_{CC} and GND to reduce the inductance, in those paths, between the chip and the lead. (See L2 in Figure 12).
3. Lead frames are modified to create a ground plane. This also reduces L2.
4. By switching from 0V to 3.5V, Harris FCT outputs provide a reduction in dv_O/dt over parts that switch from 0V to 5V in the same amount of time.
5. Additionally, for high to low output transitions, the distributed pull-down structure lowers di/dt by reducing the peak amplitude and increasing the duration of the transient current waveform.

(For item 4 and item 5 above, see the output structure description under this heading).

V_{OLP} is further reduced in Harris FCT through the use of layout techniques that minimize the mutual coupling among outputs, and also between inputs and outputs.

Input Hysteresis

In addition to reducing ground bounce/V_{OLP}, Harris has increased the immunity of FCT to such transients, as well as any other ground noise, by adding hysteresis to the inputs. (See the input structure discussion earlier in this overview).

Latch-Up Sensitivity

Latch-up is an undesired state which occurs when a parasitic SCR, formed in ICs containing CMOS circuitry, is triggered. This parasitic SCR structure is shown in Figure 14. Triggering is caused by overvoltages or undervoltages (on input, output, or supply pins) which cause current to be injected into the substrate (i.e. to flow through substrate diodes). Once the device is triggered, a low impedance path is formed between V_{CC} and GND, thus allowing potentially destructive current (I_C) to flow through the chip.

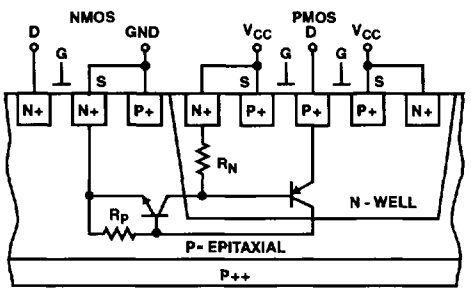


FIGURE 14A. CROSS SECTION OF CMOS STRUCTURE SHOWING SCR LATCH-UP PARASITIC TRANSISTOR

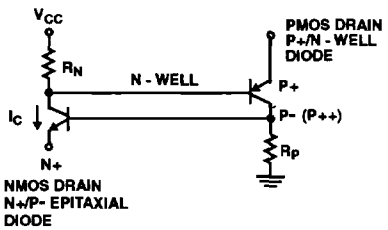


FIGURE 14B. SIMPLIFIED DIAGRAM

FIGURE 14.

The Harris FCT process employs a thin epitaxial layer of lightly doped P material. This allows for heavier doping of the P substrate, which lowers the resistance of the substrate. The resistance of the EPI layer is limited by its small thickness and through liberal use of contacts to GND. Similarly, the N-well resistance is limited by its dimensions and through the use of contacts to V_{CC}. Lowering the resistance of these regions increases the amount of current required to produce the biasing voltages needed to turn on the bipolar transistors, thereby significantly reducing the probability of triggering a parasitic SCR.

The use of the EPI layer, contacts, and other design and layout techniques result in resistance to latch-up for transient currents up to over 400mA, typical, at any input or output. The absolute maximum DC rating, as specified in the JEDEC Standard No. 18, is -20mA at the inputs and -50mA at the outputs.

DC Electrical Specifications

All DC and AC specifications of Harris FCT Bus-Interface ICs meet the industry standard JEDEC Standard No. 18 specifications.

Absolute Maximum Ratings

Note the conservative +6V absolute maximum DC supply voltage which, literally, means that Harris reliability data is based on long term operation at 6V and +125°C. For short term overvoltage and conducted transients, the supply voltage can increase to 10V or more. For the maximum rated DC input, output, V_{CC}, and ground currents shown, Harris design rules for internal chip metallization cross sections are such that there is no long term degradation of the Si-Al interconnect traces. Peak switching transient currents for V_{CC}, ground, and output traces may be higher (up to 1A) and are easily handled by the generous cross sectional area of the interconnect.

For free air power dissipation the thermal resistance of the plastic DIPs is 125°C/W, and for SOPs is 167°C/W.

Recommended Operating Conditions

All plastic packaged 74 series devices are reliably operated over the full temperature range of -55°C to +125°C. The recommended input slew rate of 10ns/V translates to the following maximum rise and fall times:

V_{IN} = 3V; t_R, $t_F \leq$ 24ns, 10% to 90%

V_{IN} = 5V; t_R, $t_F \leq$ 40ns, 10% to 90%

Please make note of the fact that switching speeds are specified and tested for input rise and fall times of 3ns.

For practical application purposes, the switching speeds and power dissipation prediction equations (shown later in this overview) are useful for up to 10ns input rise and fall times. There exists a range of capacitive loading (up through 150pF) for which FCT outputs will be within this range.

DC Electrical Specifications

The Harris FCT family DC ratings are shown in the DC Electrical Specifications table. Refer to Table 4 for the by-type output sink current (I_{OL}) and output source current (I_{OH}). Note that the critical I_{CC} quiescent current is 80µA at +70°C. The JEDEC limit, and competition's specification, is 1.5mA. Clearly, for battery power or battery back-up the Harris FCT is the preferred product.

Input Current vs Input Voltage

Figure 15 is the typical I_{IN} vs V_{IN} characteristic at T_A = +25°C for FCT devices. From V_{IN} = 0V to 10V the only current flowing is leakage current (typically 100nA). At about -0.8V the input diode to ground starts to conduct. This diode clamps the input voltage at approximately -1V. Under this condition input current should be limited to -20mA DC; 1A for peak transients of a few ns. Switching Current vs Input Voltage, Figure 16, shows the typical DC switching characteristics for an FCT input. Current (between V_{CC} and ground) begins to flow at approximately 0.7V and peaks at

about 1.4V. At the maximum current point the N and P transistors are both on and present the least resistance between V_{CC} and ground. Note that for a typical TTL V_{IL} of 0.25V to 0.4V, I_{CC} is below 1μA.

Sink Current Capability (I_{OL} vs V_{OL})

Figure 17 shows the typical output sink capability of an FCT 240 under various conditions from worst case, at V_{CC} = 4.5V and T_A = +125°C, to best case, at V_{CC} = 5.5V and T_A = -55°C. At V_{OL} = 0.55V, the output voltage at which 64mA is specified (at 5V, +25°C and 4.75V, +70°C) the curves indicate typical values of 120mA and 90mA, respectively. For V_{CC} = 4.5V and +125°C, and V_{OL} = 0.55V, the curve shows a typical value of 80mA which far exceeds the 48mA specified in the DC Electrical Specifications chart.

Source Current Capability (I_{OH} vs V_{OH})

Figure 18 shows the typical output source capability under the same conditions as in Figure 17. In these curves, at V_{OH} = 2.4V the typical currents at +25°C and +70°C are -69mA and -49mA, respectively; the minimum limit is -15mA. At +125°C and V_{OH} = 2.4V the curve shows -35mA; the minimum specified value is -12mA.

At the colder temperatures of 0°C and -55°C the current drive, both sink and source, is substantially higher.

The X-intercepts of Figure 18 show the FCT output voltage for CMOS input loads (defined as I_{IN} = 1μA, typically I_{IN} is a few nA). Table 5 summarizes V_{OH} for strictly CMOS loads. The data in this table is useful in FCT-to-CMOS (HC/HCT or AC/ACT) interface design, which is covered in AnswerFAX document number 7001, "System Design". See Section 8, "How to Use AnswerFAX".

TABLE 4. OUTPUT DRIVE CURRENT FOR 74FCT

DEVICE NUMBER	I_{OH} (mA)	I_{OL} (mA)
74FCT240	15	64
74FCT241	15	64
74FCT244	15	64
74FCT245	15	64
74FCT273	15	48
74FCT373	15	48
74FCT374	15	48
74FCT533	15	48
74FCT540	15	64
74FCT541	15	64
74FCT543	15	64
74FCT564	15	48
74FCT573	15	48
74FCT574	15	48
74FCT623	15	64
74FCT646	15	64
74FCT651	15	64
74FCT652	15	64
74FCT653	15	64
74FCT654	15	64
74FCT821A-824A	15	48
74FCT841A-844A	15	48
74FCT861A	15	48
74FCT863A	15	48
74FCT2952A	15	64
74FCT7623	15	64

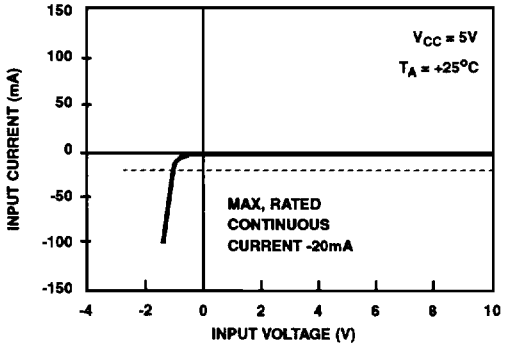


FIGURE 15. FCT INPUT CHARACTERISTIC

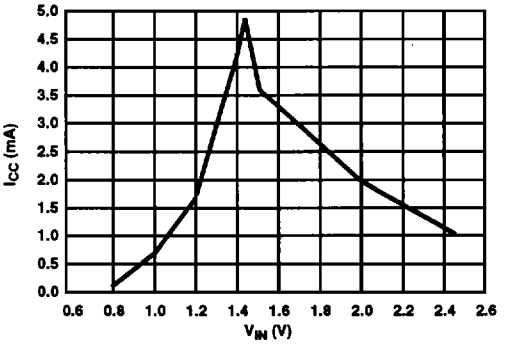


FIGURE 16. SUPPLY CURRENT vs INPUT VOLTAGE FOR FCT (TYPICAL)

Shown in Figure 19A is the FCT test circuit. A Thevenin equivalent may be used for output loading.

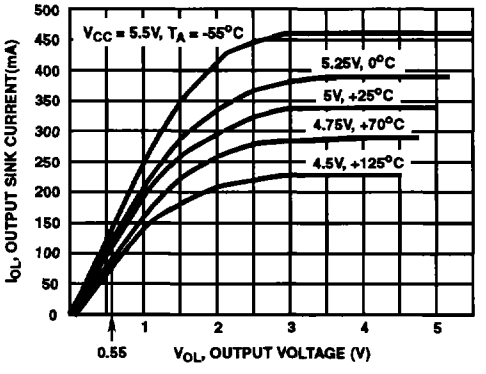


FIGURE 17. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE FOR FCT

TABLE 5. V_{OH} FOR CMOS LOADS; I_{OH} = 1μA

V_{CC} (V)	T_A (°C)	V_{OH} (V)
4.50	+125	3.5
4.75	+70	3.7
5.00	+25	4.0
5.25	0	4.2
5.50	-55	4.4

NOTE: See Figure 18.

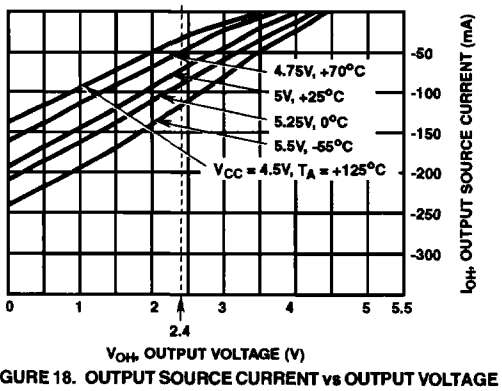


FIGURE 18. OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE FOR FCT

Dynamic Characteristics

Switching Speed

Since FCT is a low-power drop-in replacement for Fairchild Advanced Schottky TTL (FAST) 8-bit, 9-bit and 10-bit devices, the propagation delay specifications are set to equal those of the FAST family. As such, FCTXXX/A is generally the same speed as the Advanced CMOS Logic (AC/ACT) family, which should be considered a complementary, rather than competing, family. FCTXXXAT, however, is an average of 30% faster than either FAST or AC/ACT, thus creating a new speed standard that bipolar TTL cannot match. To keep switching noise under control and meet FCC emission specifications while using these extremely fast ICs, the system designer should employ transmission-line terminations, superior decoupling, and careful PC board layout.

The speed of an octal interface IC is usually characterized by the propagation delay on a single channel. For example, the CD74FCT240 Octal Inverting Buffer/Line Driver is specified for a maximum t_{PHL} and t_{PLH} of 8.0ns when operating in an ambient temperature (T_A) between 0°C and +70°C. It should be noted that all FCT specifications apply to both output signal transition directions: LH/HL, ZH/ZL, and LZ/HZ, whereas FAST frequently specifies widely different t_{PLH} and t_{PHL} values. Most designers will have to use the slower of the two values in their designs. Switching-speed parameters for FCT device types match those of JEDEC standard No. 18. Harris FCT ICs are offered for two temperature ranges: commercial 74 series (0°C to +70°C) and military/extended industrial 54 series (-55°C to +125°C) and are tested against the corresponding AC parameters. **Thus, while a 74 series part will operate over the full extended range, it is not guaranteed to meet 54 series AC parameter specifications over the full range.** Figure 19 depicts the JEDEC standard for the switching-speed test circuit and timing waveform definitions. These are the same that are used for FAST and AS; but differ slightly from those used to test AC/ACT.

FCTXXXAT - Higher Speed Version

Harris offers FCT products in two speed grades: Base speed and higher speed. The base speed version of each type is designated as either FCTXXX or FCTXXXA (the latter for 800 or 2900 series types). The higher speed versions are designated as FCTXXXAT when the base version is FCTXXX. The "T" serves to emphasize the fact that Harris FCT devices provide a TTL-like output swing, thereby reducing ground bounce. (The Harris base speed versions also offer this feature, but since those parts and numbers have already been established, they will not be changed.) Some examples:

BASE FCT PRODUCT	HIGHER SPEED PRODUCT
CD54/74FCT245E	CD54/74FCT245ATE
CD54/74FCT245M	CD54/74FCT245ATM

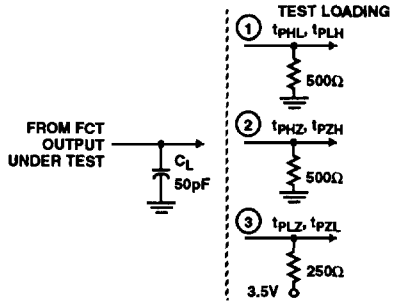
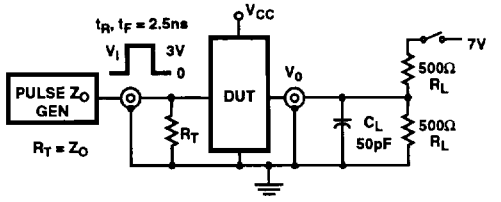


FIGURE 20. HARRIS (AND JEDEC) FCT TEST LOAD CIRCUITS

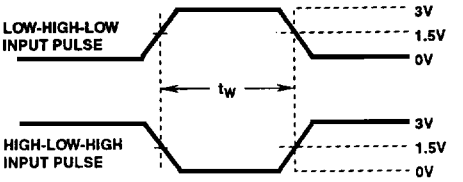


TEST	SWITCH POSITION
t_{PLZ} t_{PZL} Open Drain	Closed
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	Open

NOTES:

1. C_L = Load capacitance includes jig and probe capacitance.
2. R_T = Termination should be equal to Z_{OUT} of the pulse generator. (Typ. 50Ω).
3. V_{IN} = 0V to 3V.
4. Input: $t_R = t_F$ = 2.5ns (10% to 90%), unless otherwise specified.

FIGURE 19A. TEST CIRCUIT



OUTPUT REQUIREMENTS

1. Device must follow truth table.
   $V_{OL} \leq 0.55V$
   $V_{OH} \geq 2.4V$
2. Input Conditions:
   $t_R = t_F \leq 2.5ns$ (as fast as required)
3. Standard Output Loading:
   $R_L = 500\Omega$
   $C_L = 50pF$

FIGURE 19B. INPUT PULSE WIDTH

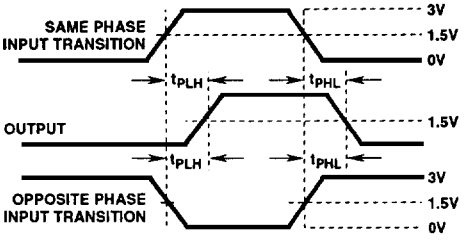


FIGURE 19C. PROPAGATION DELAY TIMES

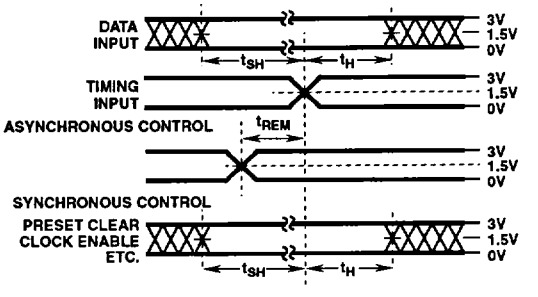


FIGURE 19D. SETUP, HOLD AND REMOVAL TIMES

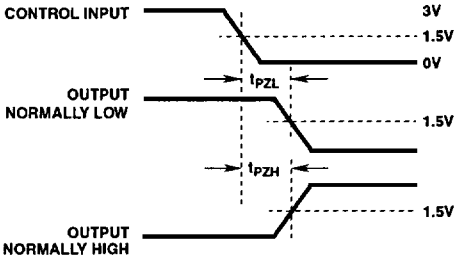


FIGURE 19E. OUTPUT ENABLE TIMES

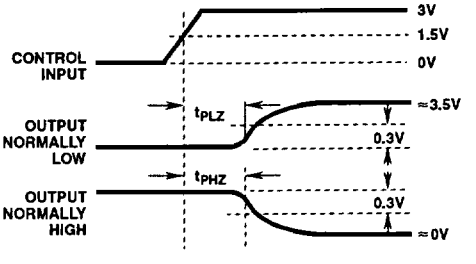


FIGURE 19F. OUTPUT DISABLE TIMES

FIGURE 19. TEST CIRCUIT AND TIMING DEFINITIONS FOR FCT

Harris FCTXXXAT high speed versions are, on the average, 30% faster than either FCT or FAST. Speeds are also faster than the AS, BCT, or BC bus interface families.

Speed vs Capacitive Load

Propagation delays for FCT interface types are determined using a JEDEC standard load as shown in Figure 20. The 50pF capacitor approximates a fan-out of 5-10 CMOS/TTL loads, which is reasonable for on-board operation, but probably too low for bus-interface applications. Figure 21 illustrates the effect of different capacitive loads on propagation delays. Above C_L = 50pF the delta delay is about 16ps/pF.

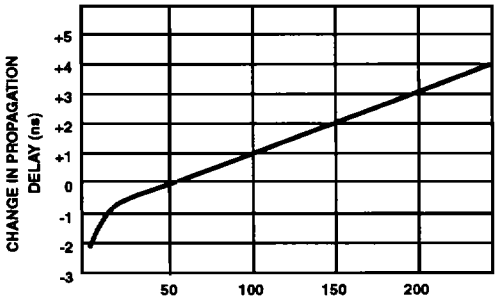


FIGURE 21. CHANGE IN PROPAGATION DELAY AS A FUNCTION OF LOAD CAPACITANCE FOR FCT

Propagation Delay vs Temperature and V_{CC}

The active delay and the delays caused by enabling and disabling outputs are plotted in Figure 22. Parameters t_{PLH}, t_{PHL}, t_{PLZ}, t_{PZL}, t_{PHZ}, t_{PZH} are shown as they vary over the temperature range of -55°C through +125°C and over the V_{CC} range of 4.50V to 5.50V. Mean data is for the FCT244 non-inverting buffer function.

Min/Max Delay Issue and Solution

Figure 23 vividly illustrates the wide Min/Max delay spread of FCT data sheet (D/S) specifications. It is readily seen that for the 74FCT373 part the design engineer would unhappily use a Min delay of 1.5ns and a Max delay of 8.0ns. This infers that for any two 373 octal latches making up a 16-bit-wide bus-interface, 8 bits could traverse the IC at 1.5ns while the other 8 bits take 8.0ns! This is a significant spread and can limit useful system clock frequency.

However, by making two simple adjustments to the Min/Max delays, a tighter set of useful design Min/Max delays are obtained:

1. Adjust ±0.5ns for built-in guardbands - used for test correlation of ICs, not design use.
2. Adjust for temperatures greater than 0°C and less than +70°C.

Rules for Useful Design Min/Max

1. t_P Min = D/S Min + 0.5ns + 0.01ns/°C
2. t_P Max = D/S Max - 0.5ns - 0.01ns/°C

These rules are applicable to t_{PLH}, t_{PHL}, t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}. In Figure 23A, the D/S and design values are shown; certainly a Min/Max range of 2.4ns to 7.4ns for a PCB operating at +50°C ±10°C is more useful than 1.5ns to 8.0ns.

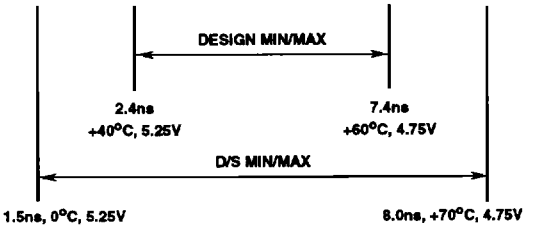


FIGURE 23A. FCT373

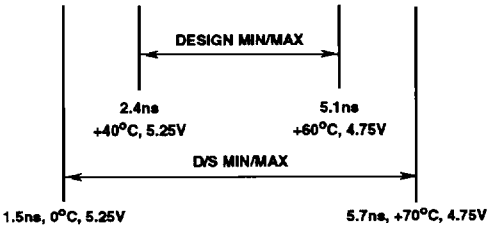


FIGURE 23B. FCT373AT

FIGURE 23. EXAMPLE SHOWING DESIGN VALUES vs DATA SHEET VALUES FOR MIN/MAX DELAYS

Even more beneficial is application of the higher speed suffix "AT" FCT parts. As shown in Figure 23B, the design Min/Max spread is only 2.4ns to 5.1ns; this is very useful! The two design rules for Min/Max are applicable to all Harris FCT types.

Delay Skew

Each 8-bit, 9-bit and 10-bit part will have propagation delay skews that fall into three categories:

- Pin to pin skew
- Simultaneous switching skew
- H-L vs L-H (edge) skew

Table 6 records the skew data for the three categories. Simultaneous switching skew is measured with 7/8 outputs switching rather than 8/8 due to the immediate availability of a good RF ground bounce fixture. Skew would be slightly larger for 8/8 switching. The largest incremental delay change occurs for 7/8 outputs switching H-L. The incremental change for the H-L skew is larger than that for the L-H skew due to output edge control circuitry.

Dynamics of Ground Bounce

Octal or 9/10-Bit bus-interface parts, when switching simultaneously, will have worst-case noise glitches on otherwise quiet outputs when N-1 of the N outputs all go HIGH or LOW at the same instant. In a practical sense, skew of the IC channels (up to 1ns) and skew of PCB interconnection (possibly 0.5ns to 1ns) will cause outputs to switch at slightly different times; therefore, this is a "Murphy's Law" exercise - what if all 7 outputs of an FCT octal (such as the popular 245

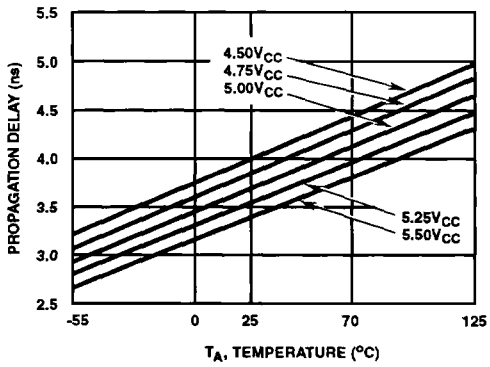


FIGURE 22A. t_{PLH}

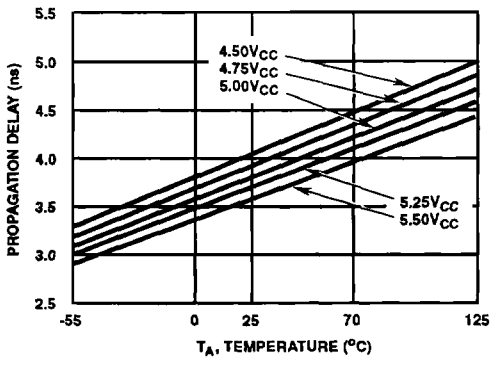


FIGURE 22B. t_{PHL}

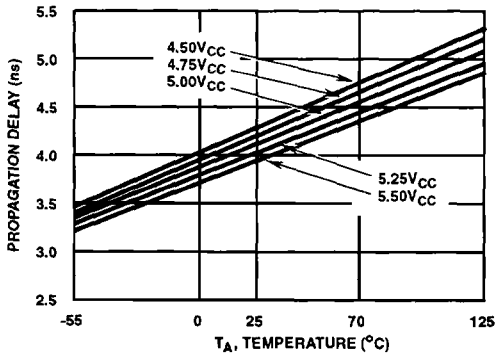


FIGURE 22C. t_{PLZ}

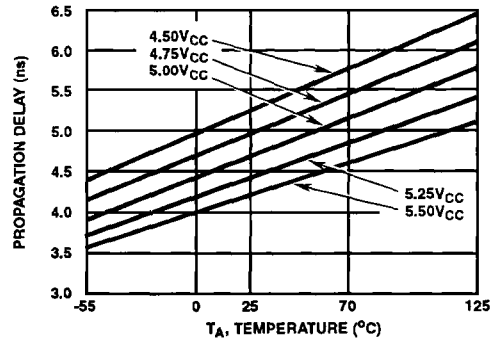


FIGURE 22D. t_{PZL}

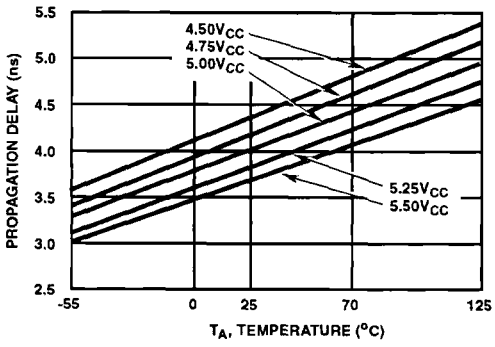


FIGURE 22E. t_{PHZ}

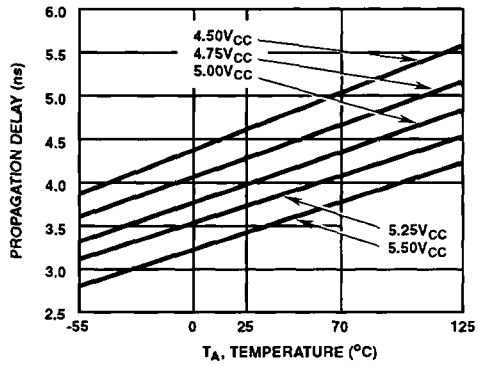


FIGURE 22F. t_{PZH}

FIGURE 22. MEAN PROPAGATION DELAY vs TEMPERATURE AND SUPPLY VOLTAGE FOR FCT

transceiver or the 373 latch) all switch H-L or L-H on top of each other? Figure 24A and Figure 24B show the ground bounce (V_{OLP}) noise glitch for Harris FCT245 and 373 types and Figure 24C shows the V_{CC} bounce (V_{OHV}) glitch for the FCT373 type - all very representative of the Harris IC and package design for minimized switching noise. In fact, the FCT373 devices used for these measurements operate at "AT" speed. Figure 25 shows the measured ground bounce of a competitor's FCT 245 IC. Ground bounce measurements for the competitor's FCT 245A are even higher. Application Note AN9001 provides a detailed description of Harris accurate Ground/V_{CC} Bounce Test PCBs and how readers may obtain one for their own measurements. From the waveforms in Figure 24 and Figure 25, a summary of useful observations is shown in Table 7.

TABLE 6. TYPICAL PROPAGATION DELAY SKEW FOR THE FCT245

OUTPUT		PROPAGATION DELAY (ns)					
		1/8 SWITCHING		7/8 SWITCHING		INCREMENT 1/8 TO 7/8	
PIN #	NAME	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}
11	B7	5.19	5.09	6.32	5.68	1.13	0.59
12	B6	5.06	4.76	6.40	5.64	1.34	0.88
13	B5	5.14	4.75	6.40	5.60	1.26	0.85
14	B4	4.93	4.82	6.40	5.56	1.47	0.74
15	B3	5.12	4.78	6.40	5.56	1.28	0.78
16	B2	5.30	4.86	6.40	5.24	1.10	0.38
17	B1	5.22	4.86	6.40	5.24	1.18	0.38
18	B0	5.25	4.84	Quiet	Quiet	-	-
Pin to Pin Skew		0.37	0.34	0.08	0.44	-	-
Maximum Edge Skew		0.44		1.16		-	-
Maximum 1/8 to 7/8 Skew		-	-	-	-	1.47	

NOTE: V_{CC} = 5V, T_A = +25°C.

TABLE 7. SELECTED DATA FROM FIGURE 24 AND FIGURE 25

DEVICE TYPE	V_{OLP} (V)	UNDER SHOOT (V)	PULSE WIDTH AT 0.8V (ns)	V_{OHV} (V)
Harris FCT245/AT	1.24	0.83	3.0	-
Harris FCT373/AT	1.24	0.9	3.5	0.46
Competitive FCT245	2.00	0.85	3.0	-
Second Peak	1.1	-	3.0	-

NOTES:

1. V_{OLP} exceeds D/S V_{IL} of 0.8V in all cases. Even the second peak of the competitive 245 ground bounce ringing waveform exceeds this limit.
2. Widths are under 3.5ns at 0.8V. This means that a wait time to strobe an output would be no longer than about 4ns after outputs switch H-L.
3. The one-of-seven switching outputs that is monitored for the Harris FCT device shows minimal undershoot and overshoot - illustrating benefits of designed-in ground/V_{CC} bounce minimization techniques. However, competitive H-L active output undershoots by 1.5V and falls faster - illustrating the lack of a slowing H-L edge control.

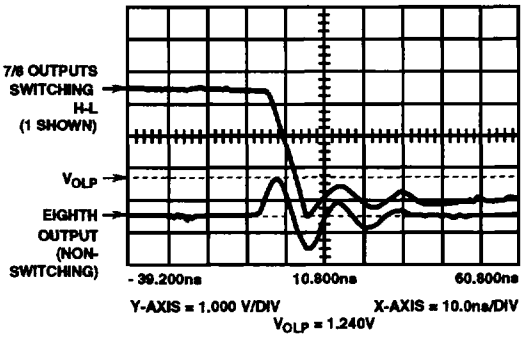


FIGURE 24A. HARRIS 245 - V_{OLP}

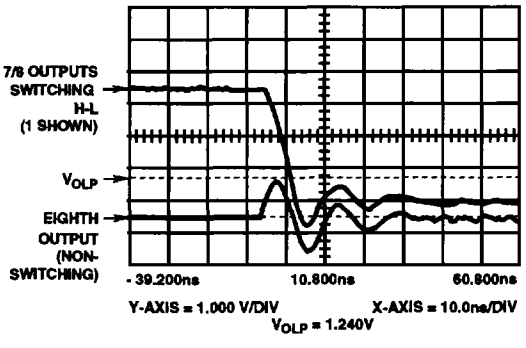


FIGURE 24B. HARRIS 373 - V_{OLP}

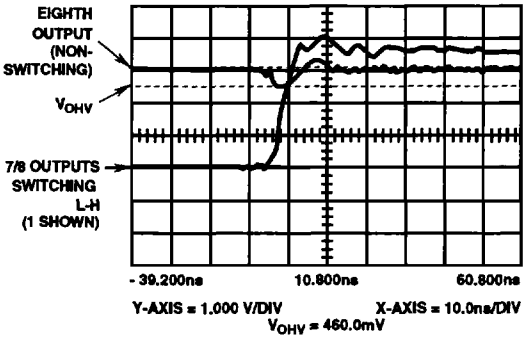


FIGURE 24C. HARRIS 373 - V_{OHV}

FIGURE 24. GROUND BOUNCE (V_{OLP}) AND V_{CC} BOUNCE (V_{OHV}) FOR HARRIS FCT

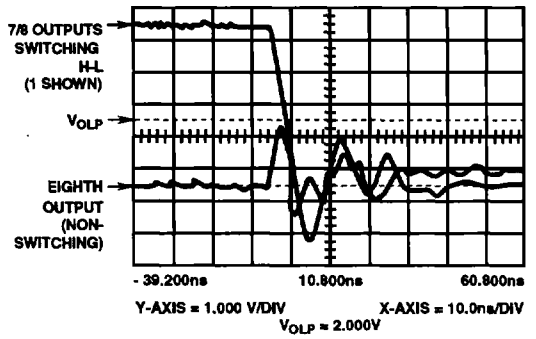


FIGURE 25. GROUND BOUNCE (V_{OLP}) FOR A COMPETITOR'S FCT

System Design Aspects of V_{OLP} and V_{OHV}

Although Harris FCT outputs might produce a peak ground bounce glitch of 1.25V, Harris FCT inputs will not respond. A built-in hysteresis circuit at each input adds about 0.2V to the input switchpoint voltage.

Power Consumption

Operating Current/Power

For Bus-Interface Logic ICs that are specified to match VME, Multibus II or other bus standards, FCT is clearly the lowest current drain family, and hence lowest heat dissipation family. Figure 26 is actual measured current up through 20MHz operation for 7/8 outputs switching into a 50pF load. Since V_{IH} is 3.5V, the I_{CC} component of FCT current drain is included; Figure 26 is a very real-world comparison of bipolar FAST, BiCMOS BCT, and Harris BiCMOS FCT. Results are very obvious for relative current drain; for example at standby (f = 0) FCT current drain is virtually zero while BCT and FAST are at 50mA and 75mA respectively. For a continuous clock, up through 20MHz, both FCT and BCT save power over FAST. Most importantly, for overall average current drain of data or address buffers, at 5MHz, FCT shows over a 2.5X savings in current, and a corresponding savings in power (or heat dissipation) in a system.

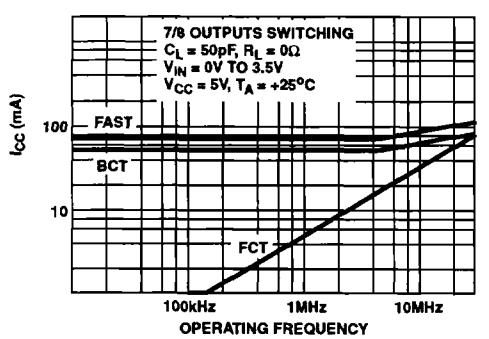


FIGURE 26. OPERATING CURRENT (I_{CC}) AS A FUNCTION OF OPERATING FREQUENCY FOR FAST, BCT, AND HARRIS FCT

Even for the Hi-Z mode, when outputs hanging on a bus are disabled, FCT saves 188X in standby or Hi-Z IC power consumption.

TABLE 8. FCT vs BCT POWER DISSIPATION COMPARISON

	I_{CC} MAXIMUM	POWER MAXIMUM
FCT	0.08mA	0.44mW
BCT	15mA	82.5mW

NOTE: V_{CC} = 5.5V, T_A = +70°C, Outputs Hi-Z, Data Sheet Values.

Power Estimating

The system designer needs to get a good handle on his PCB power consumption in order to specify his power supply, design for thermal control, and also to estimate decoupling capacitor sizes and ferrite bead currents for EMI control. Equation 2 shows the exact FCT power consumption equation per IC input or per IC function. Without going through the data sheets to extract parameters to put into this equation let's look at a concise set of values applicable to all Harris FCT types:

TABLE 9. PARAMETERS FOR CALCULATING POWER CONSUMPTION

PARAMETERS	TYPICAL V_{CC} = 5V T_A = +25°C	MAXIMUM V_{CC} = 5.5V T_A = +70°C	MAXIMUM V_{CC} = 5.5V T_A = +125°C
I_{CC}	0	80µA	500µA
ΔI_{CC}	0.4mA	1.6mA	2mA
C_{PD} (Note 1)	40pF	60pF	60pF

NOTE: 1. Will vary somewhat with device type.

All other variables such as C_L per output, and input/output frequencies are estimates made by the system designer, remembering that average frequency (not peak) is used for power averaging.

$$P = \underbrace{I_{CC} V_{CC} + \Delta I_{CC} V_{CC} D + C_{PD} V_{CC}^2 f_i}_{\text{Per Input/Function}} + \underbrace{C_L (V_{CC} - 1.4V)^2 f_O}_{\text{Per Output/Function}} \quad \text{(EQ. 2)}$$

Where:

I_{CC} = Quiescent Current (From Data Sheet Ratings)

V_{CC} = Supply Voltage

f_i = Input Frequency

f_O = Output Frequency

C_{PD} = Device Equivalent Power Dissipation Capacitance; Used for Computing Internal Chip Power ≈ 40pF

C_L = Load Capacitance; Used for Computing Output Stage Power

ΔI_{CC} = Added Direct Current When $V_{IN} = V_{CC}$ -2.1V (TTL Input High Level)

D = Duty Cycle of Input (Percent of Time High)

System Design Considerations

System Design Using Harris FCT

Successful system design using Harris FCT is assured if the fundamental DC drive and major speed considerations already covered are understood - and if "Golden Rules" of Design and PCB layout are followed. It is not enough simply to apply the static and dynamic characteristics in order to achieve excellent fault-free computer system operation, the system design engineer must also approach his hardware design task so as to stay within stringent EMI limits for conducted and radiated energy.

Ten Golden Rules for Successful Design with FCT

1. No Floating Inputs - Tie unused inputs to GND or V_{CC}. For transceiver I/O pins, return floating inputs to V_{CC} or ground via a resistor (100Ω or more) to avoid output shorts.
2. Decouple Each IC Correctly - Decoupling differs for data (non-periodic) signal ICs and clock (or periodic signal) ICs.
   A. Data/Address (non-periodic) - Place a decoupling capacitor with value C_D on same side of PCB as IC with shortest possible leads to V_{CC} and ground pins. Given a choice, put C_D closer to V_{CC} pin to minimize EMI on power buses. Placing C_D on the opposite side of the board is not as effective.

$$C_D = 9NC_{PD} + 9\sum_{1}^{N} C_L \qquad \text{EQ. 3}$$

   N = Number of Functions in IC

   Also specify C_D to have:

   ESL < 10nH

   ESR < 0.5Ω

   B. Clock Generator and Driver ICs (Periodic Signals) - 20MHz to 40MHz periodic clocks, strobes, etc. have harmonics in the EMI band (150MHz and up) where FCC rules are stringent. Decouple periodic signal ICs with both a C_D and ferrite bead. Combination three terminal devices for this purpose are available (the Murata Erie DS 310 types, for example). Place on same side of PCB as IC.
3. Terminate Interconnects More than Six Inches in Length - VME, Multibus II, and other bus standards specify adequate Thevenin termination. Interconnects within a PCB may not need to be terminated but should be if they are six inches or more in length. This avoids reflection problems and also avoids crosstalk problems should two parallel PCB traces run alongside each other for six inches or more. A termination also keeps ground bounce noise glitches from increasing in amplitude much over 1.25V, thereby preventing these glitches from false triggering inputs.
   Terminations may be series, shunt, or Thevenin.
4. Low-Voltage Operation - While Harris FCT may be operated below 4.5V, it was not designed for this purpose. Harris AC logic, operable down to V_{CC} = 1.5V is recommended for battery operation or battery backup. (References 5 and 6).

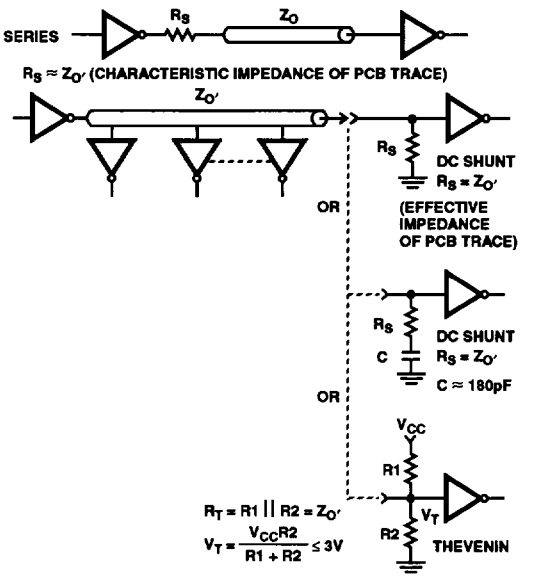


FIGURE 27. METHODS OF TERMINATION

5. Live PCB Insertion and Multi-System Interfacing is Safe With Harris FCT - Because Harris FCT (unlike other FCT) does not have input or output clamp diodes to V_{CC} there is no danger in live insertion of PCB with Harris FCT as buffers. With other buffers, live bus clocks or data can momentarily be loaded down causing loss of information. This problem will not occur with Harris FCT. Also interfacing between two systems having different power sources is facilitated.
6. Momentarily Shorting Outputs is Allowed But Restricted - If forced node testing is done, please be careful not to overheat the FCT IC (short only one output pin per package, for no more than 1s).
7. Interfacing FCT to Other Logic Families - Harris FCT Bus-Interface ICs interface easily to all other CMOS, Bipolar, and BiCMOS logic families directly as shown in Table 10. Note 1 applies to the interface between FCT devices and those that have CMOS switching levels (HC or AC); the only limitation is a reduced noise margin from what it would be if FCT had a full 5V swing. Harris FCT is intentionally designed to provide a reduced output swing. The user should understand that not swinging to 5V has overwhelming advantages, namely:
   A. Less crosstalk jeopardy
   B. Less switching noise, i.e. lower ground/V_{CC} bounce
   C. Less radiated and conducted EMI

TABLE 10. INTERFACING FCT AND OTHER LOGIC FAMILIES

FROM	TO				
	FCT	HCT/ ACT	HC/AC	FAST AS ALS/LS	BC/FCT
FCT	Direct	Direct	Direct (Note 1)	Direct	Direct
AC/ACT	Direct	Direct	Direct	Direct	Direct
HC/HCT	Direct	Direct	Direct	Direct	Direct
FAST AS/ALS/LS	Direct	Direct	(Note 2)	Direct	Direct
BC/BCT	Direct	Direct	(Note 2)	Direct	Direct

NOTES:

1. For Harris FCT to HC or AC logic families, the low logic level noise margin is 1.4V (V_{OL} < 0.1V and V_{IL}Max = 1.5V). The high logic level noise margin is as shown in Table 11.
2. For any of the TTL families (FAST, AS, ALS, LS) or the BC, BCT BiCMOS families, for low logic levels (V_{OL} to V_{IL}) there is a good noise margin of at least 1.2V. For high logic levels (V_{OH} to V_{IH}) the noise margin varies with family. If the manufacturer does not supply data like that shown in Table 11 for Harris FCT, then a pull-up resistor to V_{CC} at the interface is necessary.

8. Avoid Crosstalk Problems - As shown in Figure 28, if two PCB interconnect copper traces on the same layer run closely spaced in parallel for enough distance (L) without terminations, a noise glitch at B can be large enough to switch that input. Rules to avoid problematic crosstalk:
   A. For FCT keep L conservatively under six inches if runs have to be paralleled.
   B. If parallel runs exceed six inches, terminate with $R_S = Z_0$ of trace. Place a C of about 180pF in series with R_S to reduce power. Also a ground trace could be placed between runs.
   C. Best bet is to avoid parallel runs of over six inches. Use different PCB levels separated by a V_{CC} or ground plane.

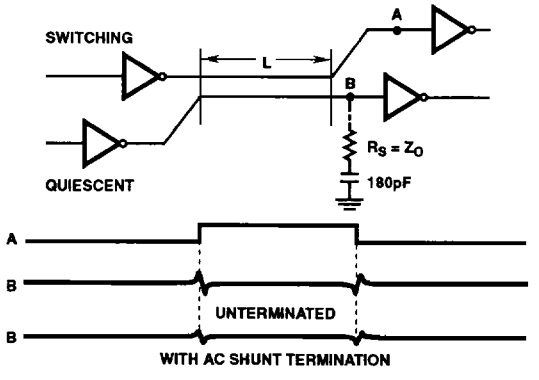
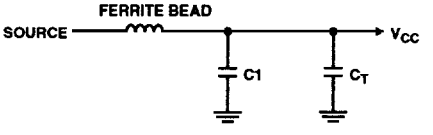


FIGURE 28. SIGNAL CROSSTALK RESULTS FROM PARALLEL TRACES AND IS REDUCED BY TERMINATION

9. Ground/V_{CC} Bounce Will Not Affect Performance with These Simple Rules:
   A. V_{CC} bounce is under 0.5V; usually not a problem.
   B. Ground bounce is about 1.25V, about half of that of competitive FCT, but above V_{IL}Max of 0.8V. Even though Harris FCT ground bounce is well below the input switchpoint, particularly with sufficient pulse width to false trigger an input, other system noise and/or DC offset of 0.2V to 0.3V above ground due to high DC loading could false trigger an input if the line is not terminated. Therefore, if an output with a potential for ground bounce exists, terminate with either series or shunt R_S as described in Rule 3 above. Remember, an unterminated line produces a signal of 2X amplitude at the end of the unterminated trace. This could easily cause false triggering. If ground bounce occurs at latch or flip-flop data inputs, its 3ns width at 0.8V and its centering right at the output edge (See Figure 24) is such that no extra strobe delay or system clock frequency reduction is needed.

   Because FCT inputs have typically 200mV of hysteresis, input dynamic noise margin remains above 0.5V in the presence of ground bouncing, i.e. internal stored data is not subject to loss for Harris FCT; this is a problem in competitive FCT which has 2V or more of ground bounce!

10. PCB Must Be Designed to Minimize EMI - Before initiation of the PCB layout and design, it is imperative that a comprehensive action plan to minimize EMI be put into place - realizing that high speed digital ICs are EMI spectrum generators. Whether it is FCT, AC/ACT, FAST, VLSI, ASICs or memory, with clock rates above 10MHz and switching edges below 5ns, PCB design for EMI containment will pay off in the end - designers will not have to apply painful "band-aids", or worse - scrap the PCB design, after equipment is built. Guidelines for EMI control in PCB application of FCT or like devices follow:
    A. Become familiar with EMI control measures - There are good comprehensive text books and reports available on PCB design spanning layout, decoupling, board materials, terminations, shielding, grounding, etc. Some of these are listed as references at the end of this section. Tutorial seminars are available from sources such as The Keenan Corporation listed as a reference. Absolute musts are summarized in the following notes.
    B. Decouple carefully.
       1. ICs as described in Rule 2 above.
       2. PCB power entry - each power plane area on PCB



C1 = 0.1μF RF CAPACITOR
C_{TMIN} = TANTALUM CAPACITOR EQUAL TO SUM OF ALL DECOUPLING CAPACITORS ON BOARD

FIGURE 29. DECOUPLING CAPACITORS AT POWER ENTRY POINT ON PC BOARD

TABLE 11. NOISE MARGINS FOR INTERFACING HARRIS FCT TO AC OR HC LOGIC

	FCT OUTPUT VOLTAGE			AC OR HC INPUT VOLTAGE		NOISE MARGIN	
LOW LOGIC LEVEL	V_{OL} < 0.1V			V_{IL} = 1.5V MAXIMUM		1.4V	
HIGH LOGIC LEVEL	V_{OH} (V)			V_{IH} (V)		NOISE MARGIN (V)	
	V_{CC} (V)	T_A (°C)	V_{OH} (V)	MINIMUM SPECIFIED	ACTUAL SWITCHING VOLTAGE	MINIMUM	ACTUAL
	4.50	+125	3.5	3.15	1.90 to 2.60	0.35	0.90
	4.75	+70	3.7	3.33	2.03 to 2.73	0.37	0.97
	5.00	+25	4.0	3.50	2.15 to 2.85	0.50	1.15
	5.25	0	4.2	3.68	2.28 to 2.98	0.52	1.22
	5.50	-55	4.4	3.85	2.40 to 3.10	0.55	1.30

C. Isolate IC block with separated power planes - On a multi-layer PCB (preferred over two-sided) use a separated V_{CC} plane for various system blocks such as high speed synchronous logic, I/O logic, memory, lower-speed logic, analog circuits. For each segmented V_{CC} area use separate power entry decoupling as illustrated in Figure 29.

D. Periodic Signal Buffers, Main Culprit - As discussed, take special care in decoupling, terminating, grouping, and laying out short ground return paths. It has been found[1-4] that most out-of-specification EMI frequency peaks are harmonics of periodic signals, and can be traced back to a violation of the "Golden Rules" covering periodic signals in the design of PCBs.

E. IC Placement - FCT as PCB I/O should be very close to the connector with its isolated V_{CC} plane. This minimizes the inductance of high current V_{CC} and ground paths. Group synchronous clocked logic and micros closely, again with a dedicated V_{CC} plane in an area close to PCB connector - but secondary to I/O. Slower speed and/or asynchronous logic should be grouped in a separate area with its own V_{CC} plane, and can be farther from connector. Likewise analog signal ICs must have separate V_{CC} and ground planes providing separate power entry.

F. Terminate - Terminations always reduce ringing on a PCB interconnect at FCT-like speed. Follow guidance of Rule 3 above.

References

[1] Harris Semiconductor, Application Note AN8906, "Noise Aspects of Applying Advanced CMOS (AC/ACT) Semiconductors," April 1989.

[2] R. Kenneth Keenan, "Decoupling and Layout of Digital Printed Circuits," The Keenan Corporation, Pinellas Park, FL.

[3] R. Kenneth Keenan, "Digital Design for Interference Specifications," The Keenan Corporation, Pinellas Park, FL.

[4] The Keenan Corporation, FCC Emissions and Power Bus Noise - 2nd Edition.

[5] Harris Semiconductor, Data Book SSD-283A, Advanced CMOS Logic ICs, October 1988.

[6] Nadolski, J. "Logic Designs for Battery-Powered or Battery Backed-Up Operation," Harris Semiconductor Application Note AN7373.

[7] JEDEC Standard No. 20, "Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High Speed CMOS Devices".

[8] JEDEC Standard No. 18, "Standard for Description of 54/74FCTXXXX High Speed CMOS[/BiCMOS] Devices".