



# 9Mb QDR™ SRAM

## 4-WORD BURST

MT54V512H18E

### Features

- 9Mb Density (512K x 18)
- Separate independent read and write data ports with concurrent transactions
- 100 percent bus utilization DDR READ and WRITE operation
- High-frequency operation with future migration to higher clock frequencies
- Fast clock to valid data times
- Full data coherency, providing most current data
- Four-tick burst counter for reduced address frequency
- Double data rate operation on read and write ports
- Two input clocks (K and K#) for precise DDR timing at clock rising edges only
- Two output clocks (C and C#) for precise flight time and clock skew matching—clock and data delivered together to receiving device
- Single address bus
- Simple control logic for easy depth expansion
- Internally self-timed, registered writes
- +2.5V core and HSTL I/O
- Clock-stop capability
- 13mm x 15mm, 1mm pitch, 11 x 15 grid FBGA package
- User-programmable impedance outputs
- JTAG boundary scan

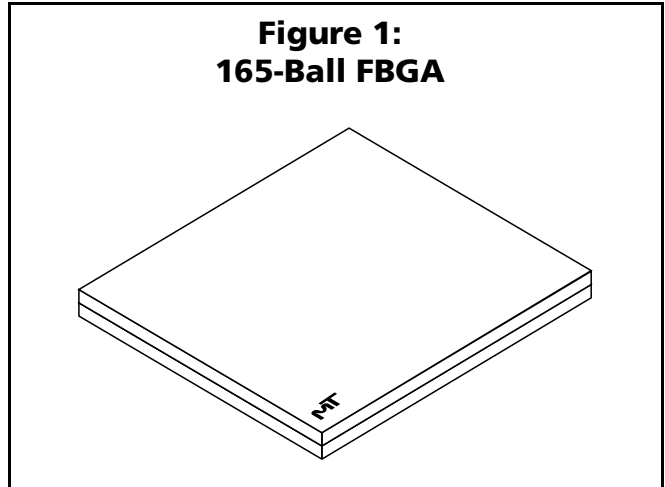
### OPTIONS

- |                            | <b>MARKING<sup>1</sup></b> |
|----------------------------|----------------------------|
| • Clock Cycle Timing       |                            |
| 6ns (167 MHz)              | -6                         |
| 7.5ns (133 MHz)            | -7.5                       |
| 10nx (100 MHz)             | -10                        |
| • Configurations           |                            |
| 512K x 18                  | MT54V512H18E               |
| • Package                  |                            |
| 165-ball, 13mm x 15mm FBGA | F                          |

### NOTE:

1. A Part Marking Guide for FBGA devices can be found on Micron's Web site—<http://www.micron.com/numberguide>

**Figure 1:**  
**165-Ball FBGA**



**Table 1: Valid Part Numbers**

PART NUMBER	DESCRIPTION
MT54V512H18EF-xx	512K x 18, QDRb4 FBGA

### General Description

The Micron<sup>®</sup> QDR<sup>®</sup> (Quad Data Rate™) Synchronous Pipelined Burst SRAM employs high-speed, low-power CMOS designs using an advanced 6T CMOS process.

The QDR architecture consists of two separate DDR (double data rate) ports to access the memory array. The read port has dedicated data outputs to support READ operations. The write port has dedicated data inputs to support WRITE operations. This architecture eliminates the need for high-speed bus turnaround. Access to each port is accomplished using a common address bus. Addresses for reads and writes are latched on alternate rising edges of the K input clock. Each address location is associated with four 18-bit words that burst sequentially into or out of the device. Since data can be transferred into and out of the device on every rising edge of both clocks (K, K#, C and C#) memory bandwidth is maximized while simplifying system design by eliminating bus turnarounds.



Depth expansion is accomplished with port selects for each port (read R#, write W#) which are received at K rising edge. Port selects permit independent port operation. All synchronous inputs pass through registers controlled by the K or K# input clock rising edges. Active LOW byte writes (BW0#, BW1#) permit byte write selection. Write data and byte writes are registered on the rising edges of both K and K#. The addressing within each burst of four is fixed and sequential. All synchronous data outputs pass through output registers controlled by the rising edges of the output clocks (C and C# if provided, otherwise K and K#).

Four balls are used to implement JTAG test capabilities: test mode select (TMS), test data-in (TDI), test clock (TCK), and test data-out (TDO). JTAG circuitry is used to serially shift data to and from the SRAM. JTAG inputs use JEDEC-standard 2.5V I/O levels to shift data during this testing mode of operation.

The SRAM operates from a +2.5V power supply, and all inputs and outputs are HSTL-compatible. The device is ideally suited for applications that benefit from a high-speed fully-utilized DDR data bus.

Please refer to Micron's Web site ([www.micron.com/sramds](http://www.micron.com/sramds)) for the latest data sheet.

## READ/WRITE Operations

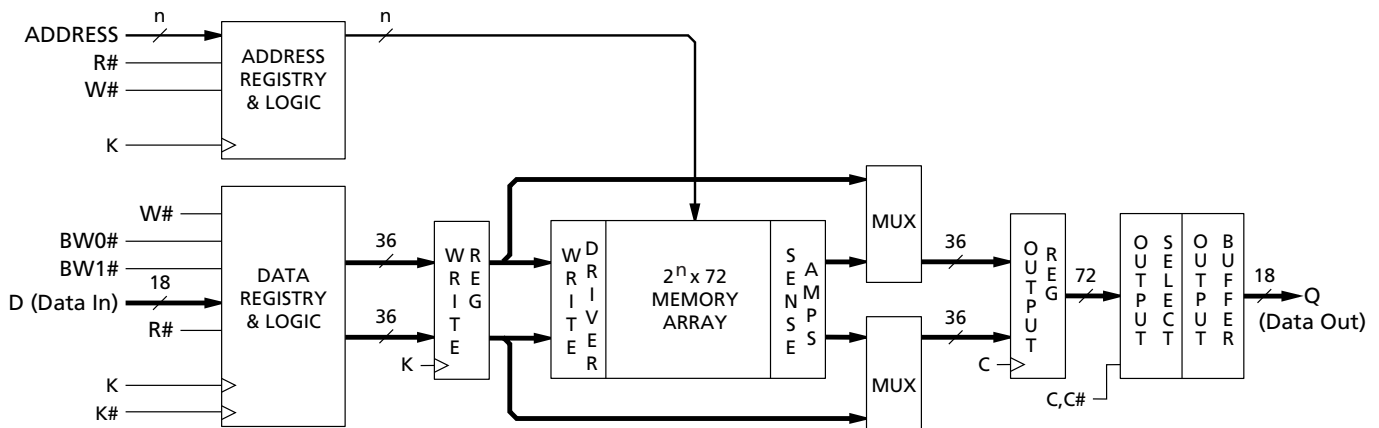
All bus transactions operate on an uninterruptable burst of four data, requiring two full clock cycles of bus utilization. Any request that attempts to interrupt a

burst in progress is ignored. The resulting benefit is that the address rate is kept down to the clock frequency even when both buses are 100 percent utilized.

READ cycles are pipelined. The request is initiated by asserting R# LOW at K rising edge. Data is delivered after the next rising edge of K using C and C# as the output timing references, or using K and K#, if C and C# are tied HIGH. If C and C# are tied HIGH, they may not be toggled during device operation. Output tri-stating is automatically controlled such that the bus is released if no data is being delivered. This permits banked SRAM systems with no complex OE timing generation. Back-to-back READ cycles are initiated every second K rising edge. Any command in between is ignored, since the burst sequence may not be interrupted and requires two full clock cycles.

WRITE cycles are initiated by W# LOW at K rising edge. Data is expected at both rising edges of K and K# beginning one clock period later. Write registers are incorporated to facilitate pipelined self-timed WRITE cycles and provide fully coherent data for all combinations of READS and WRITES. A READ can immediately follow a WRITE even if they are to the same address. Although the WRITE data has not been written to the memory array, the SRAM will deliver the data from the write register instead of using the older data from the memory array. The latest data is always utilized for all bus transactions. WRITE cycles are initiated every second K rising edge. Any command in between is ignored, since the burst sequence may not be interrupted.

**Figure 2:**  
**Functional Block Diagram: 512K x 18**



### NOTE:

1. The functional block diagram illustrates simplified device operation. See truth tables, ball descriptions, and timing diagrams for detailed information.
2.  $n = 17$





**Table 2: Ball Assignment (Top View)  
165-Ball FBGA**

	1	2	3	4	5	6	7	8	9	10	11
A	DNU	V <sub>SS</sub> /SA <sup>1</sup>	NC/SA <sup>2</sup>	W#	BW1#	K#	NC	R#	NC/SA <sup>3</sup>	V <sub>SS</sub> /SA <sup>4</sup>	DNU
B	NC	Q9	D9	SA	NC	K	BW0#	SA	NC	NC	Q8
C	NC	NC	D10	V <sub>SS</sub>	SA	NC	SA	V <sub>SS</sub>	NC	Q7	D8
D	NC	D11	Q10	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	D7
E	NC	NC	Q11	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	D6	Q6
F	NC	Q12	D12	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	Q5
G	NC	D13	Q13	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	D5
H	NC	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	NC	NC	D14	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	Q4	D4
K	NC	NC	Q14	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	D3	Q3
L	NC	Q15	D15	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC	Q2
M	NC	NC	D16	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	Q1	D2
N	NC	D17	Q16	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

## NOTE:

1. Expansion address: 2A for 144Mb
2. Expansion address: 3A for 36Mb
3. Expansion address: 9A for 18Mb
4. Expansion address: 10A for 72Mb



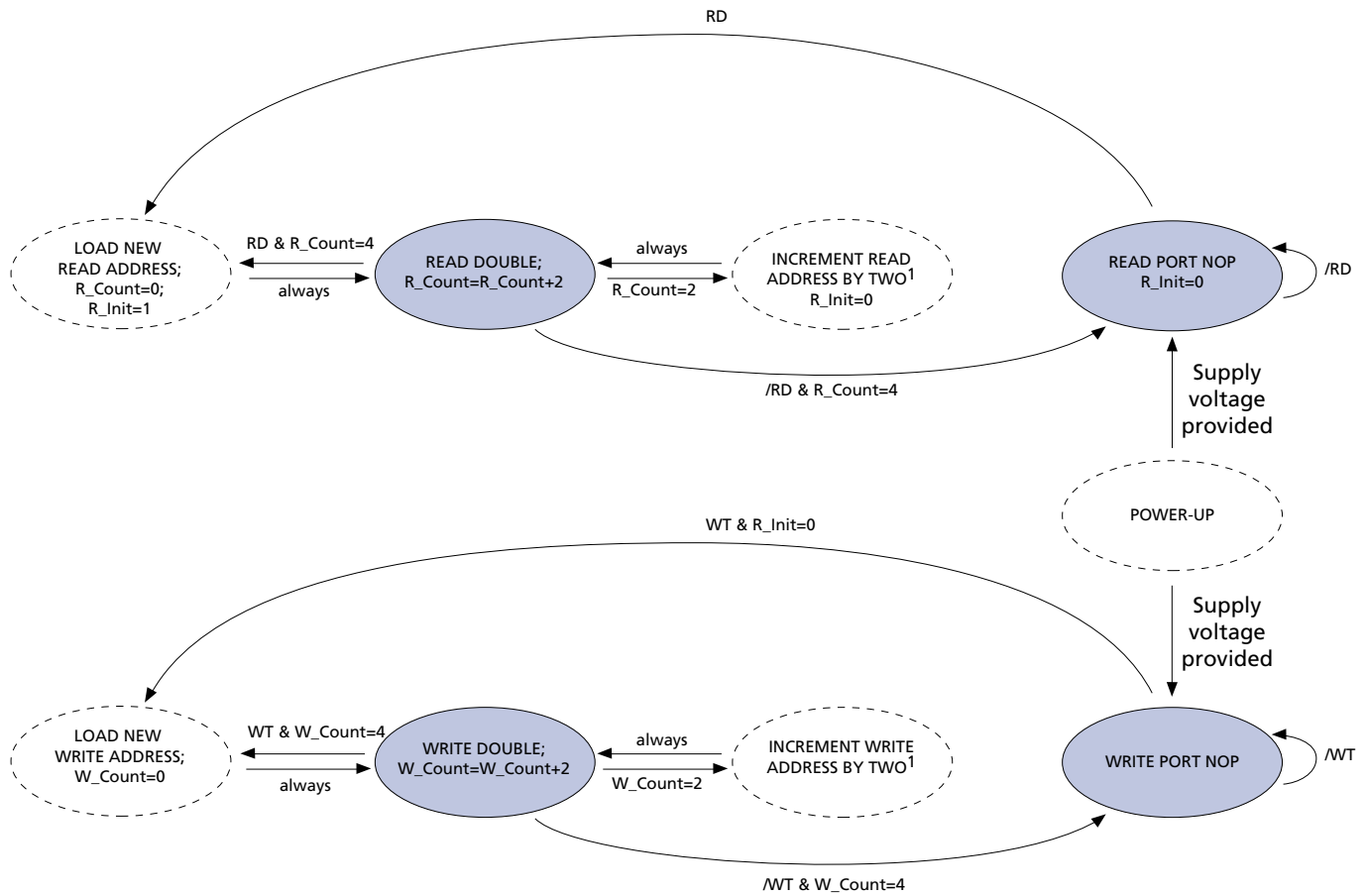
Table 3: Ball Descriptions

SYMBOL	TYPE	DESCRIPTION
SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. See Ball Assignment figures for address expansion inputs. All transactions operate on a burst of four 18-bit data (two clock periods of bus activity). These inputs are ignored when both ports are deselected.
R#	Input	Synchronous Read: When LOW, this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K and is ignored on the subsequent rising edge of K.
W#	Input	Synchronous Write: When LOW, this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K and is ignored on the subsequent rising edge of K. This input is also ignored if a READ cycle is being initiated.
BW0# BW1#	Input	Synchronous Byte Writes: When LOW, these inputs cause their respective bytes to be registered and written if W# had initiated a WRITE cycle. These signals must meet setup and hold times around the rising edges of K and K# for each of the four rising edges comprising the WRITE cycle. BW0# controls D0:D8, and BW1# controls D9:D17. See Ball Assignment figures for signal to data relationships.
K K#	Input	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
C C#	Input	Output Clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of C is used as the output timing reference for second and fourth output data. The rising edge of C# is used as the output reference for first and third output data. Ideally, C# is 180 degrees out of phase with C. C and C# may be tied HIGH to force the use of K and K# as the output reference clocks instead of having to provide C and C# clocks. If tied HIGH, these inputs may not be allowed to toggle during device operation.
TMS TDI	Input	IEEE 1149.1 Test Inputs: 2.5V I/O levels. These balls may be left as No Connects if the JTAG function is not used in the circuit.
TCK	Input	IEEE 1149.1 Clock Input: 2.5V I/O levels. This ball must be tied to V <sub>SS</sub> if the JTAG function is not used in the circuit.
VREF	Input	HSTL Input Reference Voltage: Nominally V <sub>DDQ</sub> /2, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffer trip point.
ZQ	Input	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 x R <sub>Q</sub> , where R <sub>Q</sub> is a resistor from this ball to ground. Alternately, this ball can be connected directly to V <sub>DDQ</sub> , which enables the minimum impedance mode. This ball cannot be connected directly to GND or left unconnected.
D <sub>-</sub>	Input	Synchronous Data Inputs: Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations. See Ball Assignment figures for ball site location of individual signals.
DNU	Output	Do Not Use: These balls should not be used.
TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 2.5V I/O level.
Q <sub>-</sub>	Output	Synchronous Data Outputs: Output data is synchronized to the respective C and C# or to K and K# rising edges if C and C# are tied HIGH. This bus operates in response to R# commands. See Ball Assignment figures for ball site location of individual signals.
VDD	Supply	Power Supply: 2.5V nominal. See DC Electrical Characteristics and Operating Conditions for range.
VDDQ	Supply	Power Supply: Isolated Output Buffer Supply. Nominally 1.5V. See DC Electrical Characteristics and Operating Conditions for range.
VSS	Supply	Power Supply: GND.


**Table 3: Ball Descriptions (Continued)**

SYMBOL	TYPE	DESCRIPTION
NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.
NC/SA		These balls are reserved for higher-order address bits, respectively.

**Figure 4:**  
**Bus Cycle State Diagram**



## NOTE:

1. The address is concatenated with 2 additional internal LSBs to facilitate burst operation. The address order is always fixed as: xxx...xxx+0, xxx...xxx+1, xxx...xxx+2, xxx...xxx+3. Bus cycle is terminated at the end of this sequence (burst count = 4).
2. State transitions: RD = (R# = LOW); WT = (W# = LOW).
3. Read and write state machines can be active simultaneously. Read and write cannot be simultaneously initiated. Read takes precedence.
4. State machine control timing sequence is controlled by K

**Table 4: Truth Table**

Notes 1-8

OPERATION	K	R#	W#	D or Q	D or Q	D or Q	D or Q
WRITE Cycle: Load address, input write data on two consecutive K and K# rising edges	L→H	H <sup>7</sup>	L <sup>8</sup>	DA(A + 0) at K(t + 1)↑	DA(A + 1) at K#(t + 1)↑	DA(A + 2) at K(t + 2)↑	DA(A + 3) at K#(t + 2)↑
READ Cycle: Load address, output data on two consecutive C and C# rising edges	L→H	L <sup>8</sup>	X	QA(A+0) at C(t + 1)↑	QA(A+1) at C#(t + 1)↑	QA(A+2) at C(t + 2)↑	QA(A+3) at C#(t + 2)↑
NOP: No operation	L→H	H	H	D = X Q = High-Z	D = X Q = High-Z	D = X Q = High-Z	D = X Q = High-Z
STANDBY: Clock stopped	Stopped	X	X	Previous State	Previous State	Previous State	Previous State

**Table 5: BYTE WRITE Operation**

Note 9

OPERATION	K	K#	BW0#	BW1#
WRITE D0-17 at K rising edge	L→H		0	0
WRITE D0-17 at K# rising edge		L→H	0	0
WRITE D0-8 at K rising edge	L→H		0	1
WRITE D0-8 at K# rising edge		L→H	0	1
WRITE D9-17 at K rising edge	L→H		1	0
WRITE D9-17 at K# rising edge		L→H	1	0
WRITE nothing at K rising edge	L→H		1	1
WRITE nothing at K# rising edge		L→H	1	1

## NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW. ↑ means rising edge; ↓ means falling edge.
2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges, except if C and C# are HIGH, then data outputs are delivered at K and K# rising edges.
3. R# and W# must meet setup and hold times around the rising edge (LOW to HIGH) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. It is recommended that K = /K# = C = /C# when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. If this signal was LOW to initiate the previous cycle, this signal becomes a "Don't Care" for this operation; however, it is strongly recommended that this signal is brought HIGH as shown in the Truth Table.
8. This signal was HIGH on previous K clock rising edge. Initiating consecutive READ or WRITE operations on consecutive K clock rising edges is not permitted. The device will ignore the second request.
9. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.





Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow. See Micron Technical Note TN-05-14 for more information.

### Absolute Maximum Ratings

Voltage on V <sub>DD</sub> Supply	
Relative to V <sub>SS</sub> .....	0.5V to +3.6V
Voltage on V <sub>DDQ</sub> Supply	
Relative to V <sub>SS</sub> .....	-0.5V to + V <sub>DD</sub>
V <sub>IN</sub> .....	-0.5V to V <sub>DD</sub> + 0.5V
Storage Temperature .....	-55°C to +125°C
Junction Temperature .....	+125°C
Short Circuit Output Current .....	±70mA

**Table 6: DC Electrical Characteristics And Operating Conditions**

Notes appear following parameter tables; 0°C ≤ T<sub>A</sub> ≤ +70°C; +2.4V ≤ V<sub>DD</sub> ≤ +2.6V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V <sub>IH</sub> (DC)	V <sub>REF</sub> + 0.1	V <sub>DDQ</sub> + 0.3	V	3, 4
Input Low (Logic 0) Voltage		V <sub>IL</sub> (DC)	-0.3	V <sub>REF</sub> - 0.1	V	3, 4
Clock Input Signal Voltage		V <sub>IN</sub>	-0.3	V <sub>DDQ</sub> + 0.3	V	3, 4
Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>DDQ</sub>	I <sub>LI</sub>	-5	5	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V <sub>IN</sub> ≤ V <sub>DDQ</sub> (Q)	I <sub>LO</sub>	-5	5	µA	
Output High Voltage	I <sub>OH</sub>   ≤ 0.1mA	V <sub>OH</sub> (LOW)	V <sub>DDQ</sub> - 0.2	V <sub>DDQ</sub>	V	3, 5, 7
	Note 1	V <sub>OH</sub>	V <sub>DDQ</sub> /2 - 0.08	V <sub>DDQ</sub> /2 + 0.08	V	3, 5, 7
Output Low Voltage	I <sub>OL</sub> ≤ 0.1mA	V <sub>OL</sub> (LOW)	V <sub>SS</sub>	0.2	V	3, 5, 7
	Note 2	V <sub>OL</sub>	V <sub>DDQ</sub> /2 - 0.08	V <sub>DDQ</sub> /2 + 0.08	V	3, 5, 7
Supply Voltage		V <sub>DD</sub>	2.4	2.6	V	3
Isolated Output Buffer Supply		V <sub>DDQ</sub>	1.4	1.6	V	3, 6
Reference Voltage		V <sub>REF</sub>	0.68	0.9	V	3

**Table 7: AC Electrical Characteristics And Operating Conditions**

Notes appear following parameter tables; 0°C ≤ T<sub>A</sub> ≤ +70°C; +2.4V ≤ V<sub>DD</sub> ≤ +2.6V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V <sub>IH</sub> (AC)	V <sub>REF</sub> + 0.2	-	V	3, 4, 8
Input Low (Logic 0) Voltage		V <sub>IL</sub> (AC)	-	V <sub>REF</sub> - 0.2	V	3, 4, 8

**Table 8: I<sub>DD</sub> Operating Conditions And Maximum Limits**Notes appear following parameter tables; 0°C ≤ T<sub>A</sub> ≤ +70°C; V<sub>DD</sub> = MAX unless otherwise noted

DESCRIPTION	CONDITIONS	SYM	TYP	MAX			UNITS	NOTES
				-6	-7.5	-10		
Operating Supply Current: DDR	All inputs ≤ V <sub>IL</sub> or ≥ V <sub>IH</sub> ; Cycle time ≥ t <sub>KHKH</sub> (MIN); Outputs open	I <sub>DD</sub>	400	550	500	375	mA	9, 10, 11
Standby Supply Current: NOP	t <sub>KHKH</sub> = t <sub>KHKH</sub> (MIN); Device in NOP state; All addresses/data static	I <sub>SB1</sub>	150	250	225	175	mA	10, 12
Stop Clock Current	Cycle time = 0; Input Static	I <sub>SB</sub>	TBD	75	75	75	mA	10
Output Supply Current: DDR (Information only)	C <sub>L</sub> = 15pF	I <sub>DDQ</sub>		34	27	20	mA	13

**Table 9: Capacitance**

Note 14; notes appear following parameter tables

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Address/Control Input Capacitance	T <sub>A</sub> = 25°C; f = 1 MHz	C <sub>I</sub>	4	5	pF
Output Capacitance (D, Q)		C <sub>O</sub>	6	7	pF
Clock Capacitance		C <sub>CK</sub>	5	6	pF

**Table 10: Thermal Resistance**

Note 14; notes appear following parameter tables

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Soldered on a 4.25 x 1.125 inch, 4-layer, printed circuit board	θ <sub>JA</sub>	25	°C/W	15
Junction to Case (Top)		θ <sub>JC</sub>	10	°C/W	
Junction to Balls (Bottom)		θ <sub>JB</sub>	12	°C/W	16


**Table 11: AC Electrical Characteristics And Recommended Operating Conditions**

 Notes 14, 17-19; notes appear following parameter tables;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $+2.4\text{V} \leq V_{DD} \leq +2.6\text{V}$ 

DESCRIPTION	SYM	-6		-7.5		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
<b>Clock</b>									
Clock cycle time (K, K#, C, C#)	t <sub>KHKH</sub>	6.0		7.5		10		ns	
Clock HIGH time (K, K#, C, C#)	t <sub>KHKL</sub>	2.4		3.0		3.5		ns	
Clock LOW time (K, K#, C, C#)	t <sub>KLKH</sub>	2.4		3.0		3.5		ns	
Clock to clock# (K↑→K#↑, C↑→C#↑) at t <sub>KHKH</sub> minimum	t <sub>KHK#H</sub>	2.7		3.4		4.6		ns	
Clock# to clock (K↑→K#↑, C↑→C#↑) at t <sub>KHKH</sub> minimum	t <sub>K#HKH</sub>	2.7		3.4		4.6		ns	
Clock to data clock (K↑→C↑, K#↑→C#↑)	t <sub>KHCH</sub>	0.0	2.0	0.00	2.5	0.0	3.0	ns	
<b>Output Times</b>									
C, C# HIGH to output valid	t <sub>CHQV</sub>		2.5		3.0		3.0	ns	
C, C# HIGH to output hold	t <sub>CHQX</sub>	1.2		1.2		1.2		ns	
C HIGH to output High-Z	t <sub>CHQZ</sub>		2.5		3.0		3.0	ns	20, 21
C HIGH to output Low-Z	t <sub>CHQX1</sub>	1.2		1.2		1.2		ns	20, 21
<b>Setup Times</b>									
Address valid to K rising edge	t <sub>AVKH</sub>	0.7		0.8		1.0		ns	
Control inputs valid to K rising edge	t <sub>IVKH</sub>	0.7		0.8		1.0		ns	
Data-in valid to K, K# rising edge	t <sub>DVKH</sub>	0.7		0.8		1.0		ns	20, 21
<b>Hold Times</b>									20, 21
K rising edge to address hold	t <sub>KHAX</sub>	0.7		0.8		1.0		ns	
K rising edge to control inputs hold	t <sub>KHIX</sub>	0.7		0.8		1.0		ns	22
K, K# rising edge to data-in hold	t <sub>KHDX</sub>	0.7		0.8		1.0		ns	22



## Notes

1. Outputs are impedance-controlled.  $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$  for values of  $175\Omega \leq RQ \leq 350\Omega$ .
2. Outputs are impedance-controlled.  $I_{OL} = (V_{DDQ}/2)/(RQ/5)$  for values of  $175\Omega \leq RQ \leq 350\Omega$ .
3. All voltages referenced to V<sub>SS</sub> (GND).
4. Overshoot:  $V_{IH(AC)} \leq V_{DD} + 0.7V$  for  $t \leq t_{KHKH}/2$   
 Undershoot:  $V_{IL(AC)} \geq -0.5V$  for  $t \leq t_{KHKH}/2$   
 Power-up:  $V_{IH} \leq V_{DDQ} + 0.3V$  and  $V_{DD} \leq 2.4V$  and  $V_{DDQ} \leq 1.4V$  for  $t \leq 200ms$   
 During normal operation, V<sub>DDQ</sub> must not exceed V<sub>DD</sub>. R# and W# signals may not have pulse widths less than  $t_{KHKL}$  (MIN) or operate at cycle rates less than  $t_{KHKH}$  (MIN).
5. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
6. For higher V<sub>DDQ</sub> voltages, contact factory for product information.
7. HSTL outputs meet JEDEC HSTL Class I and Class II standards.
8. To maintain a valid level, the transitioning edge of the input must:
  - a. Sustain a constant slew rate from the current AC level through the target AC level,  $V_{IL(AC)}$  or  $V_{IH(AC)}$
  - b. Reach at least the target AC level
  - c. After the AC target level is reached, continue to maintain at least the target DC level,  $V_{IL(DC)}$  or  $V_{IH(DC)}$
9. IDD is specified with no output current and increases with faster cycle times. IDDQ increases with faster cycle times and greater output loading. Typical value is measured at 7.5ns cycle time.
10. Typical values are measured at V<sub>DD</sub> = 2.5V, V<sub>DDQ</sub> = 1.5V, and temperature = 25°C.
11. Operating supply currents and burst mode currents are calculated with 50 percent READ cycles and 50 percent WRITE cycles.
12. NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.
13. Average I/O current and power is provided for informational purposes only and is not tested. Calculation assumes that all outputs are loaded with C<sub>L</sub> (in farads), f = input clock frequency, half of outputs toggle at each transition (for example, n = 18 for x36), C<sub>0</sub> = 6pF, V<sub>DDQ</sub> = 1.5V and uses the equations: Average I/O Power as dissipated by the SRAM is:  

$$P = 0.5 \times n \times f \times V_{DDQ}^2 \times (C_L + 2C_0)$$

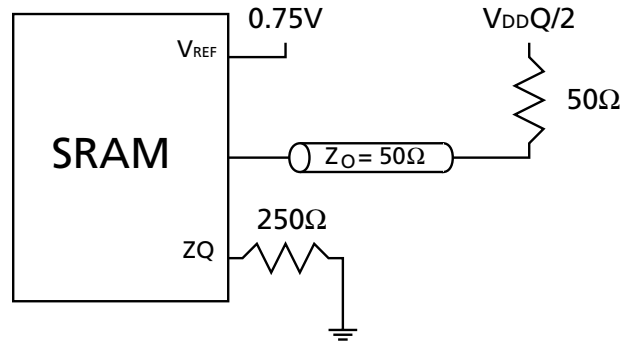
$$\text{Average } I_{DDQ} = n \times f \times V_{DDQ} \times (C_L + C_0)$$
14. This parameter is sampled.
15. Average thermal resistance between the die and the case top surface per MIL SPEC 883 Method 1012.1.
16. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.
17. Control input signals may not be operated with pulse widths less than  $t_{KHKL}$  (MIN).
18. Test conditions as specified with the output loading as shown in Figure 5, unless otherwise noted.
19. If C, C# are tied HIGH, then K, K# become the references for C, C# timing parameters.
20. Transition is measured  $\pm 100mV$  from steady state voltage.
21.  $t_{CHQXI}$  is greater than  $t_{CHQZ}$  at any given voltage and temperature.
22. This is a synchronous device. All addresses, data, and control lines must meet the specified setup and hold times for all latching clock edges.



**AC Test Conditions**

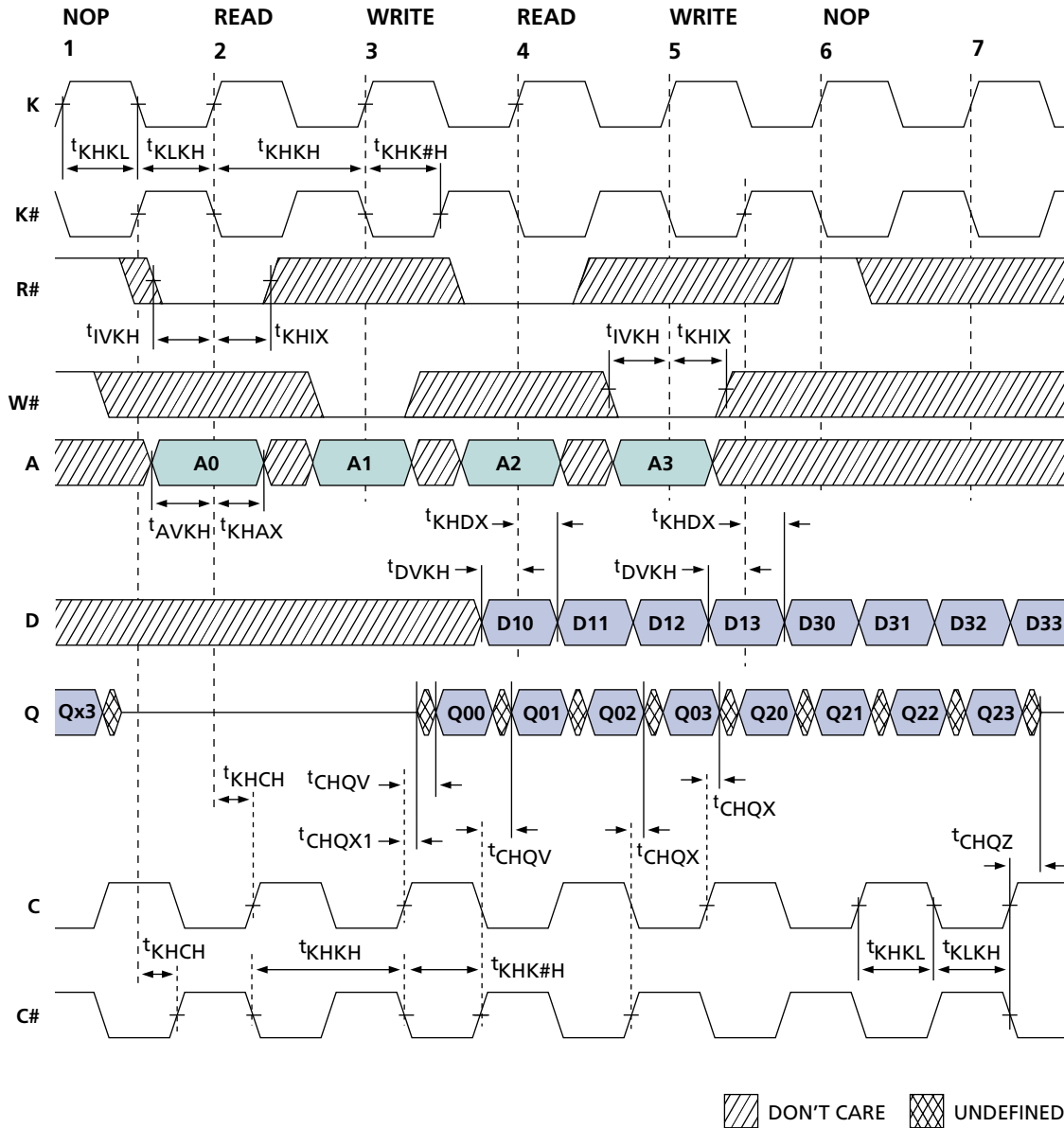
Input pulse levels . . . . .	0.25V to 1.25V
Input rise and fall times . . . . .	0.7ns
Input timing reference levels . . . . .	0.75V
Output reference levels . . . . .	V <sub>DDQ</sub> /2
Z <sub>Q</sub> for 50Ω impedance . . . . .	250Ω
Output load . . . . .	See Figure 5

**Figure 5:  
Output Load Equivalent**





**Figure 6:  
READ/WRITE Timing**



**NOTE:**

1. Q00 refers to output from address A0 + 0. Q01 refers to output from the next internal burst address following A0, i.e., A0 + 1, etc.
2. Outputs are disabled (High-Z) one clock cycle after a NOP.
3. In this example, if address A0 = A1, data Q20 = D10, Q21 = D11. Write data is forwarded immediately as read results.



## IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The QDR SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-2001 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully-compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V<sub>ss</sub>) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V<sub>DD</sub> through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

### Test Access Port (TAP)

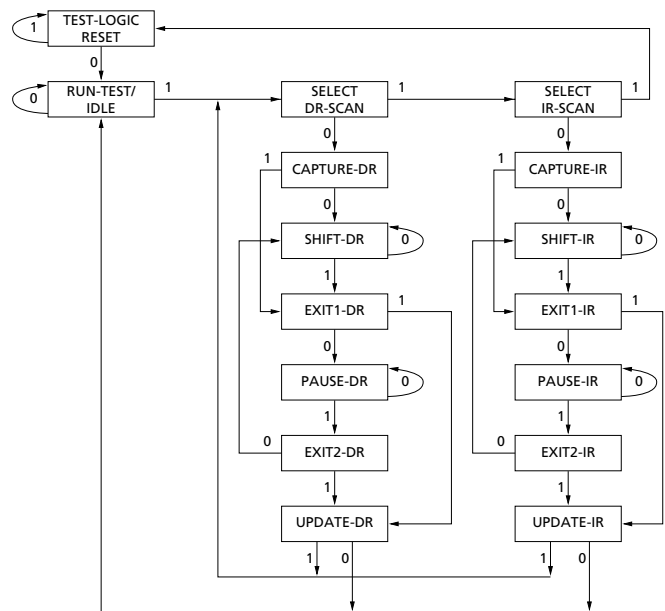
#### Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

#### Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

**Figure 7:**  
**TAP Controller State Diagram**



NOTE:

The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

### Test Data-In (TDI)

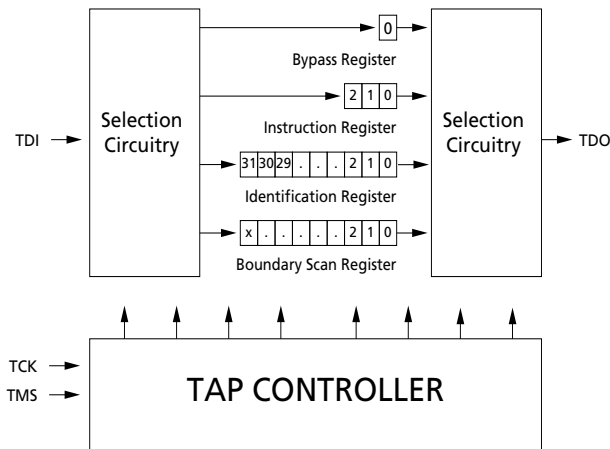
The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between the TDI and TDO balls is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 7. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most-significant bit (MSB) of any register, as shown in Figure 8.

### Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine, as depicted in Figure 7.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register, illustrated in Figure 8.)



**Figure 8:**  
**TAP Controller Block Diagram**



NOTE:

X = 69 for all configurations.

### Performing a TAP RESET

A reset is performed by forcing TMS HIGH (V<sub>DD</sub>) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

### TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

### Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in Figure 2. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two LSBs are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

### Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V<sub>SS</sub>) when the BYPASS instruction is executed.

### Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several no connect (NC) balls are also included in the scan register to reserve balls. The SRAM has a 69-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

### Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

### TAP Instruction Set Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load





### Overview (continued)

address, data, or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register and through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

### EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, hence this device is not IEEE 1149.1 compliant.

The TAP controller does not recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. EXTEST does not place the SRAM outputs in a High-Z state.

### IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins/balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

### SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bi-directional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (tCS plus tCH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

### BYPASS

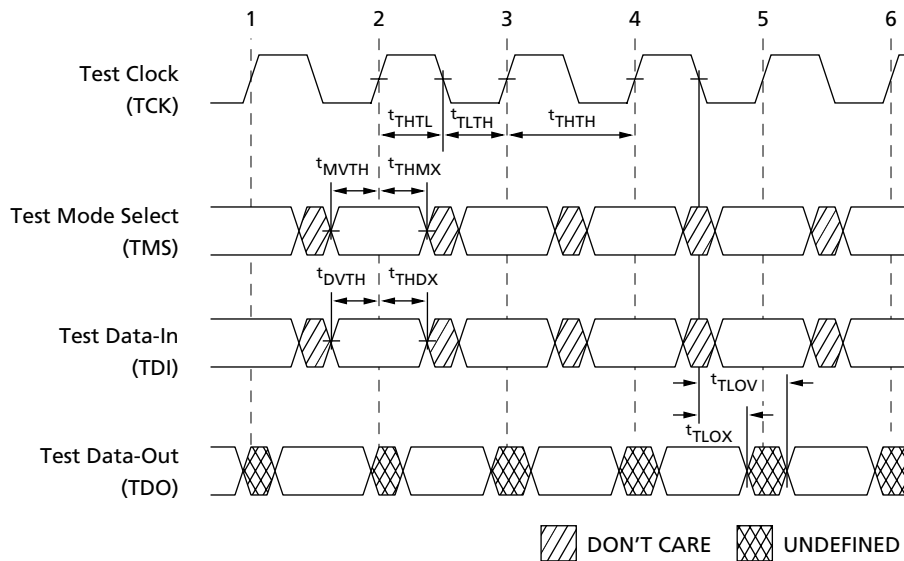
When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

### RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.



**Figure 9:  
TAP Timing**



**Table 12: TAP DC Electrical Characteristics**

Notes 1, 2; 0°C ≤ T<sub>A</sub> ≤ +70°C; +2.4V ≤ V<sub>DD</sub> ≤ +2.6V

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
<b>Clock</b>				
Clock cycle time	t <sub>THTH</sub>	100		ns
Clock frequency	f <sub>TF</sub>		10	MHz
Clock HIGH time	t <sub>THTL</sub>	40		ns
Clock LOW time	t <sub>TLTH</sub>	40		ns
<b>Output Times</b>				
TCK LOW to TDO unknown	t <sub>TLOX</sub>	0		ns
TCK LOW to TDO valid	t <sub>TLOV</sub>		20	ns
TDI valid to TCK HIGH	t <sub>DVTH</sub>	10		ns
TCK HIGH to TDI invalid	t <sub>THDX</sub>	10		ns
<b>Setup Times</b>				
TMS setup	t <sub>MVTH</sub>	10		ns
Capture setup	t <sub>CS</sub>	10		ns
<b>Hold Times</b>				
TMS hold	t <sub>THMX</sub>	10		ns
Capture hold	t <sub>CH</sub>	10		ns

NOTE:

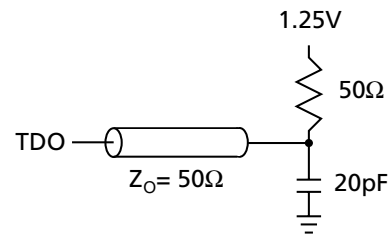
1. t<sub>CS</sub> and t<sub>CH</sub> refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 10.



### TAP AC Test Conditions

Input pulse levels . . . . .	V <sub>SS</sub> to 2.5V
Input rise and fall times . . . . .	1ns
Input timing reference levels . . . . .	1.25V
Output reference levels . . . . .	1.25V
Test load termination supply voltage . . . . .	1.25V

**Figure 10:**  
**TAP AC Output Load Equivalent**



### TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

0°C ≤ T<sub>A</sub> ≤ +70°C; +1.7V ≤ V<sub>DD</sub> ≤ +1.9V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V <sub>IH</sub>	1.7	V <sub>DD</sub> + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V <sub>IL</sub>	-0.3	0.7	V	1, 2
Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	I <sub>LI</sub>	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V <sub>IN</sub> ≤ V <sub>DDQ</sub> (DQx)	I <sub>LO</sub>	-5.0	5.0	µA	
Output Low Voltage	I <sub>OLC</sub> = 100µA	V <sub>OL1</sub>		0.2	V	
Output Low Voltage	I <sub>OLT</sub> = 2mA	V <sub>OL2</sub>		0.7	V	1
Output High Voltage	I <sub>OHC</sub> = -100µA	V <sub>OH1</sub>	2.1		V	1
Output High Voltage	I <sub>OHT</sub> = -2mA	V <sub>OH1</sub>	1.7		V	1

#### NOTE:

- All voltages referenced to V<sub>SS</sub> (GND).
- Overshoot: V<sub>IH(AC)</sub> ≤ V<sub>DD</sub> + 0.7V for t ≤ <sup>t</sup>KHKH/2  
 Undershoot: V<sub>IL(AC)</sub> ≥ -0.5V for t ≤ <sup>t</sup>KHKH/2  
 Power-up: V<sub>IH</sub> ≤ +2.6 and V<sub>DD</sub> ≤ +2.4V and V<sub>DDQ</sub> ≤ 1.4V for t ≤ 200ms  
 During normal operation, V<sub>DDQ</sub> must not exceed V<sub>DD</sub>. Control input signals (LD#, R/W#, etc.) may not have pulse widths less than <sup>t</sup>KHKL (MIN) or operate at frequencies exceeding <sup>f</sup>KF (MAX).

**Table 13: Identification Register Definitions**

INSTRUCTION FIELD	512K x 18	DESCRIPTION
REVISION NUMBER (31:28)	000	Version number.
DEVICE ID (28:12)	00011000011000000	512K x 18 QDR 4-word burst.
MICRON JEDEC ID CODE (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

**Table 14: Scan Register Sizes**

REGISTER NAME	BIT SIZE (x18)
Instruction	3
Bypass	1
ID	32
Boundary Scan	69

**Table 15: Instruction Codes**

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This operation does not affect SRAM operations. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operations. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

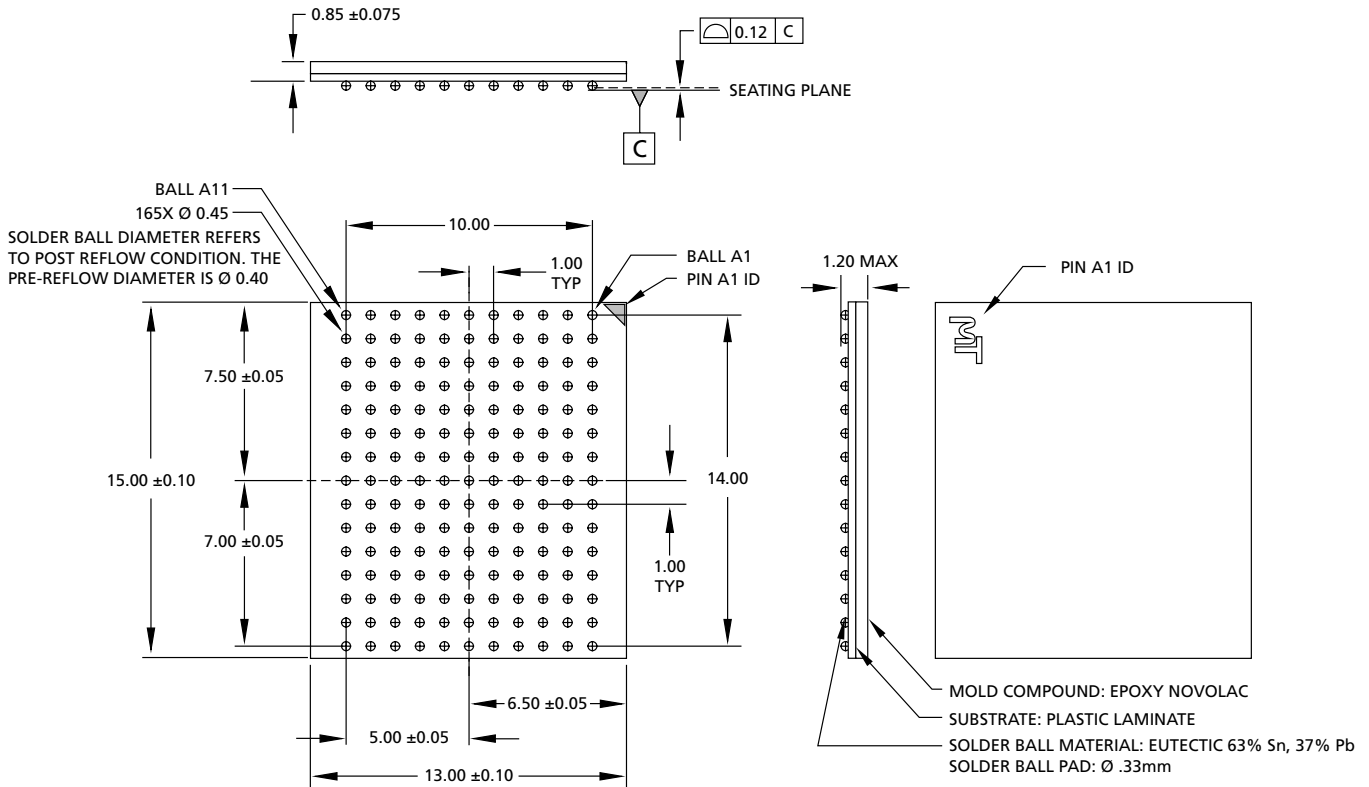

**Table 16: Boundary Scan (Exit) Order**

BIT#	SIGNAL NAME	BALL ID
1	C#	6R
2	C	6P
3	SA	6N
4	SA	7P
5	SA	7N
6	SA	7R
7	SA	8R
8	SA	8P
9	SA	9R
10	D0	10P
11	Q0	11P
12	D1	11N
13	Q1	10M
14	D2	11M
15	Q2	11L
16	D3	10K
17	Q3	11K
18	D4	11J
19	ZQ	11H
20	Q4	10J
21	D5	11G
22	Q5	11F
23	D6	10E
24	Q6	11E
25	D7	11D
26	Q7	10C
27	D8	11C
28	Q8	11B
29	Reserved	11A; reads as X
30	GND/SA20	10A; reads as 0
31	NC/SA18	9A; reads as 1
32	SA	8B
33	SA	7C
34	NC	6C; reads as 0
35	R#	8A

BIT#	SIGNAL NAME	BALL ID
36	BW0#	7B
37	K	6B
38	K#	6A
39	BW1#	5A
40	W#	4A
41	SA	5C
42	SA	4B
43	NC/SA19	3A; reads as 1
44	GND/SA21	2A; reads as 0
45	Reserved	1A; reads as X
46	D9	3B
47	Q9	2B
48	D10	3C
49	Q10	3D
50	D11	2D
51	Q11	3E
52	D12	3F
53	Q12	2F
54	D13	2G
55	Q13	3G
56	D14	3J
57	Q14	3K
58	D15	3L
59	Q15	2L
60	D16	3M
61	Q16	3N
62	D17	2N
63	Q17	3P
64	SA	3R
65	SA	4R
66	SA	4P
67	SA	5P
68	SA	5N
69	SA	5R



**Figure 11:  
165-Ball FBGA**



**NOTE:**

1. All dimensions are in millimeters.

**DATA SHEET DESIGNATION**

Advance: This data sheet contains initial descriptions of products still under development.



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**Revision History**

- New ADVANCE data sheet for 0.16µm process, Rev. A, Pub. 10 /02 .....10/02