CY7C1354DV25, CY7C1356DV25

9-Mbit (256K x 36/512K x 18) Pipelined SRAM with NoBL™ Architecture

Features

- Pin compatible with and functionally equivalent to ZBT™
- Supports 250 MHz bus operations with zero wait states
- Available speed grades are 250, 200, and 166 MHz
- Internally self timed output buffer control to eliminate the need to use asynchronous $\overline{OE}$
- Fully registered (inputs and outputs) for pipelined operation
- Byte Write capability
- Single 2.5V power supply (V_{DD})
- Fast clock-to-output times
  - 2.8 ns (for 250 MHz device)
- Clock Enable ($\overline{CEN}$) pin to suspend operation
- Synchronous self timed writes
- Available in Pb-free 100-pin TQFP package, Pb-free and non Pb-free 119-ball BGA package, and 165-ball FBGA package
- IEEE 1149.1 JTAG compatible boundary scan
- Burst capability–linear or interleaved burst order
- “ZZ” Sleep mode and Stop Clock options

Functional Description

The CY7C1354DV25 and CY7C1356DV25 are 2.5V, 256K x 36 and 512K x 18 Synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back to back read and write operations with no wait states. The CY7C1354DV25 and CY7C1356DV25 are equipped with the advanced (NoBL) logic required to enable consecutive read and write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent write and read transitions. The CY7C1354DV25 and CY7C1356DV25 are pin compatible with and functionally equivalent to ZBT devices.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.

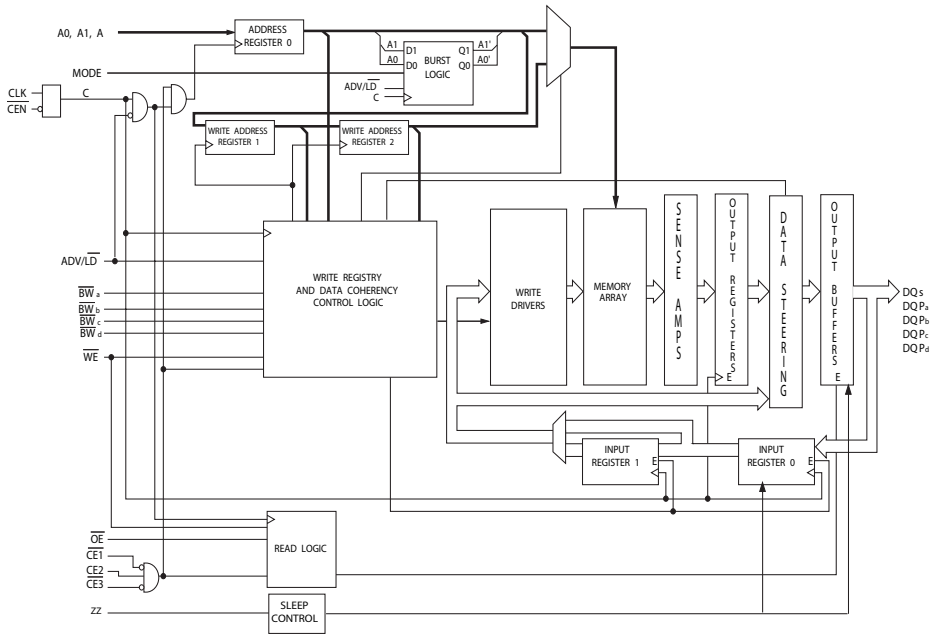
Write operations are controlled by the Byte Write Selects ($\overline{BW_a}$–$\overline{BW_d}$ for CY7C1354DV25 and $\overline{BW_a}$–$\overline{BW_b}$ for CY7C1356DV25) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence. For best practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

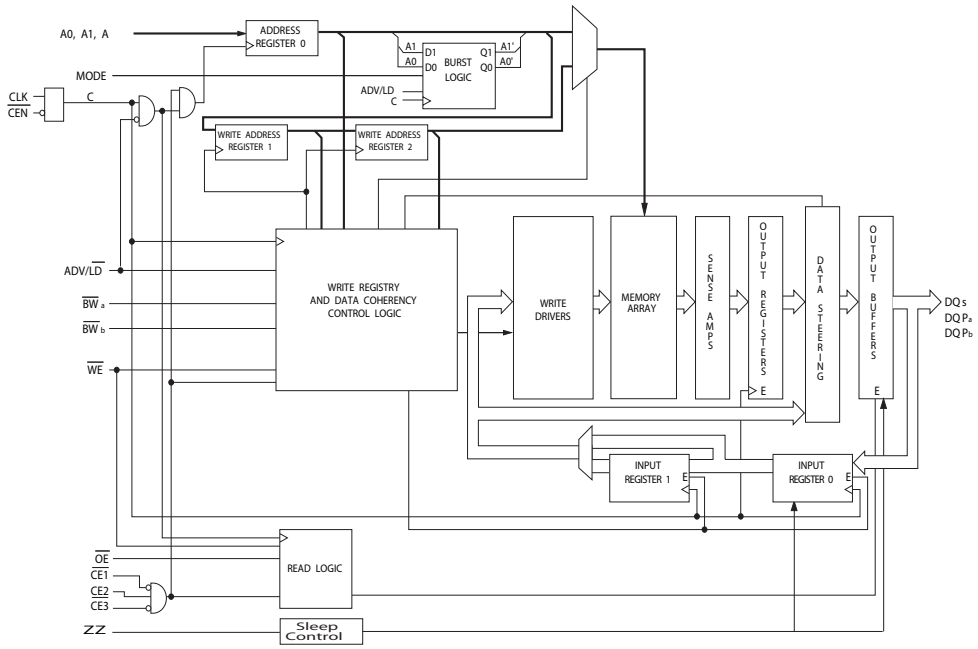
Selection Guide

Description	250 MHz	200 MHz	166 MHz	Unit
Maximum Access Time	2.8	3.2	3.5	ns
Maximum Operating Current	250	220	180	mA
Maximum CMOS Standby Current	40	40	40	mA

Logic Block Diagram – CY7C1354DV25 (256K x 36)



Logic Block Diagram – CY7C1356DV25 (512K x 18)

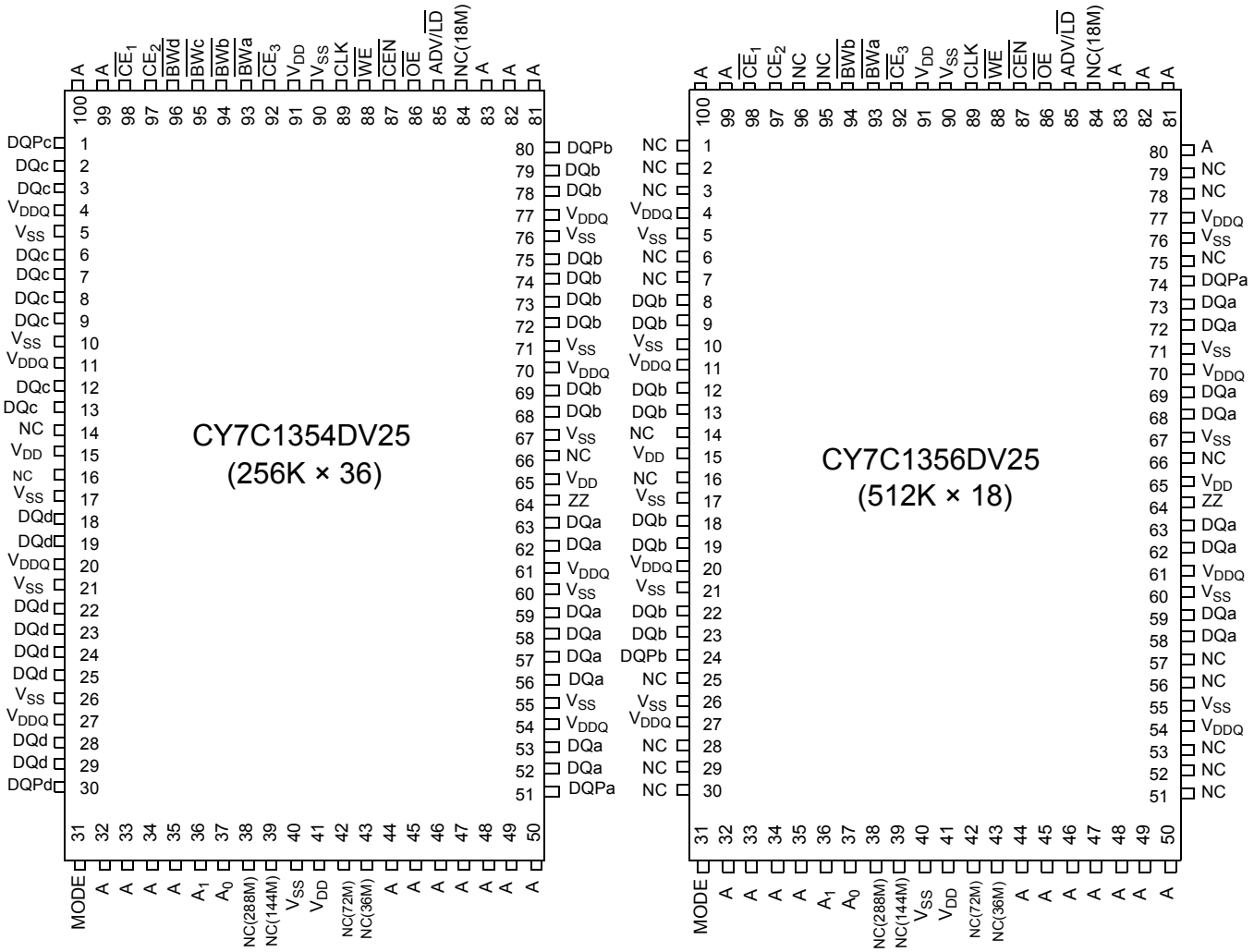


Contents

Pin Configuration

The pin configuration for CY7C1354DV25 and CY7C1356DV25 follow.

100-Pin TQFP Pinout



Pin Configuration (continued)

The pin configuration for CY7C1354DV25 and CY7C1356DV25 follow.

119-Ball BGA Pinout CY7C1354DV25 (256K x 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC/18M	A	A	V_{DDQ}
B	NC/576M	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC/1G	A	A	V_{DD}	A	A	NC
D	DQ_c	DQP_c	V_{SS}	NC	V_{SS}	DQP_b	DQ_b
E	DQ_c	DQ_c	V_{SS}	$\overline{CE_1}$	V_{SS}	DQ_b	DQ_b
F	V_{DDQ}	DQ_c	V_{SS}	$\overline{OE}$	V_{SS}	DQ_b	V_{DDQ}
G	DQ_c	DQ_c	$\overline{BW_c}$	A	$\overline{BW_b}$	DQ_b	DQ_b
H	DQ_c	DQ_c	V_{SS}	$\overline{WE}$	V_{SS}	DQ_b	DQ_b
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_d	DQ_d	V_{SS}	CLK	V_{SS}	DQ_a	DQ_a
L	DQ_d	DQ_d	$\overline{BW_d}$	NC	$\overline{BW_a}$	DQ_a	DQ_a
M	V_{DDQ}	DQ_d	V_{SS}	$\overline{CEN}$	V_{SS}	DQ_a	V_{DDQ}
N	DQ_d	DQ_d	V_{SS}	A1	V_{SS}	DQ_a	DQ_a
P	DQ_d	DQP_d	V_{SS}	A0	V_{SS}	DQP_a	DQ_a
R	NC/144M	A	MODE	V_{DD}	NC	A	NC/288M
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

119-Ball BGA Pinout CY7C1356DV25 (512K x 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC/18M	A	A	V_{DDQ}
B	NC/576M	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC/1G	A	A	V_{DD}	A	A	NC
D	DQ_b	NC	V_{SS}	NC	V_{SS}	DQP_a	NC
E	NC	DQ_b	V_{SS}	$\overline{CE_1}$	V_{SS}	NC	DQ_a
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_a	V_{DDQ}
G	NC	DQ_b	$\overline{BW_b}$	A	V_{SS}	NC	DQ_a
H	DQ_b	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQ_a	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_b	V_{SS}	CLK	V_{SS}	NC	DQ_a
L	DQ_b	NC	V_{SS}	NC	$\overline{BW_a}$	DQ_a	NC
M	V_{DDQ}	DQ_b	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	DQ_b	NC	V_{SS}	A1	V_{SS}	DQ_a	NC
P	NC	DQP_b	V_{SS}	A0	V_{SS}	NC	DQ_a
R	NC/144M	A	MODE	V_{DD}	NC	A	NC/288M
T	NC/72M	A	A	NC/36M	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configuration (continued)

The pin configuration for CY7C1354DV25 and CY7C1356DV25 follow.

165-Ball FBGA Pinout CY7C1354DV25 (256K x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE_1}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{CE_3}$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC/1G	A	CE_2	$\overline{BW_d}$	$\overline{BW_a}$	CLK	$\overline{WE}$	$\overline{OE}$	NC/18M	A	NC
C	DQP_c	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_b
D	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
E	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
F	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
G	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
K	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
L	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
M	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
N	DQP_d	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_a
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

165-Ball FBGA Pinout CY7C1356DV25 (512K x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE_1}$	$\overline{BW_b}$	NC	$\overline{CE_3}$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	A
B	NC/1G	A	CE_2	NC	$\overline{BW_a}$	CLK	$\overline{WE}$	$\overline{OE}$	NC/18M	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_a
D	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
E	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
F	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
G	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
K	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
L	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
M	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
N	DQP_b	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Pin Name	IO	Pin Description
A0 A1 A	Input-Synchronous	**Address Inputs used to Select One of the Address Locations**. Sampled at the rising edge of the CLK.
$\overline{BW_a}$, $\overline{BW_b}$, $\overline{BW_c}$, $\overline{BW_d}$,	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW_a}$ controls DQ_a and DQP_a, $\overline{BW_b}$ controls DQ_b and DQP_b, $\overline{BW_c}$ controls DQ_c and DQP_c, $\overline{BW_d}$ controls DQ_d and DQP_d.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance or Load Input used to Advance the On-Chip Address Counter or Load a New Address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE_1}$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select and deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select and deselect the device.
$\overline{CE_3}$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select and deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a Write sequence, during the first clock when emerging from a deselected state and when the device is deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Because deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_S	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by addresses during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional Data Parity I/O Lines**. Functionally, these signals are identical to $DQ_{[a:d]}$. During write sequences, DQP_a is controlled by $\overline{BW_a}$, DQP_b is controlled by $\overline{BW_b}$, DQP_c is controlled by $\overline{BW_c}$, and DQP_d is controlled by $\overline{BW_d}$.
MODE	Input Strap Pin	**Mode Input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE is default HIGH, to an interleaved burst order.
TDO	JTAG Serial Output Synchronous	**Serial Data-Out to the JTAG Circuit**. Delivers data on the negative edge of TCK.
TDI	JTAG Serial Input Synchronous	**Serial Data-In to the JTAG Circuit**. Sampled on the rising edge of TCK.

Pin Definitions (continued)

Pin Name	IO	Pin Description
TMS	Test Mode Select Synchronous	**Controls the Test Access Port State Machine**. Sampled on the rising edge of TCK.
TCK	JTAG-Clock	**Clock Input to the JTAG Circuitry**.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O Circuitry**.
V_{SS}	Ground	**Ground for the Device**. Should be connected to ground of the system.
NC	–	**No Connects**. This pin is not connected to the die.
NC (18, 36, 72, 144, 288, 576, 1G	–	**These Pins are not Connected**. They will be used for expansion to the 18M, 36M, 72M, 144M 288M, 576M, and 1G densities.
ZZ	Input-Asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.

Functional Overview

The CY7C1354DV25 and CY7C1356DV25 are synchronous pipelined Burst NoBL SRAMs designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.8 ns (250 MHz device).

Accesses are initiated by asserting all three Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). $BW_{[d:a]}$ can be used to conduct Byte Write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/$\overline{LD}$ must be driven LOW when the device is deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 2.8 ns (250 MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW for the device to drive out the requested data. During the second clock, a subsequent operation (read, write, and deselect) is initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output tri-states following the next clock rise.

Burst Read Accesses

The CY7C1354DV25 and CY7C1356DV25 have an on-chip burst counter that provides the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load a new address into the SRAM, as described in the Single Read Accesses section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ increments the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{CE_3}$ are ALL asserted active, and (3) the write signal $\overline{WE}$ is asserted LOW. The address presented to $A_0 \angle A_{16}$ is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically tri-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354DV25 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356DV25). In addition, the address for the subsequent access (read, write, and deselect) is latched into the address register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354DV25 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356DV25) (or a subset for byte write operations, see Write Cycle Description tables for details) inputs is latched into the device and the write is complete.

The data written during the write operation is controlled by $\overline{BW}$ ($\overline{BW_{a,b,c,d}}$ for CY7C1354DV25 and $\overline{BW_{a,b}}$ for CY7C1356DV25) signals. The CY7C1354DV25/CY7C1356DV25 provides Byte Write capability that is described in the Write Cycle Description tables. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BW}$) input selectively writes to only the desired bytes. Bytes not selected during a Byte Write operation remains unaltered. A synchronous self timed write mechanism is provided to simplify the write operations. Byte Write capability is included to greatly simplify read, modify, and write sequences, which can be reduced to simple Byte Write operations.

Because the CY7C1354DV25 and CY7C1356DV25 are common I/O devices, data should not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354DV25 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356DV25) inputs. Doing so tri-states the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354DV25 and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356DV25) are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1354DV25 and CY7C1356DV25 has an on-chip burst counter that provides the ability to supply a single address and conduct up to four WRITE operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load the initial address, as described in the Single Write Access section above. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE_1}$, CE_2, and $\overline{CE_3}$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}$ ($\overline{BW_{a,b,c,d}}$ for CY7C1354DV25 and $\overline{BW_{a,b}}$ for CY7C1356DV25) inputs must be driven in each cycle of the burst write to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. When in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address	Second Address	Third Address	Fourth Address
A1,A0	A1,A0	A1,A0	A1,A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address	Second Address	Third Address	Fourth Address
A1,A0	A1,A0	A1,A0	A1,A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq V_{DD} - 0.2V$		50	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table

The truth table for CY7C1354DV25 and CY7C1356DV25 follows.[1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE}$	ZZ	$\overline{ADV/LD}$	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	L	L	X	X	X	L	L-H	Tri-State
Continue Deselect Cycle	None	X	L	H	X	X	X	L	L-H	Tri-State
Read Cycle (Begin Burst)	External	L	L	L	H	X	L	L	L-H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	L	H	X	X	L	L	L-H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	L	L	H	X	H	L	L-H	Tri-State
Dummy Read (Continue Burst)	Next	X	L	H	X	X	H	L	L-H	Tri-State
Write Cycle (Begin Burst)	External	L	L	L	L	L	X	L	L-H	Data In (D)
Write Cycle (Continue Burst)	Next	X	L	H	X	L	X	L	L-H	Data In (D)
NOP/WRITE ABORT (Begin Burst)	None	L	L	L	L	H	X	L	L-H	Tri-State
WRITE ABORT (Continue Burst)	Next	X	L	H	X	H	X	L	L-H	Tri-State
IGNORE CLOCK EDGE (Stall)	Current	X	L	X	X	X	X	H	L-H	–
SLEEP MODE	None	X	H	X	X	X	X	X	X	Tri-State

Write Cycle Description

Write cycle description for CY7C1354DV25 follows.[1, 2, 3, 8]

Function	$\overline{WE}$	$\overline{BW_d}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	X	X	X	X
Write –No Bytes Written	L	H	H	H	H
Write Byte a– (DQ_a and $DQP_{a)}$	L	H	H	H	L
Write Byte b – (DQ_b and $DQP_{b)}$	L	H	H	L	H
Write Bytes b, a	L	H	H	L	L
Write Byte c – (DQ_c and $DQP_{c)}$	L	H	L	H	H
Write Bytes c, a	L	H	L	H	L
Write Bytes c, b	L	H	L	L	H
Write Bytes c, b, a	L	H	L	L	L
Write Byte d – (DQ_d and $DQP_{d)}$	L	L	H	H	H
Write Bytes d, a	L	L	H	H	L
Write Bytes d, b	L	L	H	L	H
Write Bytes d, b, a	L	L	H	L	L
Write Bytes d, c	L	L	L	H	H
Write Bytes d, c, a	L	L	L	H	L
Write Bytes d, c, b	L	L	L	L	H
Write All Bytes	L	L	L	L	L

Notes
1. X = “Don’t Care”, H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BWx}$ = L signifies at least one Byte Write Select is active, $\overline{BWx}$ = Valid signifies that the desired Byte Write Selects are asserted, see Write Cycle Description tables for details.
2. Write is defined by $\overline{WE}$ and $\overline{BW_X}$. See Write Cycle Description tablse for details.
3. When a write cycle is detected, all I/Os are tri-stated, even during Byte Writes.
4. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal.
5. $\overline{CEN}$ = H inserts wait states.
6. Device will power-up deselected and the I/Os in a tri-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = Tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs = data when $\overline{OE}$ is active.

Write cycle description for CY7C1356DV25 follows.[1, 2, 3, 8]

Function	$\overline{WE}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	x	x
Write – No Bytes Written	L	H	H
Write Byte a – (DQ_a and $DQP_{a)}$	L	H	L
Write Byte b – (DQ_b and $DQP_{b)}$	L	L	H
Write Both Bytes	L	L	L

IEEE 1149.1 Serial Boundary Scan (JTAG)

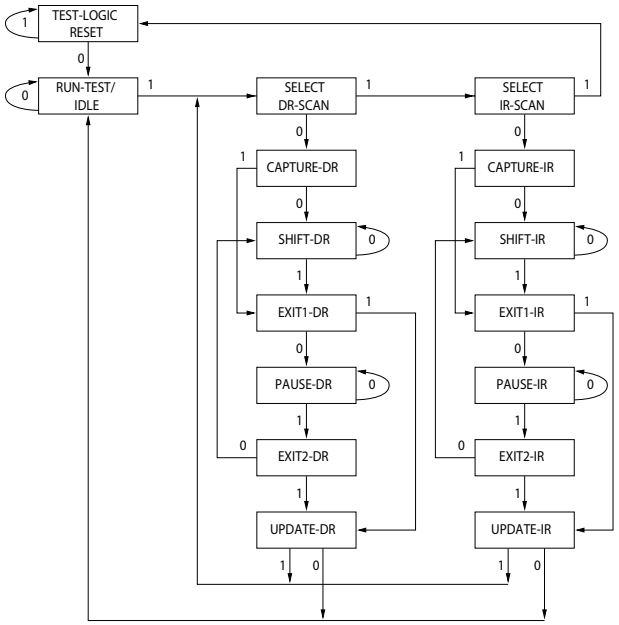
The CY7C1354DV25 and CY7C1356DV25 incorporates a serial boundary scan test access port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This part operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V I/O logic levels.

The CY7C1354DV25 and CY7C1356DV25 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. During power up, the device comes up in a reset state which does not interfere with the operation of the device.

Figure 1. TAP Controller State Diagram[9]



Notes

8. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_X$ is valid. Appropriate write will be done based on which byte write is active.
9. The 0/1 next to each state represents the value of TMS at the rising edge of the TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used.

The ball is pulled up internally, resulting in a logic HIGH level.

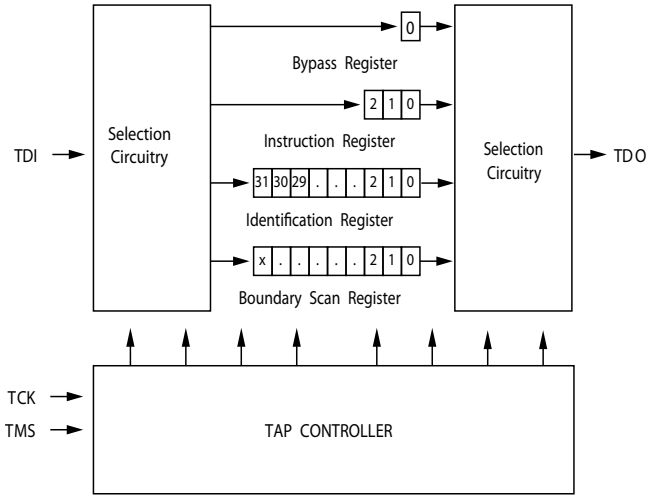
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 1. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 2.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 1.)

Figure 2. TAP Controller Block Diagram



Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

During power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in TAP Controller Block Diagram. During power up, the instruction register is loaded with the IDCODE instruction.

It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Identification Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register during power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is given during the “Update IR” state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

When the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

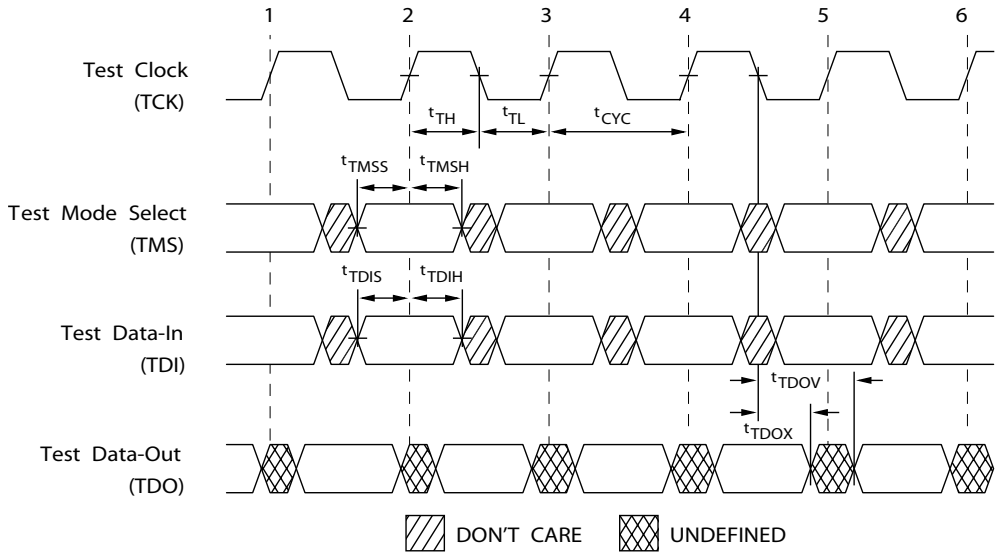
Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing

Figure 3 shows the TAP timings.

Figure 3. TAP Timing and Test Conditions



TAP AC Switching Characteristics

Over the Operating Range [10, 11]

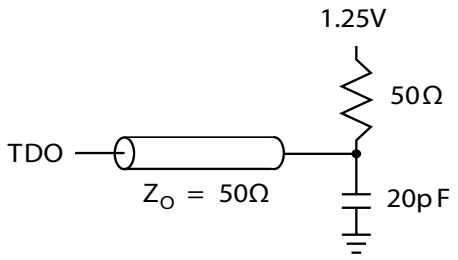
Parameter	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH Time	20		ns
t_{TL}	TCK Clock LOW Time	20		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

Notes
10. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

2.5V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 2.5V
Input rise and fall time ..... 1 ns
Input timing reference levels 1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

Figure 4. 2.5V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

(0°C < TA < +70°C; VDD = 2.5V ±0.125V unless otherwise noted)[12]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –1.0 mA, V_{DDQ} = 2.5V		2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA,V_{DDQ} = 2.5V		2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA, V_{DDQ} = 2.5V			0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 2.5V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Identification Register Definitions

Instruction Field	CY7C1354DV25	CY7C1356DV25	Description
Revision Number (31:29)	000	000	Reserved for version number.
Cypress Device ID (28:12)	01011001000100110	01011001000010110	Reserved for future use.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	Indicate the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (119-Ball BGA Package)	69	69
Boundary Scan Order (165-Ball FBGA Package)	69	69

Note:
12. All voltages referenced to V_{SS} (GND).

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Exit Order (256K × 36)

Bit #	119-Ball ID	165-Ball ID
1	K4	B6
2	H4	B7
3	M4	A7
4	F4	B8
5	B4	A8
6	G4	A9
7	C3	B10
8	B3	A10
9	D6	C11
10	H7	E10
11	G6	F10
12	E6	G10
13	D7	D10
14	E7	D11
15	F6	E11
16	G7	F11
17	H6	G11
18	T7	H11
19	K7	J10
20	L6	K10
21	N6	L10
22	P7	M10
23	N7	J11
24	M6	K11
25	L7	L11
26	K6	M11
27	P6	N11
28	T4	R11
29	A3	R10
30	C5	P10
31	B5	R9
32	A5	P9
33	C6	R8
34	A6	P8
35	P4	R6
36	N4	P6
37	R6	R4
38	T5	P4
39	T3	R3
40	R2	P3
41	R3	R1
42	P2	N1
43	P1	L2
44	L2	K2
45	K1	J2
46	N2	M2

Boundary Scan Exit Order (256K × 36) (continued)

Bit #	119-Ball ID	165-Ball ID
47	N1	M1
48	M2	L1
49	L1	K1
50	K2	J1
51	Not Bonded (Preset to 1)	Not Bonded (Preset to 1)
52	H1	G2
53	G2	F2
54	E2	E2
55	D1	D2
56	H2	G1
57	G1	F1
58	F2	E1
59	E1	D1
60	D2	C1
61	C2	B2
62	A2	A2
63	E4	A3
64	B2	B3
65	L3	B4
66	G3	A4
67	G5	A5
68	L5	B5
69	B6	A6

Boundary Scan Exit Order (512K × 18)

Bit #	119-Ball ID	165-Ball ID
1	K4	B6
2	H4	B7
3	M4	A7
4	F4	B8
5	B4	A8
6	G4	A9
7	C3	B10
8	B3	A10
9	T2	A11
10	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
11	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
12	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
13	D6	C11
14	E7	D11
15	F6	E11
16	G7	F11
17	H6	G11
18	T7	H11
19	K7	J10
20	L6	K10
21	N6	L10
22	P7	M10
23	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
24	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
25	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
26	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
27	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
28	T6	R11
29	A3	R10
30	C5	P10
31	B5	R9
32	A5	P9
33	C6	R8
34	A6	P8
35	P4	R6
36	N4	P6
37	R6	R4
38	T5	P4
39	T3	R3
40	R2	P3
41	R3	R1
42	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)

Boundary Scan Exit Order (512K × 18) (continued)

Bit #	119-Ball ID	165-Ball ID
43	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
44	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
45	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
46	P2	N1
47	N1	M1
48	M2	L1
49	L1	K1
50	K2	J1
51	Not Bonded (Preset to 1)	Not Bonded (Preset to 1)
52	H1	G2
53	G2	F2
54	E2	E2
55	D1	D2
56	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
57	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
58	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
59	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
60	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
61	C2	B2
62	A2	A2
63	E4	A3
64	B2	B3
65	Not Bonded (Preset to 0	Not Bonded (Preset to 0)
66	G3	Not Bonded (Preset to 0)
67	Not Bonded (Preset to 0	A4
68	L5	B5
69	B6	A6
69	B6	A6
69	B6	A6
68	L5	B5
69	B6	A6
66	G3	Not Bonded (Preset to 0)
67	Not Bonded (Preset to 0	A4
68	L5	B5
69	B6	A6

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND .....–0.5V to +3.6V

Supply Voltage on V_{DDQ} Relative to GND..... –0.5V to +V_{DD}

DC to Outputs in Tri-State.....–0.5V to V_{DDQ} + 0.5V

DC Input Voltage .....–0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}/V_{DDQ}
Commercial	0°C to +70°C	2.5V ±5%
Industrial	–40°C to +85°C	

Electrical Characteristics

Over the Operating Range[13, 14]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	I/O Supply Voltage	for 2.5V I/O		2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	for 2.5V I/O, I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	for 2.5V I/O, I_{OL}= 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage	for 2.5V I/O		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[13]	for 2.5V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz		250	mA
			5 ns cycle, 200 MHz		220	mA
			6 ns cycle, 166 MHz		180	mA
I_{SB1}	Automatic CE Power Down Current—TTL Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz		130	mA
			5 ns cycle, 200 MHz		120	mA
			6 ns cycle, 166 MHz		110	mA
I_{SB2}	Automatic CE Power Down Current—CMOS Inputs	Max V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All speed grades		40	mA
I_{SB3}	Automatic CE Power Down Current—CMOS Inputs	Max V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz		120	mA
			5 ns cycle, 200 MHz		110	mA
			6 ns cycle, 166 MHz		100	mA
I_{SB4}	Automatic CE Power Down Current—TTL Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All speed grades		40	mA

Notes

13. Overshoot: $V_{IH}(AC) < V_{DD} + 1.5V$ (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > –2V$ (Pulse width less than $t_{CYC}/2$).
14. $T_{Power\text{-}up}$: Assumes a linear ramp from 0V to V_{DD} (minimum) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.

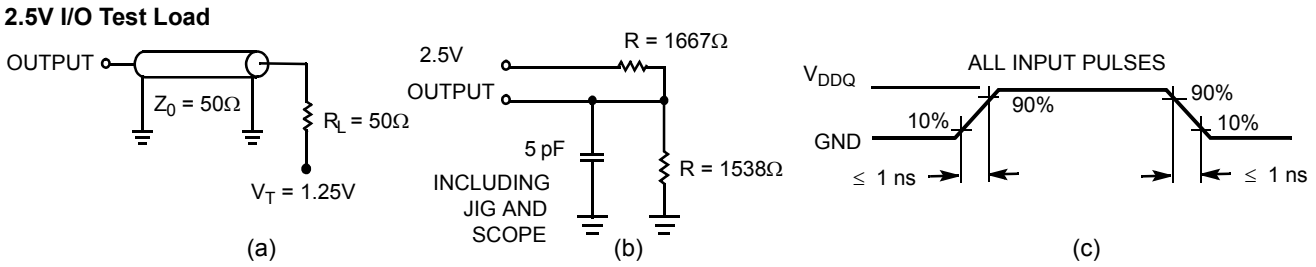
Capacitance[15]

Parameter	Description	Test Conditions	100 TQFP Max	119 BGA Max	165 FBGA Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 2.5V, V_{DDQ} = 2.5V	5	5	5	pF
C_{CLK}	Clock Input Capacitance		5	5	5	pF
$C_{I/O}$	Input/Output Capacitance		5	7	7	pF

Thermal Resistance[15]

Parameters	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	29.41	34.1	16.8	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		6.13	14	3.0	°C/W

Figure 5. AC Test Loads and Waveforms



Note
15. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range [17, 18]

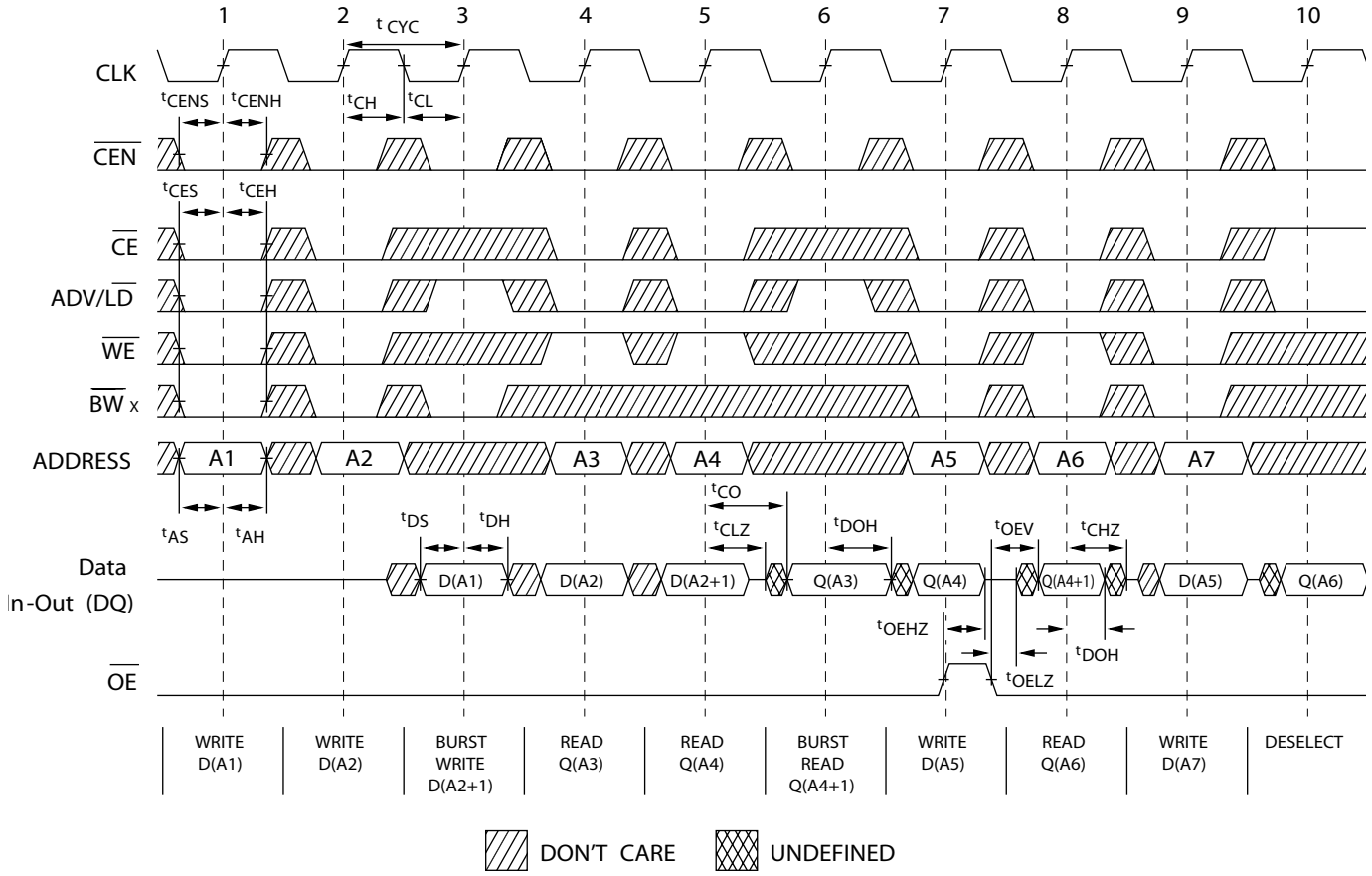
Parameter	Description	–250		–200		–166		Unit
		Min	Max	Min	Max	Min	Max	
t_{Power}[16]	V_{CC} (Typical) to the First Access Read or Write	1		1		1		ms
Clock								
t_{CYC}	Clock Cycle Time	4.0		5		6		ns
F_{MAX}	Maximum Operating Frequency		250		200		166	MHz
t_{CH}	Clock HIGH	1.8		2.0		2.4		ns
t_{CL}	Clock LOW	1.8		2.0		2.4		ns
Output Times								
t_{CO}	Data Output Valid after CLK Rise		2.8		3.2		3.5	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		2.8		3.2		3.5	ns
t_{DOH}	Data Output Hold after CLK Rise	1.25		1.5		1.5		ns
t_{CHZ}	Clock to High-Z[19, 20, 21]	1.25	2.8	1.5	3.2	1.5	3.5	ns
t_{CLZ}	Clock to Low-Z[19, 20, 21]	1.25		1.5		1.5		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[19, 20, 21]		2.8		3.2		3.5	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[19, 20, 21]	0		0		0		ns
Setup Times								
t_{AS}	Address Setup before CLK Rise	1.4		1.5		1.5		ns
t_{DS}	Data Input Setup before CLK Rise	1.4		1.5		1.5		ns
t_{CENS}	$\overline{CEN}$ Setup before CLK Rise	1.4		1.5		1.5		ns
t_{WES}	$\overline{WE}$, $\overline{BW}_x$ Setup before CLK Rise	1.4		1.5		1.5		ns
t_{ALS}	ADV/$\overline{LD}$ Setup before CLK Rise	1.4		1.5		1.5		ns
t_{CES}	Chip Select Setup	1.4		1.5		1.5		ns
Hold Times								
t_{AH}	Address Hold after CLK Rise	0.4		0.5		0.5		ns
t_{DH}	Data Input Hold after CLK Rise	0.4		0.5		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold after CLK Rise	0.4		0.5		0.5		ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_x$ Hold after CLK Rise	0.4		0.5		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.4		0.5		0.5		ns
t_{CEH}	Chip Select Hold after CLK Rise	0.4		0.5		0.5		ns

Notes

16. This part has a voltage regulator internally; t_{power} is the time power needs to be supplied above V_{DD} minimum initially, before a read or write operation can be initiated.
17. Timing reference level is when V_{DDQ} = 2.5V.
18. Test conditions shown in (a) of AC Test Loads unless otherwise noted.
19. t_{CHZ}, t_{CLZ}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
20. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
21. This parameter is sampled and not 100% tested.

Switching Waveforms

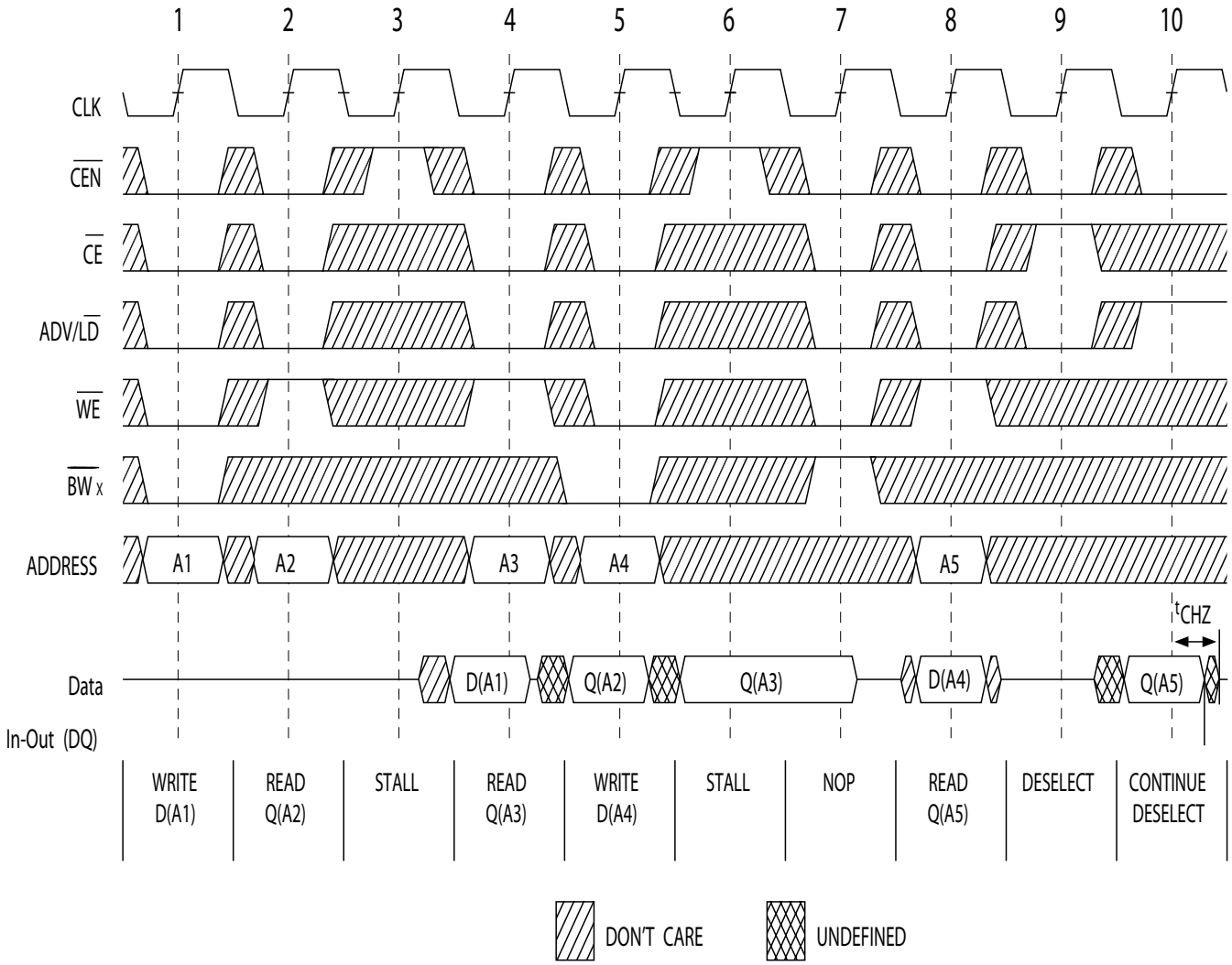
Figure 6. Read/Write Timing[22, 23, 24]



Notes
22. For this waveform ZZ is tied LOW.
23. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
24. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

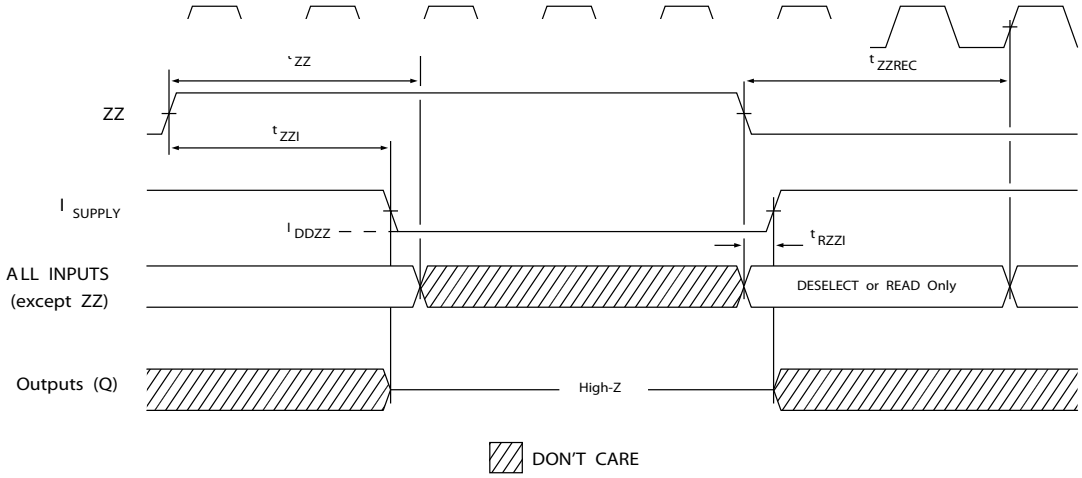
Figure 7. NOP, STALL and DESELECT CYCLES[22, 23, 25]



Note
25. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

Figure 8. ZZ Mode Timing[26, 27]



Notes
26. Device must be deselected when entering ZZ mode. See Write Cycle Description tables for all possible signal conditions to deselect the device.
27. I/Os are in High-Z when exiting ZZ sleep mode.

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.
For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.
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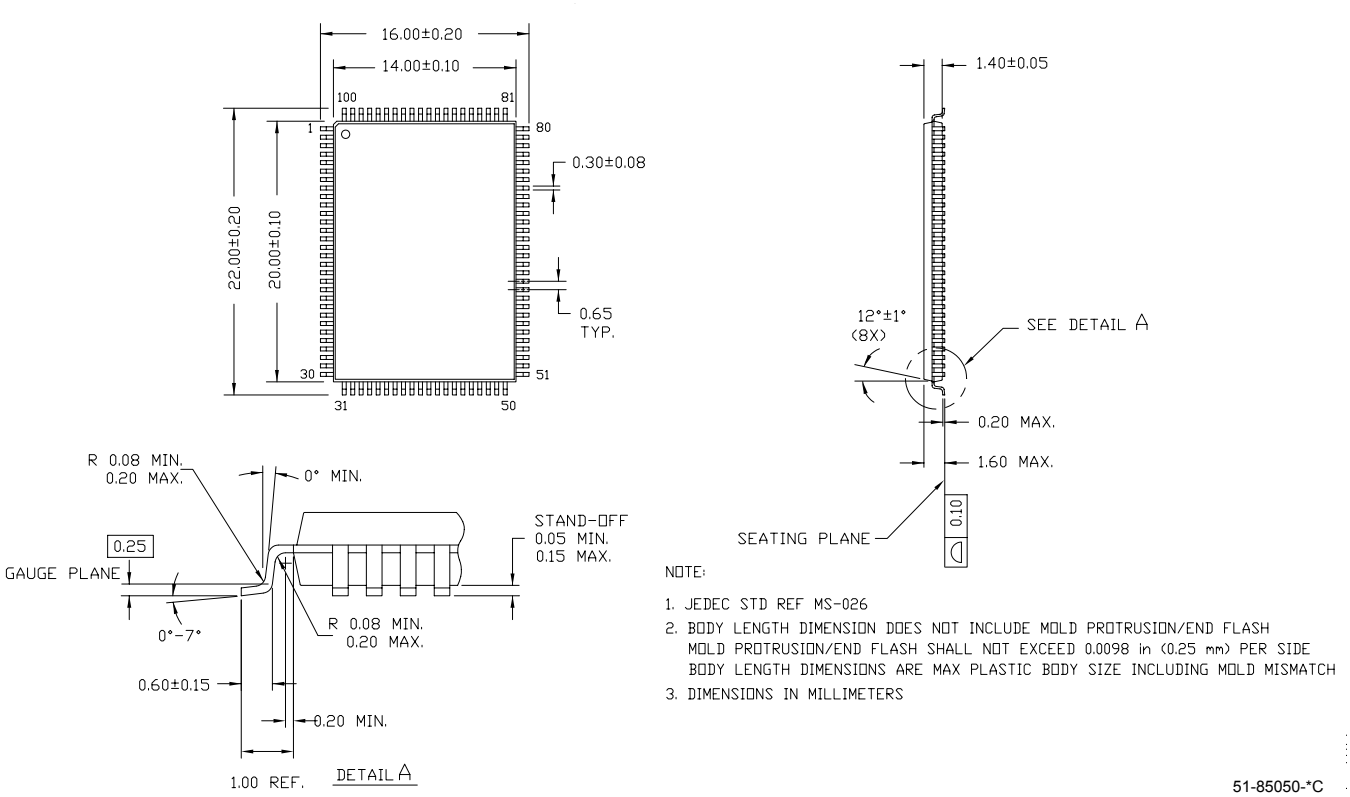
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
200	CY7C1354DV25-200BZI	51-85180	165-Ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	Industrial

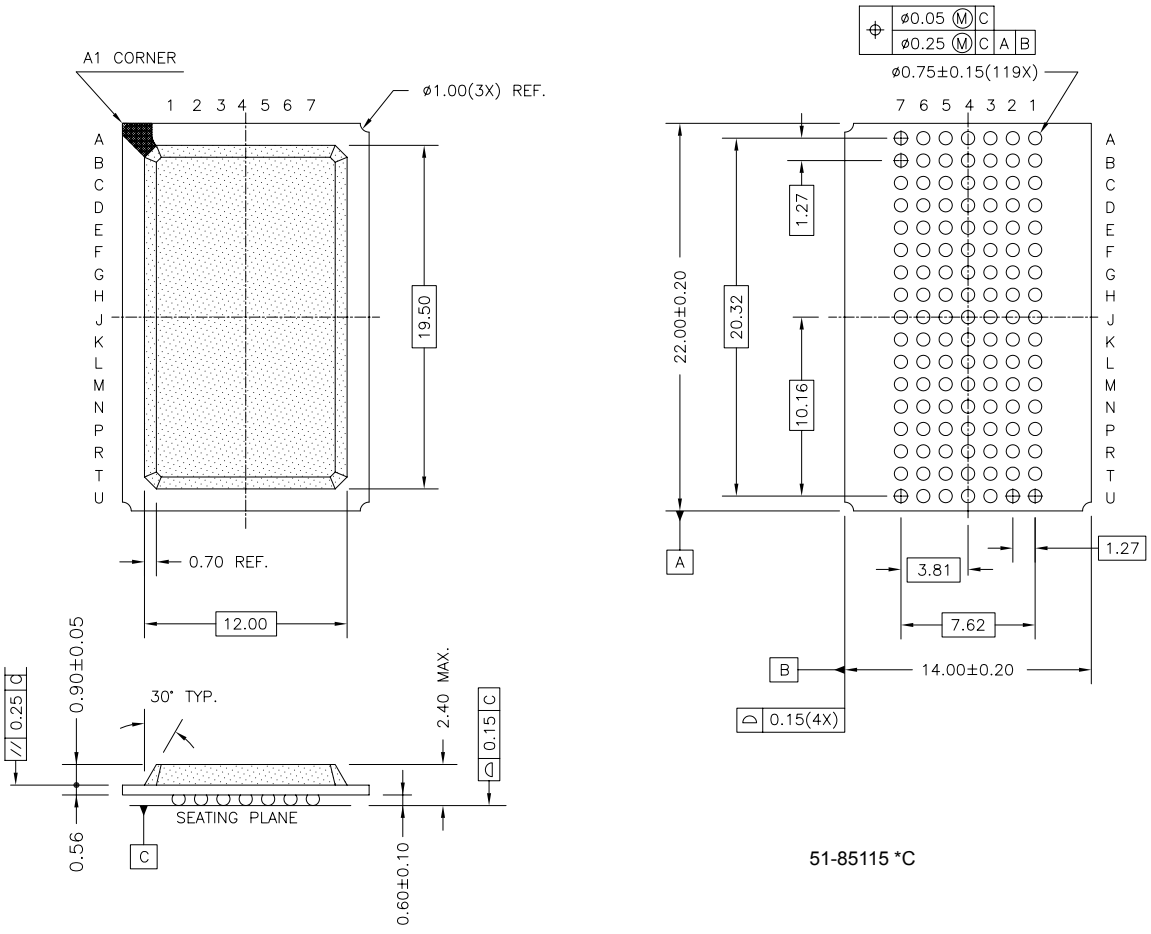
Package Diagrams

Figure 9. 100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) (51-85050)



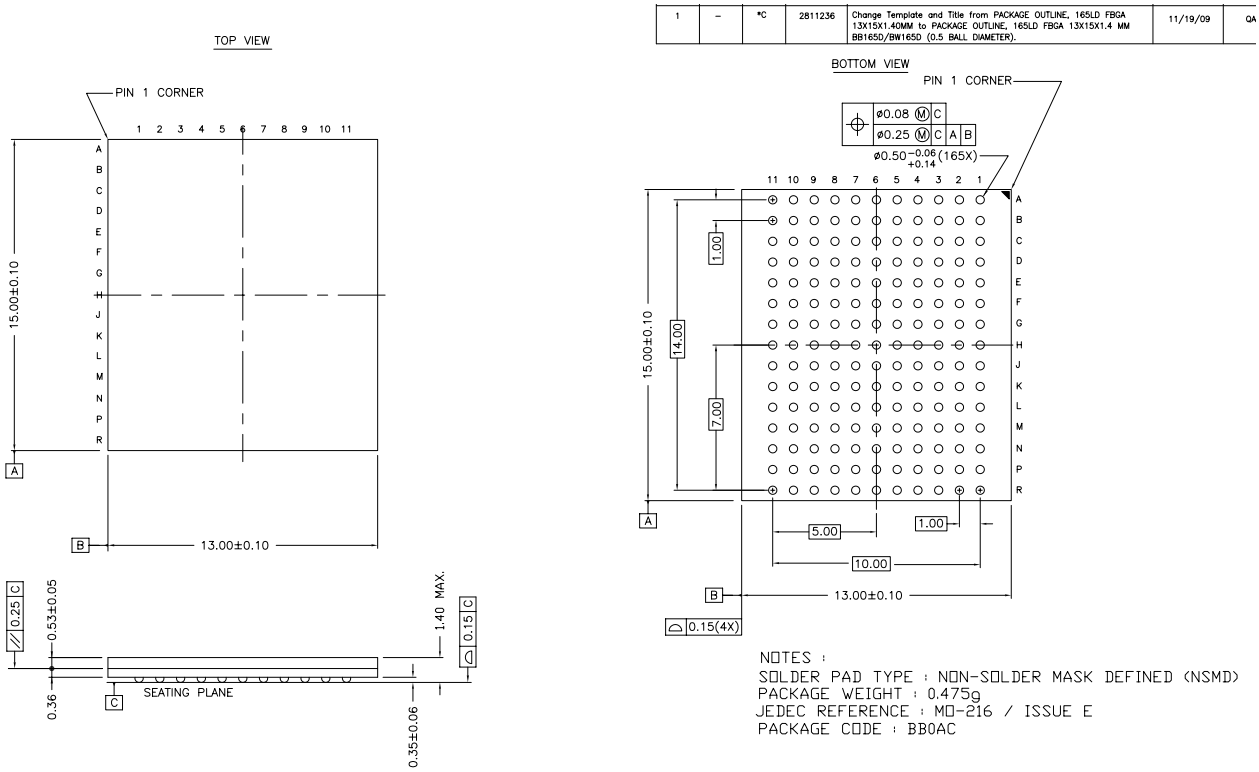
Package Diagrams (continued)

Figure 10. 119-Ball BGA (14 x 22 x 2.4 mm) (51-85115)



Package Diagrams (continued)

Figure 11. 165-Ball FBGA (13 x 15 x 1.4 mm) (51-85180)



Document History Page

Document Title: CY7C1354DV25/CY7C1356DV25, 9-Mbit (256K x 36/512K x 18) Pipelined SRAM with NoBL™ Architecture Document Number: 001-48974				
Rev.	**ECN No.**	**Origin of Change**	**Submission Date**	**Description of Change**
**	2594961	VKN	10/22/08	NSO data sheet for Tellabs
*A	2746930	07/31/09	NJY	Post to external website
*B	2896565	03/20/2010	NJY	Removed obsolete parts from Ordering Information table. Updated package diagram, data sheet template, and Sales, Solutions, and Legal Information section.

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