Rochester Electronics®

Datasheet

CA3310AD

CMOS, 10-Bit, A/D Converters with Internal Track and Hold

The Harris CA3310 is a fast, low power, 10-bit successive approximation analog-to-digital converter, with microprocessor compatible outputs. It uses only a single 3V to 6V supply and typically draws Just 3mA when operating at 5V. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100ns (typical) input time constant.

The ten data outputs feature full high-speed CMOS threestate bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

HARRIS SEMICONDUCTOR

CA3310, CA3310A

CMOS, 10-Bit, A/D Converters with Internal Track and Hold

August 1997

Features

- CMOS Low Power (Typ) 15mW
- Single Supply Voltage . . . . . .3V to 6V
- Conversion Time 13µs
- Built-In Track and Hold
- Rail-to-Rail Input Range
- Latched Three-state Output Drivers
- Microprocessor-Compatible Control Lines
- Internal or External Clock

Applications

- Fast, No-Droop, Sample and Hold
- Voice Grade Digital Audio
- DSP Modems
- Remote Low Power Data Acquisition Systems
- µP Controlled Systems

Description

The Harris CA3310 is a fast, low power, 10-bit successive approximation analog-to-digital converter, with microprocessor-compatible outputs. It uses only a single 3V to 6V supply and typically draws just 3mA when operating at 5V. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100ns (typical) input time constant.

The ten data outputs feature full high-speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

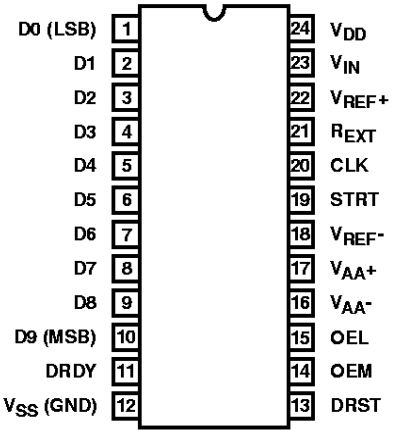
An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3310E	±0.75 LSB	-40 to 85	24 Ld PDIP	E24.6
CA3310AE	±0.5 LSB	-40 to 85	24 Ld PDIP	E24.6
CA3310M	±0.75 LSB	-40 to 85	24 Ld SOIC	M24.3
CA3310AM	±0.5 LSB	-40 to 85	24 Ld SOIC	M24.3
CA3310D	±0.75 LSB	-55 to 125	24 Ld SBDIP	D24.6
CA3310AD	±0.5 LSB	-55 to 125	24 Ld SBDIP	D24.6

Pinout

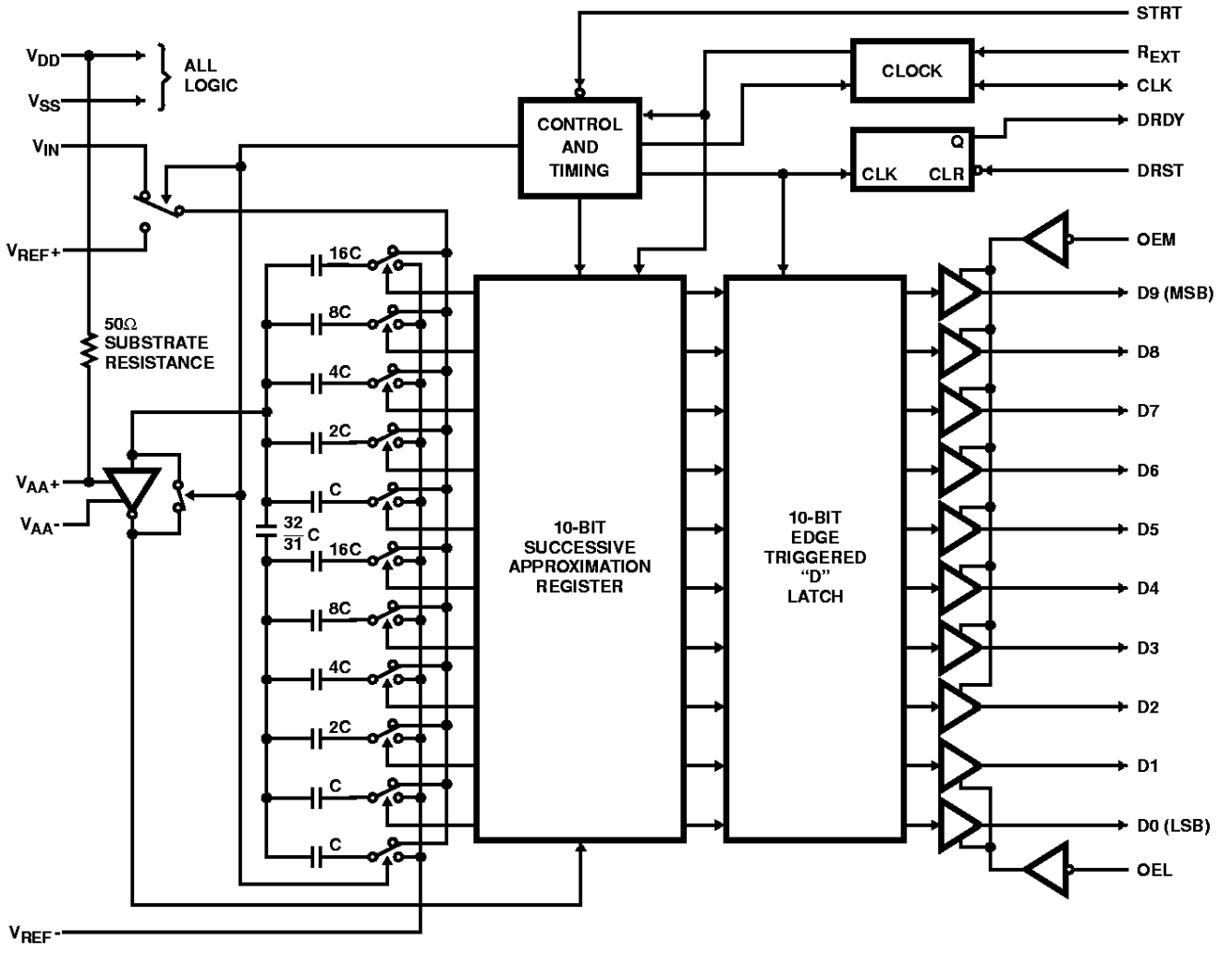
CA3310, CA3310A
(PDIP, SBDIP, SOIC)
TOP VIEW



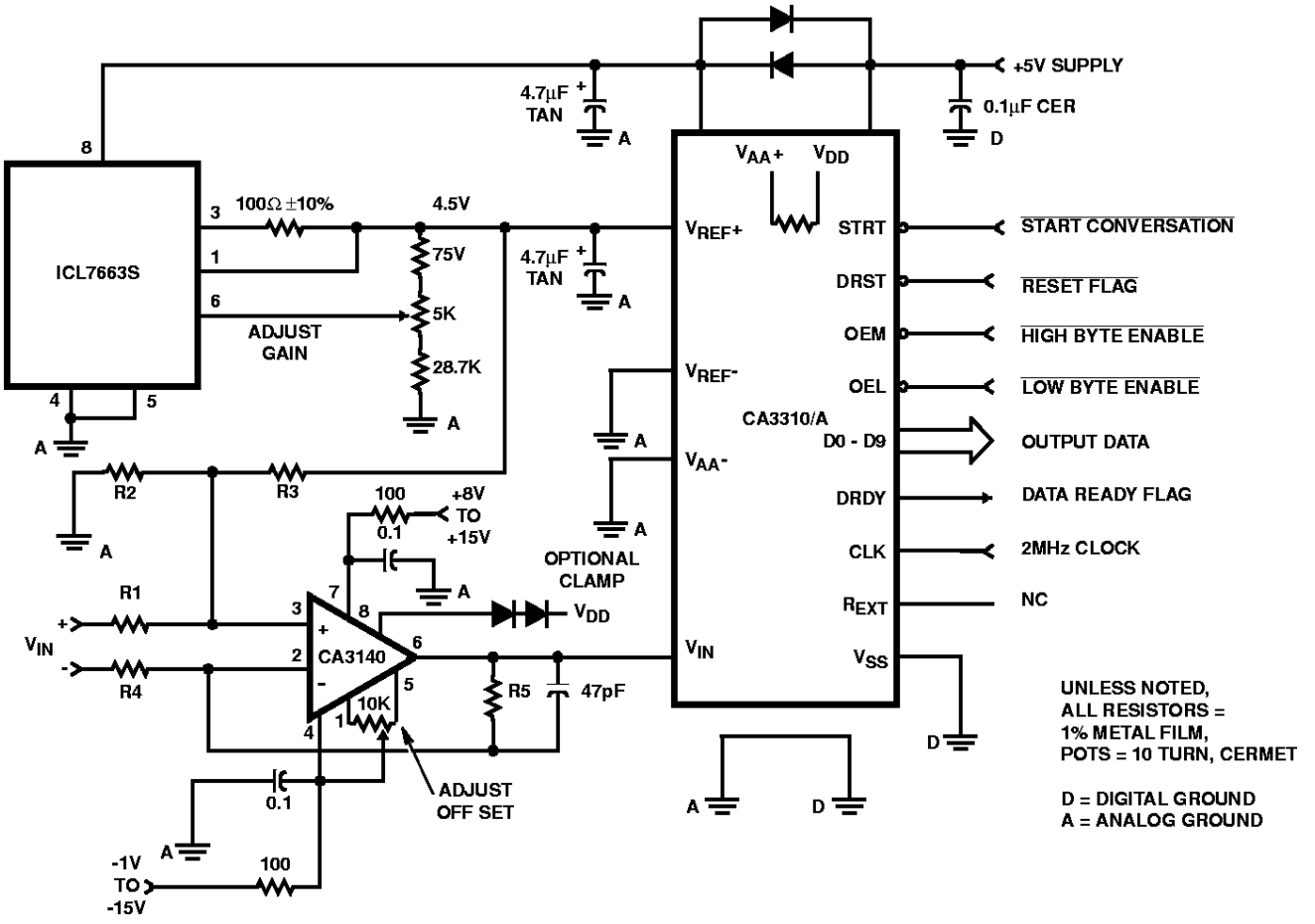
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3095.1**

Functional Block Diagram



Typical Application Schematics



INPUT RANGE	R1	R2	R3	R4	R5
0V TO 2.5V	4.99K	9.09K	OPEN	4.99K	9.09K
0V TO 5V	4.99K	4.53K	OPEN	4.99K	4.53K
0V TO 10V	10K	4.53K	OPEN	10K	4.53K
-2.5V TO +2.5V	4.99K	9.09K	9.09K	4.99K	4.53K
-5V TO +5V	10K	9.09K	9.09K	10K	4.53K

Absolute Maximum Ratings

Digital Supply Voltage V_{DD} . . . . . V_{SS} -0.5V to V_{SS} +7V
Analog Supply Voltage (V_{AA}+) . . . . . V_{DD} ±0.5V
Any Other Terminal . . . . . V_{SS} -0.5V to V_{DD} + 0.5V
DC Input Current or Output (Protection Diode) Current . . . . . ±20mA
DC Output Drain Current, per Output . . . . . ±35mA
Total DC Supply or Ground Current . . . . . ±70mA

Operating Conditions

Temperature Range (T_A)
Package Type D . . . . . -55°C to 125°C
Package Type E, M . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	75	N/A
SBDIP Package	70	22
SOIC Package	75	N/A

Maximum Junction Temperature
Plastic Packages . . . . . 150°C
Hermetic Package . . . . . 175°C
Maximum Storage Temperature (T_{STG}) . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

T_A = 25°C, V_{DD} = V_{AA}+ = 5V, V_{REF}+ = 4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 1MHz, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (See Text For Definitions)						
Resolution			10	-	-	Bits
Differential Linearity Error	CA3310		-	±0.5	±0.75	LSB
	CA3310A		-	±0.25	±0.5	LSB
Integral Linearity Error	CA3310		-	±0.5	±0.75	LSB
	CA3310A		-	±0.25	±0.5	LSB
Gain Error	CA3310		-	±0.25	±0.5	LSB
	CA3310A		-	-	±0.25	LSB
Offset Error	CA3310		-	±0.25	±0.5	LSB
	CA3310A		-	-	±0.25	LSB
ANALOG OUTPUT						
Input Resistance		In Series with Input Sample Capacitors	-	330	-	Ω
Input Capacitance		During Sample State	-	300	-	pF
Input Capacitance		During Hold State	-	20	-	pF
Input Current		At V_{IN} = V_{REF}+ = 5V	-	-	+300	µA
		At V_{IN} = V_{REF}- = 0V	-	-	-100	µA
Static Input Current		STRT = V+, CLK = V+ At V_{IN} = V_{REF}+ = 5V	-	-	1	µA
		At V_{IN} = V_{REF}- = 0V	-	-	-1	µA
Input + Full-Scale Range		(Note 2)	V_{REF}- +1	-	V_{DD} +0.3	V
Input - Full-Scale Range		(Note 2)	V_{SS} -0.3	-	V_{REF}+ -1	V
Input Bandwidth		From Input RC Time Constant	-	1.5	-	MHz
DIGITAL INPUTS DRST, OEL, OEM, STRT, CLK						
High-Level Input Voltage		Over V_{DD} = 3V to 6V (Note 2)	70	-	-	% of V_{DD}
Low-Level Input Voltage		Over V_{DD} = 3V to 6V (Note 2)	-	-	30	% of V_{DD}
Input Leakage Current		Except CLK	-	-	±1	µA
Input Capacitance		(Note 2)	-	-	10	pF
Input Current		CLK Only (Note 2)	-	-	±400	µA

Electrical Specifications $T_A = 25^oC$, $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = 4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 1MHz, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS D0 - D9, DRDY					
High-Level Output Voltage	I_{SOURCE} = -4mA	4.6	-	-	V
Low-Level Output Voltage	I_{SINK} = 6mA	-	-	0.4	V
Three-State Leakage	Except DRDY	-	-	±1	µA
Output Capacitance	Except DRDY (Note 2)	-	-	20	pF
CLK OUTPUT					
High-Level Output Voltage	I_{SOURCE} = 100µA (Note 2)	4	-	-	V
Low-Level Output Voltage	I_{SINK} = 100µA (Note 2)	-	-	1	V
TIMING					
Clock Frequency	Internal, CLK and R_{EXT} Open	200	300	400	kHz
	Internal, CLK Shorted to R_{EXT}	600	800	1000	kHz
	External, Applied to CLK (Note 2) (Max)	-	4	2	MHz
	(Min)	100	10	-	kHz
Clock Pulse Width, t_{LOW}, t_{HIGH}	External, Applied to CLK: See Figure 1 (Note 2)	100	-	-	ns
Conversion Time	Internal, CLK Shorted to R_{EXT}	13	-	-	µs
Aperture Delay, t_D APR	See Figure 1	-	100	-	ns
Clock to Data Ready Delay, t_{D1} DRDY	See Figure 1	-	150	-	ns
Clock to Data Ready Delay, t_{D2} DRDY	See Figure 1	-	250	-	ns
Clock to Data Delay, t_D Data	See Figure 1	-	200	-	ns
Start Removal Time, t_R STRT	See Figures 3 and 4 (Note 1)	-	-120	-	ns
Start Setup Time, t_{SU} STRT	See Figure 4	-	160	-	ns
Start Pulse Width, t_W STRT	See Figures 3 and 4	-	10	-	ns
Start to Data Ready Delay, t_{D3} DRDY	See Figures 3 and 4	-	170	-	ns
Clock Delay from Start, t_D CLK	See Figure 3	-	200	-	ns
Ready Reset Removal Time, t_R DRST	See Figure 50 (Note 1)	-	-80	-	ns
Ready Reset Pulse Width, t_W DRST	See Figure 5	-	10	-	ns
Ready Reset to Data Ready Delay, t_{D4} DRDY	See Figure 5	-	35	-	ns
Output Enable Delay, t_{EN}	See Figure 2	-	40	-	ns
Output Disable Delay, t_{DIS}	See Figure 2	-	50	-	ns
SUPPLIES					
Supply Operating Range, V_{DD} or V_{AA}	(Note 2)	3	-	6	V
Supply Current, $I_{DD} + I_{AA}$	See Figures 14, 15	-	3	8	mA
Supply Standby Current	Clock Stopped During Cycle 1	-	3.5	-	mA
Analog Supply Rejection	At 120Hz, See Figure 13	-	25	-	mV/V
Reference Input Current	See Figure 10	-	160	-	µA
TEMPERATURE DEPENDENCY					
Offset Drift	At 0 to 1 Code Transition	-	-4	-	µV/°C
Gain Drift	At 1022 to 1023 Code Transition	-	-6	-	µV/°C
Internal Clock Speed	See Figure 7	-	-0.5	-	%/°C

NOTES:

1. A (-) removal time means the signal can be removed after the reference signal.
2. Parameter not tested, but guaranteed by design or characterization.