

Rochester Electronics®

CA3310AD

CMOS, 10-Bit, A/D Converters with Internal Track and Hold

The Harris CA3310 is a fast, low power, 10-bit successive approximation analog-to-digital converter, with microprocessor compatible outputs. It uses only a single 3V to 6V supply and typically draws Just 3mA when operating at 5V. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100ns (typical) input time constant.

The ten data outputs feature full high-speed CMOS threestate bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

Rochester Electronics Manufactured Components	Quality Overview ISO-9001
Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM)	 AS9120 certification Qualified Manufacturers List (QML) MIL-PRF-35835 Class Q Military Class V Space Level Qualified Suppliers List of Distributors (QSLD) Rochester is a critical supplier to DLA and meets all industry and DLA standards.
Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.	Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY



CA3310, CA3310A

CMOS, 10-Bit, A/D Converters with Internal Track and Hold

August 1997

Features

- CMOS Low Power (Typ).....15mW
- Conversion Time13
 s
- Built-In Track and Hold
- Rail-to-Rail Input Range
- Latched Three-state Output Drivers
- Microprocessor-Compatible Control Lines
- Internal or External Clock

Applications

- Fast, No-Droop, Sample and Hold
- Voice Grade Digital Audio
- DSP Modems
- Remote Low Power Data Acquisition Systems
- µP Controlled Systems

Description

The Harris CA3310 is a fast, low power, 10-bit successive approximation analog-to-digital converter, with microprocessorcompatible outputs. It uses only a single 3V to 6V supply and typically draws just 3mA when operating at 5V. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100ns (typical) input time constant.

The ten data outputs feature full high-speed CMOS threestate bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (⁰ C)	PACKAGE	PKG. NO.
CA3310E	±0.75 LSB	-40 to 85	24 Ld PDIP	E24.6
CA3310AE	±0.5 LSB	-40 to 85	24 Ld PDIP	E24.6
CA3310M	±0.75 LSB	-40 to 85	24 Ld SOIC	M24.3
CA3310AM	\pm 0.5 LSB	-40 to 85	24 Ld SOIC	M24.3
CA3310D	±0.75 LSB	-55 to 125	24 Ld SBDIP	D24.6
CA3310AD	±0.5 LSB	-55 to 125	24 Ld SBDIP	D24.6



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures. Copyright © Harris Corporation 1997

Pinout





INPUT RANGE	R1	R2	R3	R4	R5
0V TO 2.5V	4.99K	9.09K	OPEN	4.99K	9.09K
0V TO 5V	4.99K	4.53K	OPEN	4.99K	4.53K
0V TO 10V	10K	4.53K	OPEN	10K	4.53K
-2.5V TO +2.5V	4.99K	9.09K	9.09K	4.99K	4.53K
-5V TO +5V	10K	9.09K	9.09K	10K	4.53K

Absolute Maximum Ratings

Digital Supply Voltage V _{DD}	.V _{SS} -0.5V to V _{SS} +7V
Analog Supply Voltage (V _{AA} +)	V _{DD} ±0.5V
Any Other Terminal	_{SS} -0.5V to V _{DD} + 0.5V
DC Input Current or Output (Protection Diode	e)
Current	±20mA
DC Output Drain Current, per Output	±35mA
Total DC Supply or Ground Current	±70mA

Operating Conditions

Temperature Range (T _A)	
Package Type D	
Package Type E, M	

Thermal Information

Thermal Resistance (Typical, Note 1)	θ _{JA} (^o C/W)	θ _{JC} (^o C/W)
PDIP Package	. 75	N/A
SBDIP Package	. 70	22
SOIC Package	. 75	N/A
Maximum Junction Temperature		
Plastic Packages		150 ⁰ C
Hermetic Package		175 ^o C
Maximum Storage Temperature (T _{STG})	6	5°C to 150°C
Maximum Lead Temperature (Soldering 1 (SOIC - Lead Tips Only)	0s)	300°C
(

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

 $\label{eq:Electrical Specifications} \textbf{T}_{A} = 25^{\circ} \textbf{C}, \ \textbf{V}_{DD} = \textbf{V}_{AA^+} = 5 \textbf{V}, \ \textbf{V}_{REF^+} = 4.608 \textbf{V}, \ \textbf{V}_{SS} = \textbf{V}_{AA^-} = \textbf{V}_{REF^-} = \textbf{GND}, \ \textbf{CLK} = \textbf{External 1MHz}, \ \textbf{CLK} = \textbf{L}_{AA^+} = \textbf{V}_{AA^+} = \textbf{V}_{A$

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

	Uniess	Otherwise Specified				
PARAMETER	3	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (See Text For	⁻ Definitions)					
Resolution			10	-	-	Bits
Differential Linearity Error	CA3310		-	±0.5	±0.75	LSB
	CA3310A		-	±0.25	±0.5	LSB
Integral Linearity Error	CA3310		-	±0.5	±0.75	LSB
	CA3310A		-	±0.25	±0.5	LSB
Gain Error	CA3310		-	±0.25	±0.5	LSB
	CA3310A		-	-	±0.25	LSB
Offset Error	CA3310		-	±0.25	±0.5	LSB
	CA3310A		-	-	±0.25	LSB
ANALOG OUTPUT		-				
Input Resistance		In Series with Input Sample Capacitors		330	-	Ω
Input Capacitance		During Sample State	-	300	-	pF
Input Capacitance		During Hold State	-	20	-	pF
Input Current		At V _{IN} = V _{REF} + = 5V	-	-	+300	μA
		At V _{IN} = V _{REF} - = 0V	-	-	-100	μΑ
Static Input Current		STRT = V+, CLK = V+ At V _{IN} = V _{REF} + = 5V	-	-	1	μΑ
		At V _{IN} = V _{REF} - = 0V	-	-	-1	μΑ
Input + Full-Scale Range		(Note 2)	V _{REF} - +1	-	V _{DD} +0.3	V
Input - Full-Scale Range		(Note 2)	V _{SS} -0.3	-	V _{REF} +-1	V
Input Bandwidth		From Input RC Time Constant	-	1.5	-	MHz
DIGITAL INPUTS DRST, C	DEL, OEM, STI	RT, CLK				
High-Level Input Voltage		Over V _{DD} = 3V to 6V (Note 2)	70	-	-	% of V _{DD}
Low-Level Input Voltage		Over V _{DD} = 3V to 6V (Note 2)	-	-	30	% of V _{DD}
Input Leakage Current		Except CLK	-	-	±1	μA
Input Capacitance		(Note 2)	-	-	10	pF
Input Current		CLK Only (Note 2)	-	-	±400	μA

Electrical Specifications

 $T_A = 25^{o}C, V_{DD} = V_{AA} + = 5V, V_{REF} + = 4.608V, V_{SS} = V_{AA^-} = V_{REF^-} = GND, CLK = External 1MHz, Unless Otherwise Specified (Continued)$

DIGITAL OUTPLITS D0D9, DRDY High-Level Output Voltage IgoNR = 8mA 4.6 . . V Low-Level Output Voltage IgoNR = 8mA . . 0.4 V Three-State Leakage Except DRDY . . 20 pF CLK OUTPUT V High-Level Output Voltage Isource = 109µA (Note 2) V CLK OUTPUT V Low-Level Output Voltage Isource = 109µA (Note 2) V TIMMO MHz Clock Frequency Internal. CLK Shorted to R _{EXT} </th <th>PARAMETER</th> <th>TEST CONDITIONS</th> <th>MIN</th> <th>ТҮР</th> <th>MAX</th> <th>UNITS</th>	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS
High-Level Output Voltage Isource = ·4mA 4.6 · · V Low-Level Output Voltage Isink = 6mA · · 0.4 V Durbut Capacitance Except DRDY · · 0.4 V Output Capacitance Except DRDY (Note 2) · · 200 pF CLK OUTPUT - · 1 V V V Low-Level Output Voltage Isource 100µA (Note 2) · · V V Concervel Output Voltage Isource 100µA (Note 2) · · V V Conv-Level Output Voltage Isource 100µA (Note 2) · · · V Clock Firequency Internal, CLK Shorded to REXT 1000 100 · RHz Clock Pulse Width, ILOW, It-IGH External, Applied to CLK: See Figure 1 1000 · Itera Itera Clock to Data Ready Delay, Itera See Figure 1 · 100 · ns Clock to Data Ready Delay, Itera See Figure 3 · </td <td>DIGITAL OUTPUTS D0 - D9, DRDY</td> <td></td> <td></td> <td></td> <td></td> <td>-</td>	DIGITAL OUTPUTS D0 - D9, DRDY					-
Low-Level Output Voltage ISINK = 6mA · · 0.4 V Trinee-State Leakage Except DRDV · · 1 µA Output Capacitance Except DRDV (Note 2) · · 20 pF CLK OUTPUT Isource = 100µA (Note 2) · · 1 V High-Level Output Voltage Isource = 100µA (Note 2) · · 1 V Low-Level Output Voltage Isource = 100µA (Note 2) · · 1 V Ide -Level Output Voltage Isource = 100µA (Note 2) · · 1 V Timmos Internal, CLK Shorted to R _{EXT} 600 800 1000 kHz Clock Frequency Internal, Applied to CLK (Note 2) Min 100 · ms Clock Pulse Width, t _{LOW} , t _{HIGH} External, Applied to CLK (Note 2) 100 · ms Clock Data Ready Delay, t _{DD} DRDY See Figure 1 · 100 · ms Clock Data Ready Delay, t _{DD} DRDY See Figure 3 ·	High-Level Output Voltage	I _{SOURCE} = -4mA	4.6	-	-	V
Three-Slate Leakage Except DRDY · · ±1 μA Output Capacitance Except DRDY (Note 2) · · 20 pF CLK OUTPUT High-Level Output Voltage Isource = 100µA (Note 2) 4 · · V Low-Level Output Voltage Isource = 100µA (Note 2) · · 1 V TIMINO - Internal, CLK and R _{EXT} Open 200 300 4000 KHz Clock Frequency Internal, CLK Shorted to R _{EXT} 600 8000 1000 KHz Clock Pulse Width, t _{LOW} , t _{HIGH} External, Applied to CLK: See Figure 1 (Nole 2) 100 · µA Conversion Time Internal, CLK Shorted to R _{EXT} 13 · · µs Aperture Delay, t _D APR See Figure 1 · 150 · ns Clock to Data Ready Delay, t _{DD} DRDY See Figure 1 · 150 · ns Start Bemonal Time, t _R STRT See Figure 3 and 4 (Note 1) · 160 · ns St	Low-Level Output Voltage	I _{SINK} = 6mA	-	-	0.4	V
Oulput Capacitance Except DRDY (Note 2) · · 20 pF CLK OUTPUT	Three-State Leakage	Except DRDY	-	-	±1	μΑ
CLK OUTPUT ISOURCE = 100µA (Note 2) 4 - - V High-Level Output Voltage I _{SNK} = 100µA (Note 2) - - 1 V Low-Level Output Voltage Internal, CLK and R _{EXT} Open 200 300 400 kHz Clock Frequency Internal, CLK Shorted to R _{EXT} 600 800 1000 kHz External, Applied to CLK (Note 2) (Max) - 4 2 MHz Clock Pulse Width, t _L OW, t _{HIGH} External, Applied to CLK: 100 10 - ikHz Conversion Time Internal, CLK Shorted to R _{EXT} 13 - - ms Aperture Delay, tp APR See Figure 1 - 100 - ns Clock to Data Ready Delay, tp_DRDV See Figure 1 - 200 - ns Start Renoval Time, t _B STRT See Figure 3 - 100 - ns Start Renoval Time, t _B STRT See Figure 3 - 100 - ns Start Renoval Time, t _B STRT See Figure	Output Capacitance	Except DRDY (Note 2)	-	-	20	рF
High-Level Output Voltage I _{SOURCE} = 100µA (Note 2) 4 . . V Low-Level Output Voltage I _{SINK} = 100µA (Note 2) . . 1 V TIMING Internal, CLK and R _{EXT} Open 200 300 400 KHz Internal, CLK Shorted to R _{EXT} 600 800 1000 KHz External, Applied to CLK (Note 2) . . 4 2 MHz Clock Pulse Width, t _L OW, t _{HIGH} External, Applied to CLK: See Figure 1 (Note 2) . <td>CLK OUTPUT</td> <td>•</td> <td></td> <td></td> <td></td> <td>•</td>	CLK OUTPUT	•				•
Low-Level Output Vollage IsiNK = 100 μA (Note 2) · · I V TIMING Internal, CLK and R _{EXT} Open 200 300 400 kHz Clock Frequency Internal, CLK shorted to R _{EXT} 600 800 10000 kHz Clock Pulse Width, t _{LOW} , t _{HIGH} External, Applied to CLK: (Min) 0 · 4 2 MHz Clock Pulse Width, t _{LOW} , t _{HIGH} External, Applied to CLK: (Min) 100 · . <td>High-Level Output Voltage</td> <td>I_{SOURCE} = 100μA (Note 2)</td> <td>4</td> <td>-</td> <td>-</td> <td>V</td>	High-Level Output Voltage	I _{SOURCE} = 100μA (Note 2)	4	-	-	V
TMING Internal, CLK and R _{EXT} Open 200 300 400 KHz Clock Frequency Internal, CLK Shorted to R _{EXT} 600 800 1000 kHz External, Applied to CLK (Note 2) (Max) - 4 2 MHz Clock Pulse Width, t _{LOW} , t _{HIGH} External, Applied to CLK (Note 2) (Max) - 4 2 MHz Conversion Time Internal, CLK Shorted to R _{EXT} 100 - . ms Conversion Time Internal, CLK Shorted to R _{EXT} 13 - .	Low-Level Output Voltage	I _{SINK} = 100μA (Note 2)	-	-	1	V
	TIMING	•				•
Internal, CLK Shorted to R _{EXT} 600 800 1000 kHz External, Applied to CLK (Note 2) (Max) - 4 2 MHz (Min) 100 10 - kHz (Min) 100 10 - kHz Clock Pulse Width, t _{LOW} , t _{HIGH} External, Applied to CLK: See Figure 1 (Note 2) 100 - - ms Conversion Time Internal, CLK Shorted to R _{EXT} 13 - - µs Aperture Delay, to APR See Figure 1 - 100 - ns Clock to Data Ready Delay, to DRDY See Figure 1 - 250 - ns Clock to Data Delay, to DAT See Figure 1 - 200 - ns Start Removal Time, tg STRT See Figure 3 and 4 - 160 - ns Start Data Ready Delay, tog DRDY See Figure 3 - 170 - ns Start Setup Time, tg STRT See Figure 5 - 100 - ns Clock Delay	Clock Frequency	Internal, CLK and R _{EXT} Open	200	300	400	kHz
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		Internal, CLK Shorted to R _{EXT}	600	800	1000	kHz
(Min)10010-kHzClock Pulse Width, t_{LOW} , t_{HIGH} External, Applied to CLK: See Figure 1 (Note 2)100nsConversion TimeInternal, CLK Shorted to R_{EXT} 13 μ sAperture Delay, $t_D APR$ See Figure 1-100-nsClock to Data Ready Delay, $t_D IDRDY$ See Figure 1-150-nsClock to Data Delay, $t_D DRDY$ See Figure 1-250-nsClock to Data Delay, $t_D DRDY$ See Figure 1-120-nsStart Removal Time, $t_R STRT$ See Figure 3 and 4 (Note 1)-120-nsStart Setup Time, $t_R STRT$ See Figure 3 and 4-100-nsStart o Data Ready Delay, $t_D DRDY$ See Figure 5 and 4-100-nsStart Setup Time, $t_R STRT$ See Figure 5 and 4-100-nsStart to Data Ready Delay, $t_D DRDY$ See Figure 50 (Note 1)40-nsReady Reset Removal Time, $t_R DRST$ See Figure 50 (Note 1)-35-nsReady Reset Pulse Width, $t_W DRST$ See Figure 5-35-nsReady Reset Pulse Width, $t_D DST$ See Figure 5-40-nsReady Reset Data Ready Delay, $t_D DRY$ See Figure 5-35-nsReady Reset Pulse Width, $t_D DST$ See Figure 5-30-nsReady Reset P		External, Applied to CLK (Note 2) (Max)	-	4	2	MHz
Clock Pulse Width, t _{LOW} , t _{HIGH} External, Applied to CLK: See Figure 1 (Note 2) 100 . . ns Conversion Time Internal, CLK Shorted to R _{EXT} 13 . . . μs Aperture Delay, t _D APR See Figure 1 . 100 . ns Clock to Data Ready Delay, t _D DRDY See Figure 1 . 150 . ns Clock to Data Ready Delay, t _D DRDY See Figure 1 . 250 . ns Clock to Data Ready Delay, t _D DRDY See Figure 1 . 250 . ns Start Setup Time, t _R STRT See Figure 3 and 4 (Note 1) ns Start Setup Time, t _R STRT See Figure 3 and 4 . 100 . ns Start Data Ready Delay, t _D DBDY See Figure 50 (Note 1) ns Ready Reset Neroval Time, t _R DRST See Figure 50 (Note 1) 		(Min)	100	10	-	kHz
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Clock Pulse Width, t _{LOW} , t _{HIGH}	External, Applied to CLK: See Figure 1 (Note 2)	100	-	-	ns
Aperture Delay, t _D ΔPR See Figure 1 . 100 . ns Clock to Data Ready Delay, t _{D1} DRDY See Figure 1 . 150 . ns Clock to Data Ready Delay, t _{D2} DRDY See Figure 1 . 250 . ns Clock to Data Delay, t _{D2} DRDY See Figure 1 . 250 . ns Start Removal Time, t _R STRT See Figure 3 and 4 (Note 1) . . 120 . ns Start Setup Time, t _R STRT See Figure 3 and 4 (Note 1) . . 100 . ns Start Data Ready Delay, t _{D3} DRDY See Figure 3 and 4 . . 100 . ns Start Data Ready Delay, t _{D3} DRDY See Figure 3 . 200 . ns Start Data Ready Delay, t _{D3} DRDY See Figure 5 . . 100 . ns Clock Delay from Start, t _D CLK See Figure 5 Ready Reset Pulse Width, t _W DRST See Figure 5 <	Conversion Time	Internal, CLK Shorted to R _{EXT}	13	-	-	μs
Clock to Data Ready Delay, t_{D1} DRDYSee Figure 1.150.nsClock to Data Ready Delay, t_{D2} DRDYSee Figure 1.250.nsClock to Data Delay, t_{D} DataSee Figure 1.200.nsStart Removal Time, t_{R} STRTSee Figure 3 and 4 (Note 1)120.nsStart Setup Time, t_{SU} STRTSee Figure 3 and 4 (Note 1)120.nsStart Setup Time, t_{SU} STRTSee Figure 3 and 4.10.nsStart To Data Ready Delay, t_{D3} DRDYSee Figure 3 and 4nsClock to Data Ready Delay, t_{D3} DRDYSee Figure 3 and 4nsStart to Data Ready Delay, t_{D3} DRDYSee Figure 3 and 4nsReady Reset Pulse Width, t_W STRTSee Figure 3 and 4Ready Reset Removal Time, t_R DRSTSee Figure 3 <td< td=""><td>Aperture Delay, t_D APR</td><td>See Figure 1</td><td>-</td><td>100</td><td>-</td><td>ns</td></td<>	Aperture Delay, t _D APR	See Figure 1	-	100	-	ns
Clock to Data Ready Delay, t _{D2} DRDY See Figure 1 - 250 - ns Clock to Data Delay, t _D Data See Figure 1 - 200 - ns Start Removal Time, t _R STRT See Figure 3 and 4 (Note 1) - -120 - ns Start Setup Time, t _{SU} STRT See Figure 3 and 4 (Note 1) - 160 - ns Start Setup Time, t _{SU} STRT See Figures 3 and 4 - 10 - ns Start Duts Ready Delay, t _{D3} DRDY See Figures 3 and 4 - 170 - ns Clock Delay from Start, t _D CLK See Figure 3 - 200 - ns Ready Reset Removal Time, t _R DRST See Figure 50 (Note 1) - -80 - ns Ready Reset Pulse Width, t _W DRST See Figure 5 - 10 - ns Ready Reset to Data Ready Delay, t _{EN} See Figure 2 - 40 - ns Output Disable Delay, t _{EN} See Figure 14, 15 - 3 8 mA Supply Qp	Clock to Data Ready Delay, t _{D1} DRDY	See Figure 1	-	150	-	ns
Clock to Data Delay, to DataSee Figure 1-200-nsStart Removal Time, t _R STRTSee Figures 3 and 4 (Note 1)120-nsStart Setup Time, t _{SU} STRTSee Figures 3 and 4-160-nsStart Pulse Width, t _W STRTSee Figures 3 and 4-10-nsStart to Data Ready Delay, t _{D3} DRDYSee Figures 3 and 4-100-nsClock Delay from Start, t _D CLKSee Figure 3-200-nsReady Reset Removal Time, t _R DRSTSee Figure 50 (Note 1)80-nsReady Reset Pulse Width, t _W DRSTSee Figure 5-10-nsReady Reset to Data Ready Delay, top DRDYSee Figure 5-10-nsOutput Enable Delay, t _{EN} See Figure 2-40-nsSupPUPLIESSupply Operating Range, V _{DD} or V _{AA} (Note 2)3-6VSupply Standby CurrentClock Stopped During Cycle 1-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-25-mV/VReference Input CurrentSee Figure 10-160- μA TEMPERATURE DEPENDENCYOffset DriftAt 0 to 1 Code Transition-4- $\mu V/^0 C$ Gain DriftAt 1022 to 1023 Code Transition6- $\mu V/^0 C$ Internal Clock SpeedSee Figure 75.5 </td <td>Clock to Data Ready Delay, t_{D2} DRDY</td> <td>See Figure 1</td> <td>-</td> <td>250</td> <td>-</td> <td>ns</td>	Clock to Data Ready Delay, t _{D2} DRDY	See Figure 1	-	250	-	ns
Start Removal Time, $t_R STRT$ See Figures 3 and 4 (Note 1)120-nsStart Setup Time, $t_{SU} STRT$ See Figure 4-160-nsStart Pulse Width, $t_W STRT$ See Figures 3 and 4-10-nsStart Data Ready Delay, $t_{D3} DRDY$ See Figures 3 and 4-170-nsClock Delay from Start, $t_D CLK$ See Figure 3-200-nsReady Reset Removal Time, $t_R DRST$ See Figure 50 (Note 1)80-nsReady Reset Pulse Width, $t_W DRST$ See Figure 50 (Note 1)80-nsReady Reset Data Ready Delay, $t_D DRY$ See Figure 5-10-nsReady Reset to Data Ready Delay, $t_D DRY$ See Figure 5-10-nsOutput Enable Delay, t_EN See Figure 2-40-nsOutput Disable Delay, t_{DS} See Figure 2-50-nsSUPPLIESSupply Operating Range, V_{DD} or V_{AA} (Note 2)3-6VSupply Standby CurrentClock Stopped During Cycle 1-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-25-mV/VReference Input CurrentSee Figure 10-160- $\mu A^{V/C}$ Gain DriftAt 0 to 1 Code Transition4- $\mu V/^PC$ Gain DriftAt 1022 to 1023 Code Transition-6- $\mu V/^$	Clock to Data Delay, t _D Data	See Figure 1	-	200	-	ns
Start Setup Time, t_{SU} STRTSee Figure 4-160-nsStart Pulse Width, t_W STRTSee Figures 3 and 4-10-nsStart to Data Ready Delay, t_{D3} DRDYSee Figures 3 and 4-170-nsClock Delay from Start, t_D CLKSee Figure 3-200-nsReady Reset Removal Time, t_R DRSTSee Figure 50 (Note 1)80-nsReady Reset Pulse Width, t_W DRSTSee Figure 50 (Note 1)80-nsReady Reset Data Ready Delay, t_D4 DRDYSee Figure 5-10-nsOutput Enable Delay, t_{EN} See Figure 2-440-nsOutput Disable Delay, t_{DS} See Figure 2-50-nsSUPPLIESSupply Operating Range, V_{DD} or V_{AA} (Note 2)3-6VSupply Standby CurrentClock Stopped During Cycle 1-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-225-mV/VReference Input CurrentSee Figure 10-160- μA TEMPERATURE DEPENDENCYOto 1 Code Transition4- $\mu V/^{0}C$ Gain DriftAt 0 to 1 Code Transition6- $\mu V/^{0}C$ Internal Clock SpeedSee Figure 70.5-%/^0C	Start Removal Time, t _R STRT	See Figures 3 and 4 (Note 1)	-	-120	-	ns
Start Pulse Width, tw STRTSee Figures 3 and 4-10-nsStart to Data Ready Delay, tog DRDYSee Figures 3 and 4-170-nsClock Delay from Start, to CLKSee Figure 3-200-nsReady Reset Removal Time, tn DRSTSee Figure 50 (Note 1)80-nsReady Reset Pulse Width, tw DRSTSee Figure 5-10-nsReady Reset to Data Ready Delay, tog DRDYSee Figure 5-10-nsOutput Enable Delay, tenSee Figure 2-40-nsOutput Enable Delay, tenSee Figure 2-50-nsSupply Operating Range, VDD or VAA(Note 2)3-6VSupply Qurrent, IDD + IAASee Figure 14, 15-38mASupply Standby CurrentClock Stopped During Cycle 1-160- μA Analog Supply RejectionAt 120Hz, See Figure 13-160- μA TEMPERATURE DEPENDENCYOffset DriftAt 0 to 1 Code Transition4- $\mu V/^{\circ}C$ Gain DriftAt 1022 to 1023 Code Transition6- $\mu V/^{\circ}C$	Start Setup Time, t _{SU} STRT	See Figure 4	-	160	-	ns
Start to Data Ready Delay, t_{D3} DRDYSee Figures 3 and 4-170-nsClock Delay from Start, t_D CLKSee Figure 3-200-nsReady Reset Removal Time, t_R DRSTSee Figure 50 (Note 1)80-nsReady Reset Pulse Width, t_W DRSTSee Figure 5-10-nsReady Reset to Data Ready Delay, t_{D4} DRDYSee Figure 5-35-nsOutput Enable Delay, t_{EN} See Figure 2-40-nsOutput Enable Delay, t_{DS} See Figure 2-50-nsSupply Operating Range, V_{DD} or V_{AA} (Note 2)3-6VSupply Current, $l_{DD} + l_{AA}$ See Figure 13-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-160- μA TEMPERATURE DEPENDENCYOt to 1 Code Transition4 $\mu V/^{oC}$ Gain DriftAt 1022 to 1023 Code Transition6 $\mu V/^{oC}$	Start Pulse Width, t _W STRT	See Figures 3 and 4	-	10	-	ns
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Start to Data Ready Delay, t _{D3} DRDY	See Figures 3 and 4	-	170	-	ns
Ready Reset Removal Time, t _R DRSTSee Figure 50 (Note 1)80-nsReady Reset Pulse Width, t _W DRSTSee Figure 5-10-nsReady Reset to Data Ready Delay, t _{D4} DRDYSee Figure 5-35-nsOutput Enable Delay, t _{EN} See Figure 2-40-nsOutput Disable Delay, t _{EN} See Figure 2-50-nsSUPPLIESSupply Operating Range, V _{DD} or V _{AA} (Note 2)3-6VSupply Current, I _{DD} + I _{AA} See Figure 14, 15-38mASupply Standby CurrentClock Stopped During Cycle 1-160- μA Reference Input CurrentSee Figure 10-160- μA TEMPERATURE DEPENDENCYOffset DriftAt 0 to 1 Code Transition4- $\mu V/^o C$ Internal Clock SpeedSee Figure 7	Clock Delay from Start, t _D CLK	See Figure 3	-	200	-	ns
Ready Reset Pulse Width, tw DRSTSee Figure 5-10-nsReady Reset to Data Ready Delay, to ADRDYSee Figure 5-35-nsOutput Enable Delay, tENSee Figure 2-40-nsOutput Disable Delay, tENSee Figure 2-50-nsSupPLIESSee Figure 123-6VSupply Operating Range, VDD or VAA(Note 2)3-6VSupply Current, IDD + IAASee Figures 14, 15-38mASupply Standby CurrentClock Stopped During Cycle 1-3.5-mV/VReference Input CurrentSee Figure 10-160- μ ATEMPERATURE DEPENDENCYAt 0 to 1 Code Transition4- μ V/°CGain DriftAt 1022 to 1023 Code Transition6- μ V/°CInternal Clock SpeedSee Figure 70.5- $\%$ /°C	Ready Reset Removal Time, t _R DRST	See Figure 50 (Note 1)	-	- 80	-	ns
Ready Reset to Data Ready Delay, $t_{D4} DRDY$ See Figure 5-35-nsOutput Enable Delay, t_{EN} See Figure 2-40-nsOutput Disable Delay, t_{DIS} See Figure 2-50-nsSUPPLIESSupply Operating Range, V_{DD} or V_{AA} (Note 2)3-6VSupply Current, $I_{DD} + I_{AA}$ See Figures 14, 15-38mASupply Standby CurrentClock Stopped During Cycle 1-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-160- μA TEMPERATURE DEPENDENCYOffset DriftAt 0 to 1 Code Transition4- $\mu V/^{\circ}C$ Gain DriftAt 1022 to 1023 Code Transition6- $\mu V/^{\circ}C$ Internal Clock SpeedSee Figure 70.5- $9_{V}/^{\circ}C$	Ready Reset Pulse Width, t _W DRST	See Figure 5	-	10	-	ns
Output Enable Delay, t_{EN} See Figure 2-40-nsOutput Disable Delay, t_{DIS} See Figure 2-50-nsSUPPLIESSupply Operating Range, V_{DD} or V_{AA} (Note 2)3-6VSupply Current, $I_{DD} + I_{AA}$ See Figures 14, 15-38mASupply Standby CurrentClock Stopped During Cycle 1-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-25-mV/VReference Input CurrentSee Figure 10-160- μA TEMPERATURE DEPENDENCYOffset DriftAt 0 to 1 Code Transition4- $\mu V/^{\circ}C$ Gain DriftAt 1022 to 1023 Code Transition6- $\mu V/^{\circ}C$ Internal Clock SpeedSee Figure 70.5- $\%/^{\circ}C$	Ready Reset to Data Ready Delay, t _{D4} DRDY	See Figure 5	-	35	-	ns
Output Disable Delay, t_{DIS} See Figure 2-50-nsSUPPLIESSupply Operating Range, V_{DD} or V_{AA} (Note 2)3-6VSupply Current, $I_{DD} + I_{AA}$ See Figures 14, 15-38mASupply Standby CurrentClock Stopped During Cycle 1-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-25-mV/VReference Input CurrentSee Figure 10-160- μA TEMPERATURE DEPENDENCYOffset DriftAt 0 to 1 Code Transition4- $\mu V/^{\circ}C$ Gain DriftAt 1022 to 1023 Code Transition6- $\mu V/^{\circ}C$ Internal Clock SpeedSee Figure 70.5- $\%/^{\circ}C$	Output Enable Delay, t _{EN}	See Figure 2	-	40	-	ns
SUPPLIESSupply Operating Range, V _{DD} or V _{AA} (Note 2)3-6VSupply Current, I _{DD} + I _{AA} See Figures 14, 15-38mASupply Standby CurrentClock Stopped During Cycle 1-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-25-mV/VReference Input CurrentSee Figure 10-160-μATEMPERATURE DEPENDENCYOffset DriftAt 0 to 1 Code Transition4-μV/°CGain DriftAt 1022 to 1023 Code Transition6-μV/°CInternal Clock SpeedSee Figure 70.5-%/°C	Output Disable Delay, t _{DIS}	See Figure 2	-	50	-	ns
Supply Operating Range, V_{DD} or V_{AA} (Note 2)3-6VSupply Current, $I_{DD} + I_{AA}$ See Figures 14, 15-38mASupply Standby CurrentClock Stopped During Cycle 1-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-25-mV/VReference Input CurrentSee Figure 10-160- μA TEMPERATURE DEPENDENCYOffset DriftAt 0 to 1 Code Transition4- $\mu V/^{\circ}C$ Gain DriftAt 1022 to 1023 Code Transition6- $\mu V/^{\circ}C$ Internal Clock SpeedSee Figure 70.5- $\%/^{\circ}C$	SUPPLIES	•				•
Supply Current, $I_{DD} + I_{AA}$ See Figures 14, 15-38mASupply Standby CurrentClock Stopped During Cycle 1-3.5-mAAnalog Supply RejectionAt 120Hz, See Figure 13-25-mV/VReference Input CurrentSee Figure 10-160- μA TEMPERATURE DEPENDENCYOffset DriftAt 0 to 1 Code Transition4- $\mu V/^{\circ}C$ Gain DriftAt 1022 to 1023 Code Transition6- $\mu V/^{\circ}C$ Internal Clock SpeedSee Figure 70.5- $\%/^{\circ}C$	Supply Operating Range, V _{DD} or V _{AA}	(Note 2)	3	-	6	V
Supply Standby Current Clock Stopped During Cycle 1 - 3.5 - mA Analog Supply Rejection At 120Hz, See Figure 13 - 25 - mV/V Reference Input Current See Figure 10 - 160 - μA TEMPERATURE DEPENDENCY Offset Drift At 0 to 1 Code Transition - -4 - μV/°C Gain Drift At 1022 to 1023 Code Transition - -6 - μV/°C Internal Clock Speed See Figure 7 - -0.5 - %/°C	Supply Current, I _{DD} + I _{AA}	See Figures 14, 15	-	3	8	mA
Analog Supply Rejection At 120Hz, See Figure 13 - 25 - mV/V Reference Input Current See Figure 10 - 160 - μA TEMPERATURE DEPENDENCY Mt 0 to 1 Code Transition - -4 - μV/°C Gain Drift At 1022 to 1023 Code Transition - -6 - μV/°C Internal Clock Speed See Figure 7 - -0.5 - %/°C	Supply Standby Current	Clock Stopped During Cycle 1	-	3.5	-	mA
Reference Input Current See Figure 10 - 160 - μA TEMPERATURE DEPENDENCY μV/°C Offset Drift At 0 to 1 Code Transition - -4 - μV/°C Gain Drift At 1022 to 1023 Code Transition - -6 - μV/°C Internal Clock Speed See Figure 7 - -0.5 - %/°C	Analog Supply Rejection	At 120Hz, See Figure 13	-	25	-	mV/V
TEMPERATURE DEPENDENCY Offset Drift At 0 to 1 Code Transition 4 μV/°C Gain Drift At 1022 to 1023 Code Transition 6 - μV/°C Internal Clock Speed See Figure 7 -0.5 - %/°C	Reference Input Current	See Figure 10	-	160	-	μΑ
Offset Drift At 0 to 1 Code Transition - -4 - μV/°C Gain Drift At 1022 to 1023 Code Transition - -6 - μV/°C Internal Clock Speed See Figure 7 - -0.5 - %/°C	TEMPERATURE DEPENDENCY					-
Gain Drift At 1022 to 1023 Code Transition -6 - μV/°C Internal Clock Speed See Figure 7 - -0.5 - %/°C	Offset Drift	At 0 to 1 Code Transition	-	-4	-	μV/ ^o C
Internal Clock Speed See Figure 70.5 - %/°C	Gain Drift	At 1022 to 1023 Code Transition	-	-6	-	μV/°C
	Internal Clock Speed	See Figure 7	-	-0.5	-	%/°C

NOTES:

1. A (-) removal time means the signal can be removed after the reference signal.

2. Parameter not tested, but guaranteed by design or characterization.