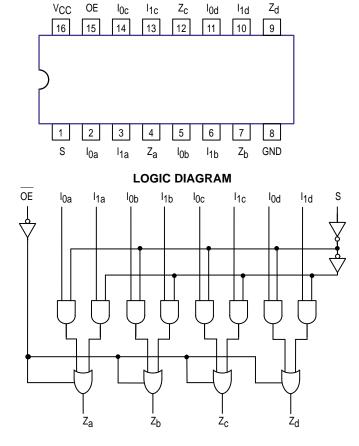


QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC74F257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (OE) input, allowing the outputs to interface directly with bus oriented systems.

CONNECTION DIAGRAM

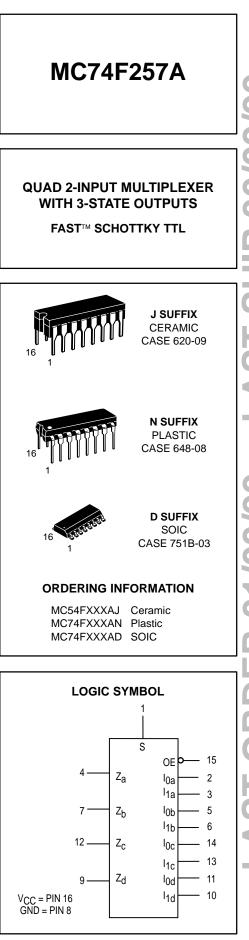
- Multiplexer Expansion by Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects
- AC Enhanced Version of the F257



FUNCTION TABLE

| Output Enable | Select Input | Data Inputs | | | | | | | | Outputs | |
|------------------|-----------------|----------------|----------------|---|--|--|--|--|--|---------|--|
| OE | S | I0 | l ₁ | Z | | | | | | | |
| Н | Х | Х | Х | Z | | | | | | | |
| L | н | Х | L | L | | | | | | | |
| L | Н | Х | Н | н | | | | | | | |
| L | L | L | Х | L | | | | | | | |
| L | L | н | Х | н | | | | | | | |

H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care Z = High Impedance



MC74F257A

GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Тур | Max | Unit |
|-----------------|-------------------------------------|----|-----|-----|------|------|
| VCC | Supply Voltage | 74 | 4.5 | 5.0 | 5.5 | V |
| T _A | Operating Ambient Temperature Range | 74 | 0 | 25 | 70 | °C |
| IOH | Output Current — High | 74 | | | -3.0 | mA |
| I _{OL} | Output Current — Low | 74 | | | 24 | mA |

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| | | | | Limits | | Limits | | Limits | | | | |
|-----------------|------------------------------------|----|-----|--------|------|--------|--|--------------------------|--|--|--|--|
| Symbol | Parameter | | Min | Тур | Max | Unit | Test Conditions | | | | | |
| VIH | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage | | | | | |
| V _{IL} | Input LOW Voltage | | | | 0.8 | V | Guaranteed Input LOW Voltage | | | | | |
| VIK | Input Clamp Diode Voltage | | | | -1.2 | V | I _{IN} =18 mA | V _{CC} = MIN | | | | |
| VOH | Output HIGH Voltage | 74 | 2.4 | 3.3 | | V | I _{OH} = -3.0 mA | V _{CC} = 4.50 V | | | | |
| | | 74 | 2.7 | 3.3 | | V | I _{OH} = -3.0 mA | V _{CC} = 4.75 V | | | | |
| VOL | Output LOW Voltage | - | | 0.35 | 0.5 | V | I _{OL} = 24 mA | V _{CC} = MIN | | | | |
| IOZH | Output OFF Current — HIGH | | | | 50 | μΑ | V _{OUT} = 2.7 V | V _{CC} = MAX | | | | |
| IOZL | Output OFF Current — LOW | | | | -50 | μΑ | V _{OUT} = 0.5 V | V _{CC} = MAX | | | | |
| IIН | Input HIGH Current | | | | 20 | μΑ | V _{IN} = 2.7 V | V _{CC} = MAX | | | | |
| | | | | | 100 | | V _{IN} = 7.0 V | 1 | | | | |
| ۱ _{IL} | Input LOW Current | | | | -0.6 | mA | V _{IN} = 0.5 V | V _{CC} = MAX | | | | |
| los | Output Short Circuit Current (Note | 2) | -60 | | -150 | mA | V _{OUT} = 0 V | V _{CC} = MAX | | | | |
| ІССН | | | | 9.0 | 15 | | S, I _{1X} = 4.5 V | | | | | |
| | | | | | | | OE, I _{0x} = GND | | | | | |
| ICCL | Power Supply Current | | | 14.5 | 22 | mA | I _{1x} = 4.5 V | V _{CC} = MAX | | | | |
| | | | | | | | \overline{OE} , I _{0x,} S = GND | | | | | |
| ICCZ | 1 | | | 15 | 23 | 1 | S, I _{0x} = GND | 1 | | | | |
| | | | | | | | OE, I _{1x} = 4.5 V | | | | | |

NOTES:

h

1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.

2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION

The F257A is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0X} inputs are selected and when Select is HIGH, the I_{1X} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_{a} = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$

$$Z_{b} = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$Z_{c} = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$

$$Z_{d} = OE \bullet (I_{1d} \bullet S + I_{0d} \bullet S)$$

When the Output Enable input (OE) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

AC CHARACTERISTICS

| | | 74F T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF | | $T_A = +25^{\circ}C$ $T_A = 0^{\circ}C$ to $70^{\circ}C$ $V_{CC} = +5.0$ V $V_{CC} = 5.0$ V $\pm 10\%$ | | to 70°C) V \pm 10% | |
|------------------|----------------------------------|---|-----|--|------|--------------------------|--|
| Symbol | Parameter | Min | Мах | Min | Max | Unit | |
| ^t PLH | Propagation Delay | 1.5 | 5.5 | 1.5 | 6.0 | ns | |
| ^t PHL | I _n to Z _n | 2.0 | 5.5 | 2.0 | 6.0 | | |
| ^t PLH | Propagation Delay | 3.0 | 9.5 | 3.0 | 10.5 | ns | |
| ^t PHL | S to Z _n | 2.5 | 7.0 | 2.5 | 8.0 | | |
| ^t PZH | Output Enable Time | 2.0 | 6.5 | 2.0 | 7.0 | ns | |
| ^t PZL | | 2.5 | 7.0 | 2.5 | 8.0 | | |
| ^t PHZ | Output Disable Time | 2.0 | 6.0 | 2.0 | 7.0 | ns | |
| ^t PLZ | | 2.0 | 6.0 | 2.0 | 7.0 | | |

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