HARRIS SEMICONDUCTOR

CD74FCT16511T, CD74FCT162511T

Fast CMOS 16-Bit Registered/Latched Transceivers with Parity

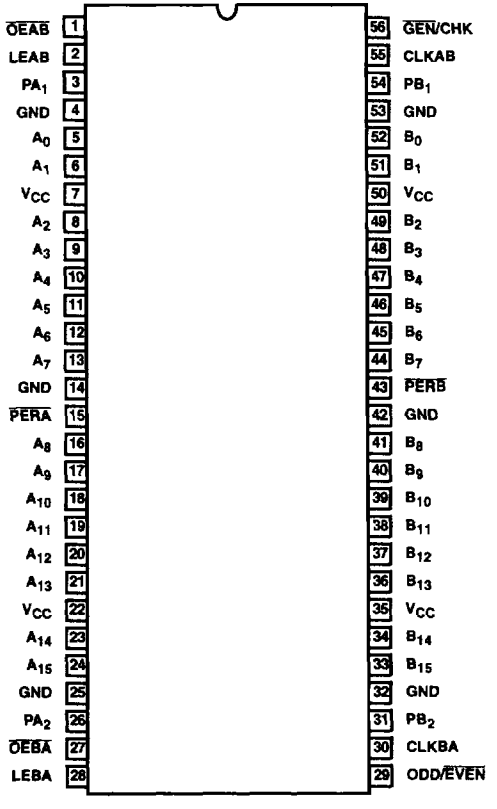
December 1996

Features

- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16511T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162511T**
  - **Balanced Output Drivers: ±24mA**
  - **Open Drain Parity Error Allows Wire-OR**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**

Pinout

CD74FCT16511T, CD74FCT162511T (SSOP, TSSOP)
TOP VIEW



Description

Harris' CD74FCT16511T and CD74FCT162511T are produced in an advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The CD74FCT16511T and CD74FCT162511T are high-speed, low-power 16-bit registered/latched transceiver with parity which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched or clocked modes. It has a parity generator/checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. One error flag for each direction (A-to-B or B-to-A) exists to indicate an error for either byte in either direction. The parity error flags which are open drain outputs, can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. To disable the error flag during combinational transitions, a designer can disable the parity error flag by the $\overline{OEXX}$ control pins.

The operation in A-to-B direction is controlled by LEAB, CLKAB and $\overline{OEAB}$ control pins, and the operation in B-to-A direction is controlled by LEBA, CLKBA and $\overline{OEBA}$ control pins. $\overline{GEN}$/CHK is used to select the operation of A-to-B direction, while B-to-A direction is always in checking mode. The ODD/$\overline{EVEN}$ select is common between the two directions. Independent operation can be achieved between the two directions by using the corresponding control lines except for the ODD/$\overline{EVEN}$ control.

Ordering Information

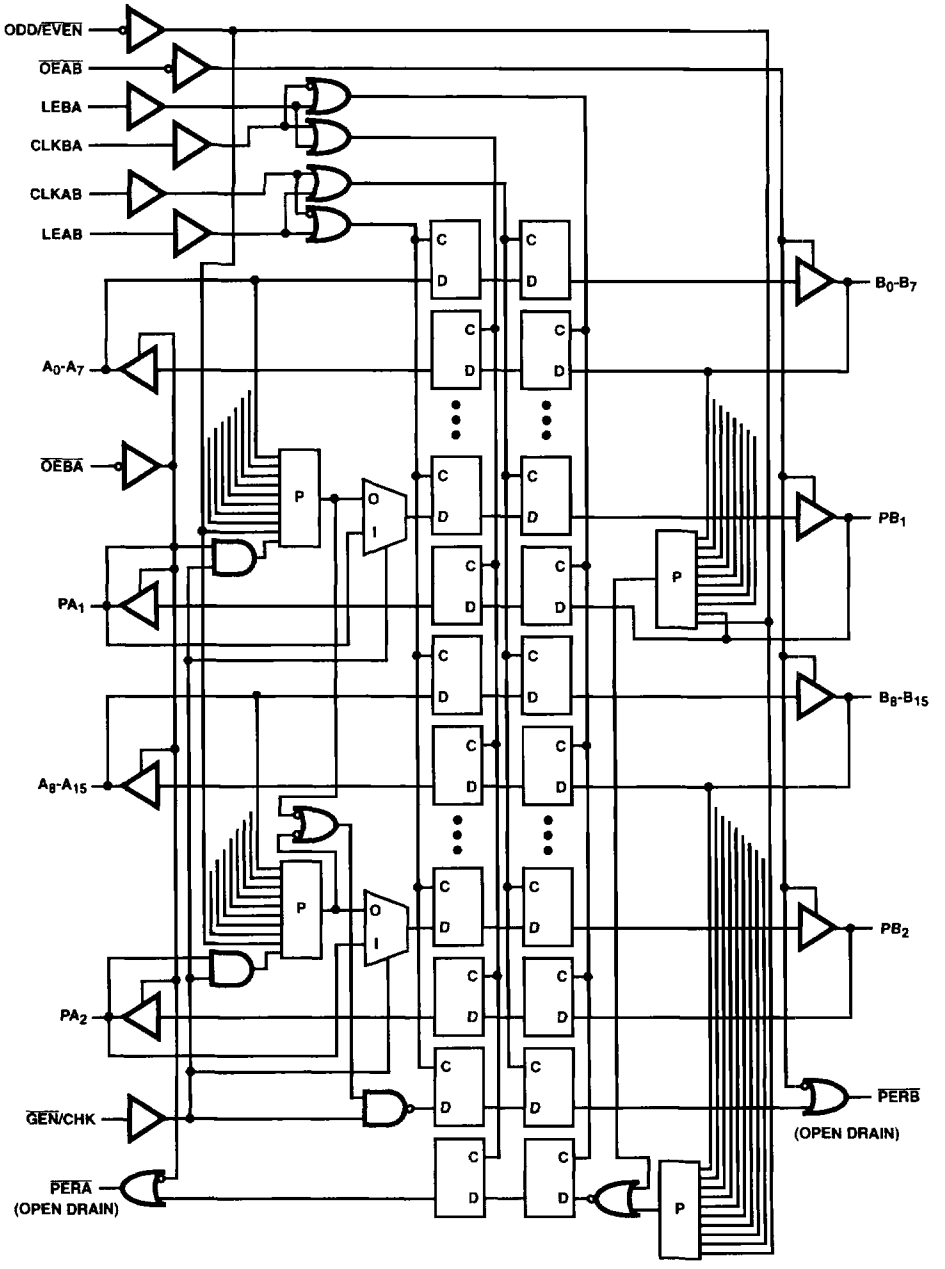
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16511ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16511TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162511ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162511ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162511TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162511TSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

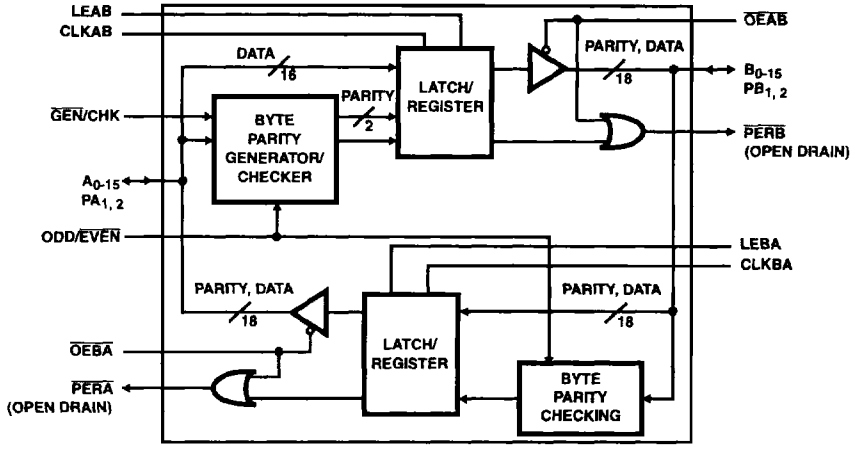
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4218.2**

Functional Block Diagram



Simplified Functional Block Diagram



TRUTH TABLE (NOTES 1, 2)

INPUTS				OUTPUT BUFFERS
$\overline{OEAB}$	LEAB	CLKAB	A_X	B_X
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	B (Note 3)
L	L	H	X	B (Note 4)

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A flow control is the same, except using $\overline{OEBA}$, LEBA, and CLKBA.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, assuming CLKAB was HIGH before LEAB went LOW.

TRUTH TABLE (PARITY GENERATION) (NOTES 5, 6, 7, 8, 9)

TOTAL NUMBER OF INPUTS THAT ARE HIGH, A_0 - A_7	ODD/$\overline{EVEN}$	PB_1
1, 3, 5 or 7	L	H
1, 3, 5 or 7	H	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	H	H

NOTES:

5. Conditions shown are for $\overline{GEN}$/CHK = L, $\overline{OEAB}$ = L, $\overline{OEBA}$ = H.
6. A-to-B parity generation is shown. B-to-A can check parity while A-to-B is performing generation. B-to-A will not generate parity.
7. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
8. Conditions shown are for the byte A0-A7. The byte A8-A15 is similar but will output the parity on PB2.
9. The error flag $\overline{PERB}$ will remain in a high state during parity generation.

TRUTH TABLE (PARITY CHECKING) (NOTES 10, 11, 12, 13)

TOTAL NUMBER OF INPUTS THAT ARE HIGH, A_0 - A_7 AND PA_1 (NOTE 14)	ODD/$\overline{EVEN}$	PB_1
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	H	H (Note 15)
0, 2, 4, 6 or 8	L	H (Note 15)
0, 2, 4, 6 or 8	H	L

10. Conditions shown are for $\overline{GEN}$/CHK = H, $\overline{OEAB}$ = L, $\overline{OEBA}$ = H.
11. A-to-B parity checking is shown. B-to-A parity checking is same but uses $\overline{OEBA}$ = L, $\overline{OEAB}$ = H and errors will be indicated on $\overline{PERA}$.
12. In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors. ($PB_1 = PA_1$)
13. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
14. Conditions shown are for the byte A_0-A_7 and PA_1. The byte A_8-A_{15} and PA_2 is same.
15. The parity error flag $\overline{PERB}$ is a combined flag for both bytes A_0-A_7 and A_8-A_{15}. If a parity error occurs on either byte $\overline{PERB}$ will go low.

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{PERA}$	Parity Error (Open Drain) on A Outputs
$\overline{PERB}$	Parity Error (Open Drain) on B Outputs
A_X	A-to-B Data Inputs or B-to-A Three State Outputs
B_X	B-to-A Data Inputs or B-to-A Three State Outputs
ODD/$\overline{EVEN}$ (Note 16)	Parity Mode Selection Input
$\overline{GEN}$/CHK (Note 16)	A-to-B Port Generate or Check Mode Input
PA_X (Note 17)	A-to-B Parity Input, B-to-A Parity Output
PB_X	B-to-A Parity Input, A-to-B Parity Output
GND	Ground
V_{CC}	Power

NOTES:

16. ODD/$\overline{EVEN}$ and $\overline{GEN}$/CHK should be tied to V_{CC} or GND with no resistor for optimum results.
17. The PA_X pin input is internally disabled during parity generation. This means that when generating parity in the A-to-B direction, there is no need to add a pull-up resistor to guarantee state. The pin will still function properly as the parity output for the B-to-A direction.

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 18)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

18. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 19) TEST CONDITIONS		MIN	(NOTE 20) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = Vcc	-	-	1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = Vcc	-	-	-1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current (I/O Pins)	I_{OS}	V_{CC} = Max (Note 21), V_{OUT} = GND		-80	-140	-225	mA
Output Drive Current (I/O Pins)	I_O	V_{CC} = Max (Note 21), V_{OUT} = 2.5V		-50	-	-180	mA
Output Leakage Current (Open Drain)	I_{OFF}	V_{CC} = Max, V_{OUT} = 4.5V		-	-	±100	µA
Input Hysteresis -	V_H			-	100	-	mV
CD74FCT16511T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V		-	-	±100	µA
CD74FCT162511T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 21)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 21)		-60	-115	-150	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 19) TEST CONDITIONS		MIN	(NOTE 20) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 22)	C_{IN}	V_{IN} = 0V		-	4.5	6.0	pF
I/O Capacitance (Note 22)	$C_{I/O}$	V_{OUT} = 0V		-	5.5	8.0	pF
Open Drain Capacitance (Note 22)	C_O	V_{OUT} = 0V		-	4.5	6.0	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CCL}, I_{CCH}, I_{CCZ}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 23)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 24)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OEAB}$ = GND $\overline{OEBA}$ = VCC One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 26)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle LEAB = $\overline{OEAB}$ = GND $\overline{OEBA}$ = V_{CC} f_i = 5MHz One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.8	1.7 (Note 25)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	3.2 (Note 25)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle LEAB = $\overline{OEAB}$ = GND $\overline{OEBA}$ = V_{CC} f_i = 2.5MHz 18 Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.8	6.5 (Note 25)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	9.0	21.8 (Note 25)	mA

Switching Specifications Over Operating Range (Propagation Delays)

PARAMETER	SYMBOL	(NOTE 27) TEST CONDITIONS	T (NOTE 28) MIN	T MAX	AT (NOTE 28) MIN	AT MAX	UNITS
Propagation Delay PA_X to PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.7	ns
Propagation Delay A_X to B_X or B_X to A_X, PB_X to PA_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.0	ns
Propagation Delay A_X to PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	7.5	ns
Propagation Delay A_X to $\overline{PERB}$, PA_X to $\overline{PERB}$	t_{PLH} (Note 29) t_{PHL}	C_L = 50pF R_L = 500Ω	1.5 1.5	10.5 9.5	1.5 1.5	9.0 8.0	ns ns
Propagation Delay B_X to $\overline{PERA}$, PB_X to $\overline{PERA}$	t_{PLH} (Note 29) t_{PHL}	C_L = 50pF R_L = 500Ω	1.5 1.5	10.5 9.5	1.5 1.5	9.0 8.0	ns ns
Propagation Delay LEBA to A_X and PA_X, LEAB to B_X and PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.6	ns
Propagation Delay LEBA to $\overline{PERA}$, LEAB to $\overline{PERB}$	t_{PLH} (Note 29) t_{PHL}	C_L = 50pF R_L = 500Ω	1.5 1.5	7.5 6.5	1.5 1.5	7.0 6.0	ns ns

Switching Specifications Over Operating Range (Propagation Delays) **(Continued)**

PARAMETER	SYMBOL	(NOTE 27) TEST CONDITIONS	T (NOTE 28) MIN	T MAX	AT (NOTE 28) MIN	AT MAX	UNITS
Propagation Delay CLKBA to A_X and PA_X CLKAB to B_X and PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.6	ns
Propagation Delay CLKBA to $\overline{PERA}$	t_{PLH} (Note 29) t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	7.0	ns
CLKAB to $\overline{PERB}$			1.5	6.5	1.5	6.0	ns
Output Enable Time $\overline{OEBA}$ to A_X and PA_X $\overline{OEAB}$ to B_X and PB_X	t_{PZH} t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	6.0	ns
Output Disable Time (Note 30) $\overline{OEBA}$ to Ax and PAx $\overline{OEAB}$ to Bx and PBx	t_{PHZ} t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	5.6	ns
Parity ERROR Enable $\overline{OEBA}$ to $\overline{PERA}$, $\overline{OEAB}$ to $\overline{PERB}$	t_{PLZ} (Note 29) t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	6.0	ns
			1.5	6.0	1.5	6.0	ns
ODD/$\overline{EVEN}$ to $\overline{PERB}$	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	ns
			1.5	10.0	1.5	10.0	ns
ODD/$\overline{EVEN}$ to PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	ns

Switching Specifications Over Operating Range (Setup Times)

DESCRIPTION	SYMBOL	(NOTES 27, 31) CONDITIONS			T MIN	T MAX	AT MIN	AT MAX	UNITS
Setup Time HIGH or LOW A_X to CLKAB	t_{SU}	$\overline{GEN}$/CHK LOW	PB_X valid	C_L = 50pF R_L = 500Ω	6.5	-	4	-	ns
			PB_X not valid		3	-	3	-	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	4	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
Setup Time PA_X to CLKAB	t_{SU}	$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	4	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
Setup Time B_X to CLKBA PB_X to CLKBA	t_{SU}		$\overline{PERA}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	4	-	ns
			$\overline{PERA}$ not valid		3	-	3	-	ns
Setup Time A_X to LEAB	t_{SU}	CLKAB LOW $\overline{GEN}$/CHK LOW	PB_X valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			PB_X not valid		3	-	3	-	ns
		CLKAB LOW $\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
		CLKAB HIGH $\overline{GEN}$/CHK LOW	PB_X valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			PB_X not valid		3	-	3	-	ns
		CLKAB HIGH $\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns

Switching Specifications Over Operating Range (Setup Times) **(Continued)**

DESCRIPTION	SYMBOL	(NOTES 27, 31) CONDITIONS			T		AT		UNITS
					MIN	MAX	MIN	MAX	
Setup Time PAx to LEAB	t_{SU}	CLKAB LOW $\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
		CLKAB HIGH $\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
Setup Time B_X to LEBA PB_X to LEBA	t_{SU}	CLKBA LOW	$\overline{PERA}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERA}$ not valid		3	-	3	-	ns
		CLKAB HIGH	$\overline{PERA}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERA}$ not valid		3	-	3	-	ns

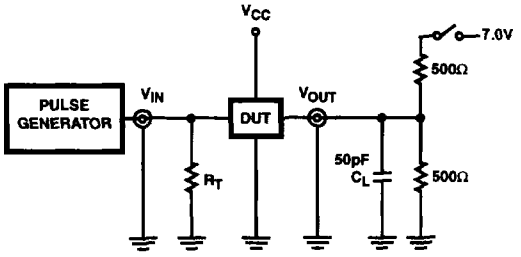
Switching Specifications Over Operating Range (Hold Times)

DESCRIPTION	SYMBOL	(NOTE 27) CONDITIONS	T		AT		UNITS
			MIN	MAX	MIN	MAX	
Hold Time HIGH or LOW A_X to LEAB, B_X to LEBA	t_H	C_L = 50pF R_L = 500Ω	1	-	1	-	ns
Hold Time HIGH or LOW PA_X to LEAB	t_H		1	-	1	-	ns
Hold Time HIGH or LOW PB_X to LEBA	t_H		1	-	1	-	ns
Hold Time A_X to CLKAB, PA_X to CLKAB	t_H		1	-	1	-	ns
Hold Time B_X to CLKBA, PB_X to CLKBA	t_H		1	-	1	-	ns
LEAB or LEBA Pulse Width HIGH (Note 30)	t_W		3	-	3	-	ns
CLKAB or CLKBA Pulse Width HIGH or LOW (Note 30)	t_W		3	-	3	-	ns

NOTES:

19. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
20. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
21. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
22. This parameter is determined by device characterization but is not production tested.
23. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
24. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
25. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
26. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
27. See test circuit and wave forms.
28. Minimum limits are guaranteed but not tested on Propagation Delays.
29. On Open Drain Outputs t_{PLH} is measured up to $V_{OUT} = V_{OL} + 0.3V$.
30. This parameter is guaranteed but not production tested.
31. "Not Valid" means the setup time indicated is not sufficient to assure proper funtioning of this output; however, the set-up time indicated will assure proper functioning of the A-to-B or B-to-A port respective to the indicated direction.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

32. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

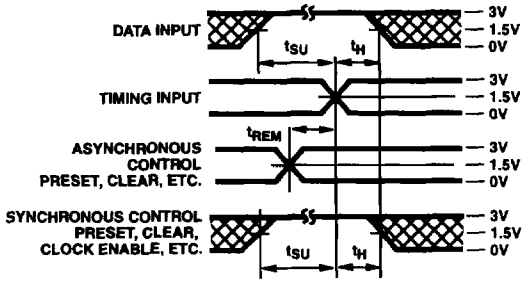


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

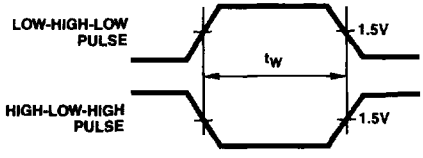


FIGURE 3. PULSE WIDTH

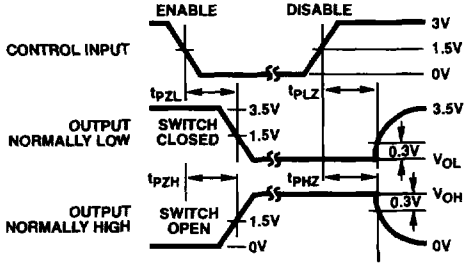


FIGURE 4. ENABLE AND DISABLE TIMING

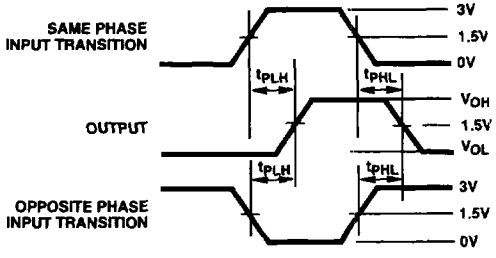


FIGURE 5. PROPAGATION DELAY