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Renesas Electronics website: http://www.renesas.com

April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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# SILICON POWER MOS FET NE5510279A

## 4.8 V OPERATION SILICON RF POWER LDMOS FET FOR 1.8 GHz 2 W TRANSMISSION AMPLIFIERS

#### **DESCRIPTION**

The NE5510279A is an N-channel silicon power MOS FET specially designed as the transmission power amplifier for 4.8 V GSM 1 800 handsets. Dies are manufactured using our NEWMOS technology (our 0.6  $\mu$ m WSi gate laterally diffused MOS FET) and housed in a surface mount package. The device can deliver 33.0 dBm output power with 47% power added efficiency at 1.8 GHz under the 4.8 V supply voltage.

#### **FEATURES**

High output power
 Pout = 35.5 dBm TYP. (VDS = 4.8 V, IDSet = 300 mA, f = 900 MHz, Pin = 25 dBm)

: Pout = 33.0 dBm TYP. (VDS = 4.8 V, IDset = 300 mA, f = 1.8 GHz, Pin = 25 dBm)

• High power added efficiency :  $\eta_{add}$  = 65% TYP. (V<sub>DS</sub> = 4.8 V, I<sub>Dset</sub> = 300 mA, f = 900 MHz, P<sub>in</sub> = 25 dBm)

:  $\eta_{add} = 47\%$  TYP. (VDS = 4.8 V, IDset = 300 mA, f = 1.8 GHz, Pin = 25 dBm)

High linear gain
 G<sub>L</sub> = 16.0 dB TYP. (V<sub>DS</sub> = 4.8 V, I<sub>Dset</sub> = 300 mA, f = 900 MHz, P<sub>in</sub> = 10 dBm)

: GL = 10.0 dB TYP. (VDS = 4.8 V, IDset = 300 mA, f = 1.8 GHz, Pin = 10 dBm)

• Surface mount package : 5.7 × 5.7 × 1.1 mm MAX.

★ • Single supply : VDS = 3.0 to 8.0 V

#### **APPLICATIONS**

• Digital cellular phones : 4.8 V GSM 1 800 class 1 handsets

• Others : General purpose amplifiers for 1.6 to 2.0 GHz TDMA applications

#### ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE5510279A-T1	79A	W2	<ul><li>12 mm wide embossed taping</li><li>Gate pin face the perforation side of the tape</li><li>Qty 1 kpcs/reel</li></ul>

**Remark** To order evaluation samples, contact your nearby sales office.

Part number for sample order: NE5510279A

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

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Not all devices/types available in every country. Please check with local NEC Compound Semiconductor Devices representative for availability and additional information.

#### ABSOLUTE MAXIMUM RATINGS (TA = +25°C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	VDS	20.0	٧
Gate to Source Voltage	Vgs	5.0	V
Drain Current	lσ	1.0	Α
Drain Current (Pulse Test)	ID Note	2.0	Α
Total Power Dissipation	Ptot	20	W
Channel Temperature	Tch	125	°C
Storage Temperature	T <sub>stg</sub>	-65 to +125	°C

**Note** Duty Cycle  $\leq$  50%, Ton  $\leq$  1 s

#### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	V <sub>DS</sub>		3.0	4.8	8.0	V
Gate to Source Voltage	Vgs		0	2.0	3.5	V
Drain Current (Pulse Test)	lο	Duty Cycle ≤ 50%, Ton ≤ 1 s	I	1.0	1.5	Α
Input Power	Pin	f = 1.8 GHz, V <sub>DS</sub> = 4.8 V	25	-	27	dBm

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#### **ELECTRICAL CHARACTERISTICS (TA = +25°C)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	Igss	Vgss = 5.0 V	_	-	100	nA
Drain to Source Leakage Current (Zero Gate Voltage Drain Current)	Ipss	V <sub>DSS</sub> = 8.5 V	_	_	100	nA
Gate Threshold Voltage	Vth	V <sub>DS</sub> = 4.8 V, I <sub>D</sub> = 1 mA	1.0	1.35	2.0	V
Transconductance	Gm	V <sub>DS</sub> = 4.8 V, I <sub>D</sub> = 600 mA	-	1.50	-	S
Drain to Source Breakdown Voltage	BVDSS	loss = 10 $\mu$ A	20	24	-	V
Thermal Resistance	Rth	Channel to Case	_	5	-	°C/W
Linear Gain	GL	f = 900 MHz, P <sub>in</sub> = 10 dBm, V <sub>DS</sub> = 4.8 V, I <sub>Dset</sub> = 300 mA, <b>Note 1, 2</b>	-	16.0	-	dB
Output Power	Pout	f = 900 MHz, Pin = 25 dBm,	-	35.5	-	dBm
Operating Current	lop	V <sub>DS</sub> = 4.8 V, I <sub>Dset</sub> = 300 mA, <b>Note 1, 2</b>	_	1 000	_	mA
Power Added Efficiency	$\eta$ add		_	65	-	%
Linear Gain	GL	f = 1.8 GHz, P <sub>in</sub> = 10 dBm, V <sub>DS</sub> = 4.8 V, I <sub>Dset</sub> = 300 mA, <b>Note 1, 2</b>	-	10.0	-	dB
Output Power	Pout	f = 1.8 GHz, Pin = 25 dBm,	32.0	33.0	-	dBm
Operating Current	lop	V <sub>DS</sub> = 4.8 V, I <sub>Dset</sub> = 300 mA, <b>Note 1, 2</b>	_	750	_	mA
Power Added Efficiency	$\eta$ add		38	47	_	%

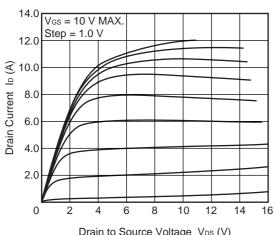
**Notes 1.** Peak measurement at Duty Cycle  $\leq$  50%, Ton  $\leq$  1 s.

**2.** DC performance is 100% testing. RF performance is testing several samples per wafer. Wafer rejection criteria for standard devices is 1 reject for several samples.

Data Sheet PU10121EJ03V0DS

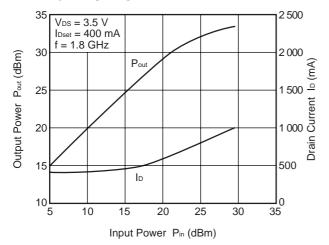
#### TYPICAL CHARACTERISTICS (TA = +25°C)

#### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

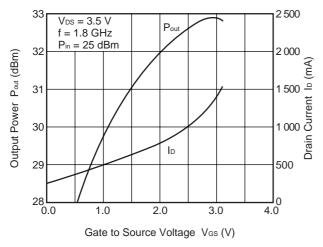


Drain to Source Voltage VDS (V)

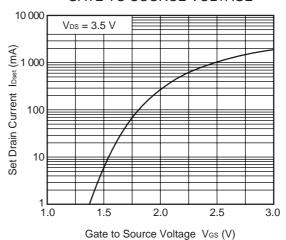
#### **OUTPUT POWER, DRAIN CURRENT** vs. INPUT POWER



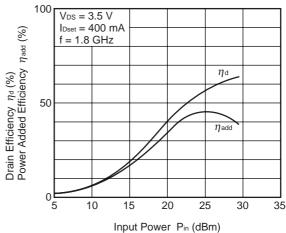
**OUTPUT POWER, DRAIN CURRENT** vs. GATE TO SOURCE VOLTAGE



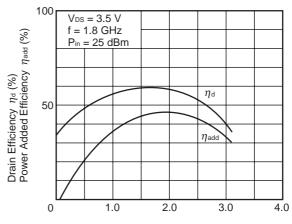
#### SET DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER

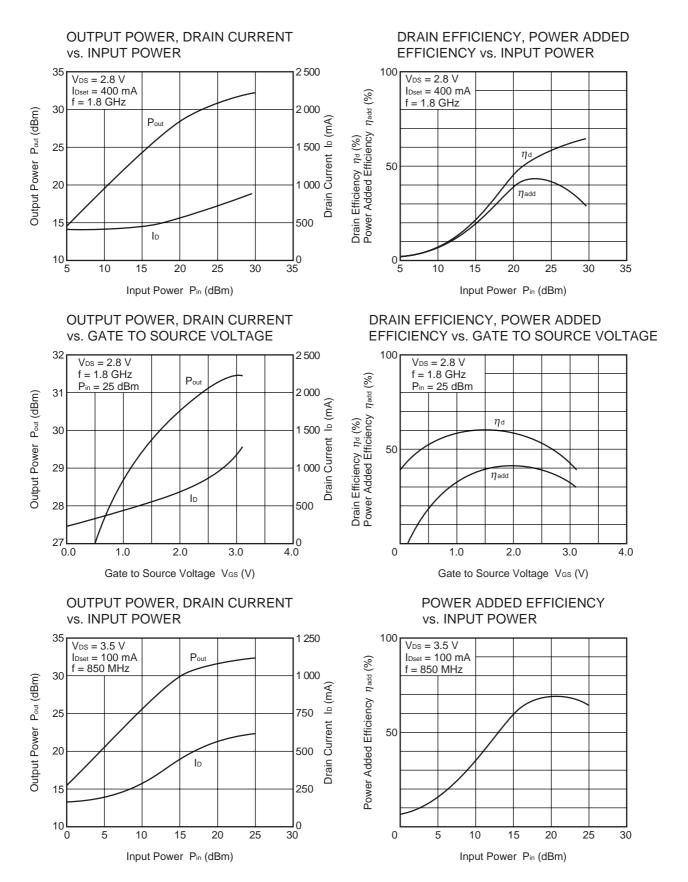


DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



Gate to Source Voltage Vgs (V)





**Remark** The graphs indicate nominal characteristics.

#### **S-PARAMETERS**

S-parameters/Noise parameters are provided on the NEC Compound Semiconductor Devices Web site in a form (S2P) that enables direct import to a microwave circuit simulator without keyboard input.

Click here to download S-parameters.

[RF and Microwave]  $\rightarrow$  [Device Parameters]

URL http://www.csd-nec.com/

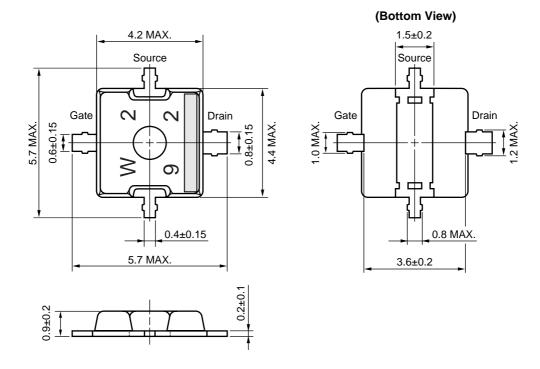
#### LARGE SIGNAL IMPEDANCE (VDS = 3.5 V, ID = 400 mA, Pin = 25 dBm)

f (GHz)	$Z_{in}\left(\Omega\right)$	$ZoL\left(\Omega ight)^{Note}$
1.8	TBD	TBD

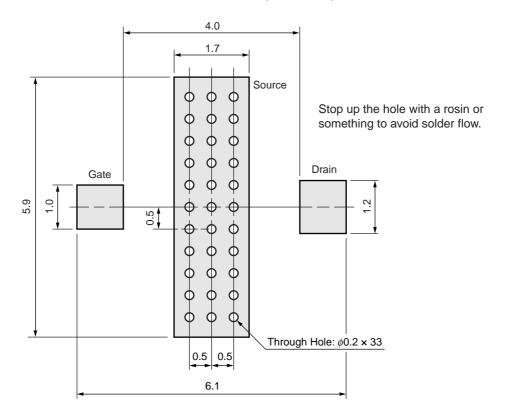
Note ZoL is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

#### **★ PACKAGE DIMENSIONS**

79A (UNIT: mm)



#### 79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)





#### RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2%(Wt.) or below	IR260
VPS	Peak temperature (package surface temperature) Time at temperature of 200°C or higher Preheating time at 120 to 150°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 215°C or below : 25 to 40 seconds : 30 to 60 seconds : 3 times : 0.2%(Wt.) or below	VP215
Wave Soldering	Peak temperature (molten solder temperature) Time at peak temperature Preheating temperature (package surface temperature) Maximum number of flow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 120°C or below : 1 time : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) Soldering time (per pin of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	HS350-P3

Caution Do not use different soldering methods together (except for partial heating).

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M8E 00.4-0110

NEC NE5510279A

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