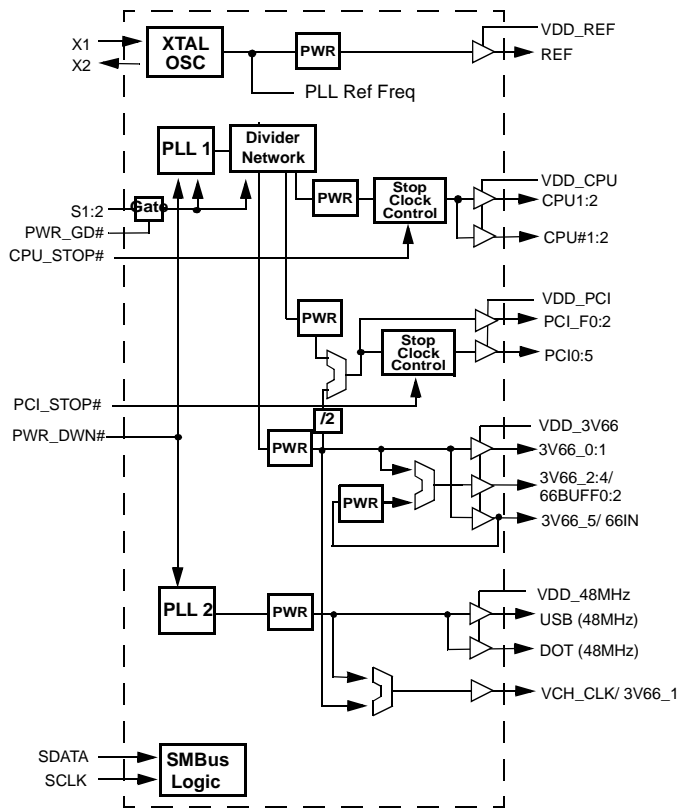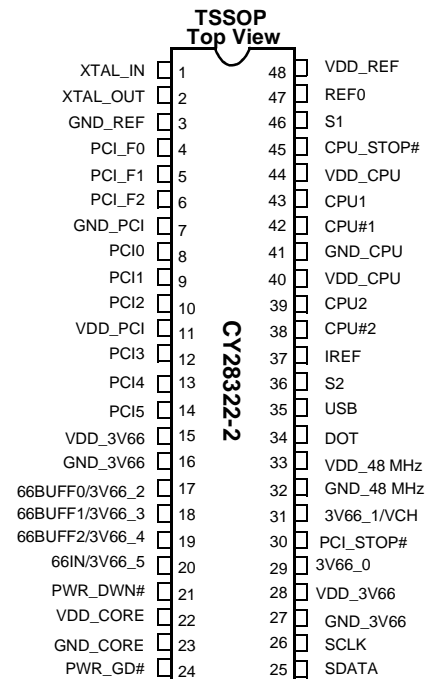# CYPRESS

133-MHz Spread Spectrum Clock Synthesizer with Differential CPU Outputs

Features	Benefits
• **Compliant with Intel® CK-Titan and CK-408 clock synthesizer/driver specifications**	Supports next generation Pentium® processors using differential clock drivers
• **Multiple output clocks at different frequencies**	Motherboard clock generator
—**Two pairs of differential CPU outputs, up to 200 MHz**	—Support multiple CPUs and a chipset
—**Nine synchronous PCI clocks, three free-running**	—Support for PCI slots and chipset
—**Six 3V66 clocks**	—Supports AGP, DRCG reference, and Hub Link
—**Two 48-MHz clocks**	—Supports USB host and graphic controllers
—**One reference clock at 14.318 MHz**	—Supports ISA slots and I/O chip
—**One VCH clock**	
• **Spread Spectrum clocking (down spread)**	Enables reduction of EMI and overall system cost
• **Power-down features (PCI_STOP#, CPU_STOP# PWR_DWN#)**	Enables ACPI-compliant designs
• **Two select inputs (Mode select & IC Frequency Select)**	Supports up to four CPU clock frequencies
• **48-pin TSSOP package**	Widely available, standard package enables lower cost

Logic Block Diagram

Pin Configurations

TSSOP Top View

XTAL_IN	1		48	VDD_REF
XTAL_OUT	2		47	REF0
GND_REF	3		46	S1
PCI_F0	4		45	CPU_STOP#
PCI_F1	5		44	VDD_CPU
PCI_F2	6		43	CPU1
GND_PCI	7		42	CPU#1
PCI0	8		41	GND_CPU
PCI1	9		40	VDD_CPU
PCI2	10		39	CPU2
VDD_PCI	11	CY28322-2	38	CPU#2
PCI3	12		37	IREF
PCI4	13		36	S2
PCI5	14		35	USB
VDD_3V66	15		34	DOT
GND_3V66	16		33	VDD_48 MHz
66BUFF0/3V66_2	17		32	GND_48 MHz
66BUFF1/3V66_3	18		31	3V66_1/VCH
66BUFF2/3V66_4	19		30	PCI_STOP#
66IN/3V66_5	20		29	3V66_0
PWR_DWN#	21		28	VDD_3V66
VDD_CORE	22		27	GND_3V66
GND_CORE	23		26	SCLK
PWR_GD#	24		25	SDATA

Pin Summary

Pin Name	Pin Number	Pin Description
REF0	47	3.3V 14.318-MHz clock output
XTAL_IN	1	14.318-MHz crystal input
XTAL_OUT	2	14.318-MHz crystal input
CPU, CPU# [1:2]	43, 39, 42, 38	Differential CPU clock outputs
3V66_0	29	3.3V 66-MHz clock output
3V66_1/VCH	31	3.3V selectable through SMBus to be 66 MHz or 48 MHz
66IN/3V66_5	20	66-MHz input to buffered 66BUFF and PCI or 66-MHz clock from internal VCO
66BUFF [2:0] /3V66 [4:2]	17, 18, 19	66-MHz buffered outputs from 66Input or 66-MHz clocks from internal VCO
PCI_F [0:2]	4, 5, 6	33 MHz clocks divided down from 66Input or divided down from 3V66
PCI [0:5]	8, 9, 10, 12, 13, 14	PCI clock outputs divided down from 66Input or divided down from 3V66
USB	35	Fixed 48-MHz clock output
DOT	34	Fixed 48-MHz clock output
S2	36	Special 3.3V 3-level input for Mode selection
S1	46	3.3V LVTTL inputs for CPU frequency selection
IREF	37	A precision resistor is attached to this pin which is connected to the internal current reference
PWR_DWN#	21	3.3V LVTTL input for Power_Down# (active LOW)
PCI_STOP#	30	3.3V LVTTL input for PCI_STOP# (active LOW)
CPU_STOP#	45	3.3V LVTTL input for CPU_STOP# (active LOW)
PWRGD#	24	3.3V LVTTL input is a level sensitive strobe used to determine when S[2:1] inputs are valid and OK to be sampled (Active LOW). Once PWRGD# is sampled LOW, the status of this output will be ignored.
SDATA	25	SMBus compatible SDATA
SCLK	26	SMBus compatible Sclk
VDD_PCI, VDD_3V66, VDD_CPU,VDD_REF	11, 15, 28, 40, 44, 48	3.3V power supply for outputs
VDD_48 MHz	33	3.3V power supply for 48 MHz
VDD_CORE	22	3.3V power supply for PLL
GND_REF, GND_PCI, GND_3V66, GND_IREF, GND_CPU	3, 7, 16, 27, 32, 41	Ground for outputs
GND_CORE	23	Ground for PLL

Function Table[1]

S2	S1	CPU (MHz)	3V66[0:1] (MHz)	66BUFF[0:2]/3 V66[2:4] (MHz)	66IN/3V66_5 (MHz)	PCI_F/PCI (MHz)	REF0(MHz)	USB/DOT (MHz)	Notes
1	0	100 MHz	66 MHz	66IN	66 MHz Input	66IN/2	14.318 MHz	48 MHz	2, 3, 4
1	1	133 MHz	66 MHz	66IN	66 MHz Input	66IN/2	14.318 MHz	48 MHz	2, 3, 4
0	0	100 MHz	66 MHz	66 MHz	66 MHz	33 MHz	14.318 MHz	48 MHz	2, 3, 4
0	1	133 MHz	66 MHz	66 MHz	66 MHz	33 MHz	14.318 MHz	48 MHz	2, 3, 4
Mid	0	TCLK/2	TCLK/4	TCLK/4	TCLK/4	TCLK/8	TCLK	TCLK/2	7, 8, 5
Mid	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	–

Notes:
1. TCLK is a test clock driven in on the XTALIN input in test mode.
2. "Normal" mode of operation
3. Range of reference frequency allowed is min. = 14.316 nominal = 14.31818 MHz, max = 14.32 MHz.
4. Frequency accuracy of 48 MHz must be +167 PPM to match USB default.
5. Mid is defined a voltage level between 1.0V and 1.8V for 3 level input functionality. Low is below 0.8V. High is above 2.0V.
6. Required for DC output impedance verification.
7. These modes are to use the same internal dividers as the CPU = 200-MHz mode. The only change is to slow down the internal VCO to allow under clock margining.
8. All parameters specified with loaded outputs.

Clock Driver Impedances

Buffer	V$_{DD}$ Range	Buffer Type	Impedance		
			Min. Ω	Typ. Ω	Max. Ω
CPU, CPU#		Type X1		50	
REF	3.135–3.465	Type 3	20	40	60
PCI, 3V66, 66BUFF	3.135–3.465	Type 5	12	30	55
USB	3.135–3.465	Type 3A	12	30	55
DOT	3.135–3.465	Type 3B	12	30	55

Clock Enable Configuration

PWR_DWN#	CPU_STOP#	PCI_STOP#	CPU	CPU#	3V66	66BUFF	PCI_F	PCI	USB/DOT	VCOS/OSC
0	X	X	IREF*2	FLOAT	LOW	LOW	LOW	LOW	LOW	OFF
1	0	0	IREF*2	FLOAT	ON	ON	ON	OFF	ON	ON
1	0	1	IREF*2	FLOAT	ON	ON	ON	ON	ON	ON
1	1	0	ON	ON	ON	ON	ON	OFF	ON	ON
1	1	1	ON	ON	ON	ON	ON	ON	ON	ON

Serial Data Interface (SMBus)

To enhance the flexibility and function of the clock synthesizer, a two signal SMBus interface is provided according to SMBus specification. Through the Serial Data Interface, various device functions such as individual clock output buffers, can be individually enabled or disabled. CY28322-2 supports both block read and block write operations.

The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions.
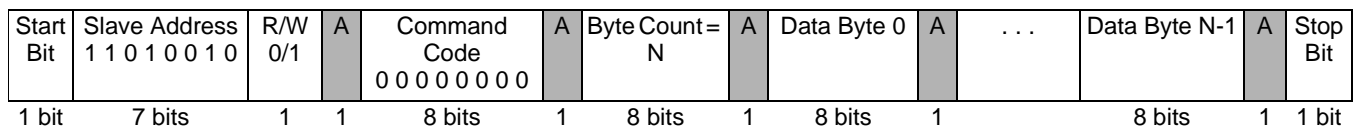
Data Protocol

The clock driver serial protocol accepts only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte, (most significant bit first) with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed.

A block write begins with a slave address and a WRITE condition. The R/W bit is used by the SMBus controller as a data direction bit. A zero indicates a WRITE condition to the clock device. The slave receiver address is 11010010 (D2h).

A command code of 0000 0000 (00h) and the byte count bytes are required for any transfer. After the command code, the core logic issues a byte count which describes number of additional bytes required for the transfer, not including the command code and byte count bytes. For example, if the host has 20 data bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes It may not be 0. *Figure 1* shows an example of a block write.

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller.

Start Bit	Slave Address 1 1 0 1 0 0 1 0	R/W 0/1	A	Command Code 0 0 0 0 0 0 0 0	A	Byte Count = N	A	Data Byte 0	A	. . .	Data Byte N-1	A	Stop Bit
1 bit	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit

☐ From Master to Slave
■ From Slave to Master

Figure 1. An Example of a Block Write

Data Byte Configuration Map

Data Byte 0: Control Register (0 = Enable, 1 = Disable)

Bit	Affected Pin#	Name	Description	Type	Power-on Default
Bit 7	4, 5, 6, 10, 11, 12, 13, 16, 17, 18, 33, 35	PCI [0:6] CPU[2:1] 3V66[1:0]	**Spread Spectrum Enable** 0 = Spread Off, 1 = Spread On	R/W	0
Bit 6	–	TBD	TBD	R	0
Bit 5	31	3V66_1/VCH	**VCH Select 66 MHz/48 MHz** 0 = 66 MHz, 1 = 48 MHz	R/W	0
Bit 4	39, 43, 38, 42	CPU [2:1] CPU# [2:1]	**CPU_STOP#** Reflects the current value of the external CPU_STOP# pin	R	N/A
Bit 3	8, 9, 10, 11, 12, 13, 14,	PCI [5:0]	**PCI_STOP#** (Does not affect PCI_F [2:0] pins)	R/W	N/A
Bit 2	–	–	**S2**–Reflects the value of the S2 pin sampled on power-up	R	N/A
Bit 1	–	–	**S1**–Reflects the value of the S1 pin sampled on power-up	R	N/A
Bit 0	–	–	Reserved	R	1

Data Byte 1

Bit	Pin#	Name	Description	Type	Power-on Default
Bit 7	–	N/A	CPU Mult0 Value	R	N/A
Bit 6	43,39,	CPU1:2	Three-state CPU1:2 during power-down 0 = Normal; 1 = Three-stated	R/W	0
Bit 5	38, 39	CPU2 CPU2#	Allow Control of CPU2 with assertion of CPU_STOP# 0 = Not free running; 1 = Free running	R/W	0
Bit 4	42, 43	CPU1 CPU1#	Allow Control of CPU1 with assertion of CPU_STOP# 0 = Not free running;1 = Free running	R/W	0
Bit 3	–	Reserved	Reserved	R/W	0
Bit 2	38, 39	CPU2 CPU2#	CPU2 Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 1	42, 43	CPU1 CPU1#	CPU1Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 0	–	Reserved	Reserved	R/W	1

Data Byte 2

Bit	Pin#	Name	Pin Description	Type	Power-on Default
Bit 7		N/A	N/A	R	0
Bit 6	14	PCI5	PCI5 Output Enable 1 = Enabled, 0 = Disabled	R/W	1
Bit 5	13	PCI4	PCI4 Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 4	12	PCI3	PCI3 Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 3	10	PCI2	PCI2Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 2	9	PCI1	PCI1 Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 1	8	PCI0	PCI0 Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 0		Reserved	Write to"0"	R/W	1

Data Byte 3

Bit	Pin#	Name	Pin Description	Type	Power-on Default
Bit 7	34	DOT	DOT 48-MHz Output Enable	R/W	1
Bit 6	35	USB	USB 48-MHz Output Enable	R/W	1
Bit 5	6	PCI_F2	Allow control of PCI_F2 with assertion of PCI_STOP# 0 = Free running; 1 = Stopped with PCI_STOP#	R/W	0
Bit 4	5	PCI_F1	Allow control of PCI_F1 with assertion of PCI_STOP# 0 = Free running; 1 = Stopped with PCI_STOP#	R/W	0
Bit 3	4	PCI_F0	Allow control of PCI_F0 with assertion of PCI_STOP# 0 = Free running; 1 = Stopped with PCI_STOP#	R/W	0
Bit 2	6	PCI_F2	PCI_F2 Output Enable	R/W	1
Bit 1	5	PCI_F1	PCI_F1Output Enable	R/W	1
Bit 0	4	PCI_F0	PCI_F0 Output Enable	R/W	1

Data Byte 4

Bit	Pin#	Name	Pin Description	Type	Power-on Default
Bit 7	–	TBD	N/A	R	0
Bit 6	–	TBD	N/A	R	0
Bit 5	29	3V66_0	3V66_0 Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 4	31	3V66_1/VCH	3V66_1/VCH Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 3	20	66IN/3V66_5	3V66_5 Output Enable 1 = Enable; 0 = Disable Note. This bit should be used when pin 24 is configured as 3v66_5 output. Do not clear this bit when pin 24 is configured as 66IN input.	R/W	1
Bit 2	19	66BUFF2	66-MHz Buffered 2 Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 1	18	66BUFF1	66-MHz Buffered 1 Output Enable 1 = Enabled; 0 = Disabled	R/W	1
Bit 0	17	66BUFF0	66-MHz Buffered 0 Output Enable 1 = Enabled; 0 = Disabled	R/W	1

Data Byte 5

Bit	Pin#	Name	Pin Description	Type	Power-on Default
Bit 7		N/A	N/A	R	0
Bit 6		N/A	N/A	R	0
Bit 5		66BUFF [2:0]	Tpd 66IN to 66BUFF propagation delay control	R/W	0
Bit 4		66BUFF [2:0]		R/W	0
Bit 3		DOT	DOT edge rate control	R/W	0
Bit 2		DOT		R/W	0
Bit 1		USB	USB edge rate control	R/W	0
Bit 0		USB		R/W	0

Byte 6: Vendor ID

Bit	Description	Type	Power-on Default
Bit 7	Revision Code Bit 3	R	0
Bit 6	Revision Code Bit 2	R	0
Bit 5	Revision Code Bit 1	R	0

Byte 6: Vendor ID (continued)

Bit	Description	Type	Power-on Default
Bit 4	Revision Code Bit 0	R	0
Bit 3	Vendor ID Bit 3	R	1
Bit 2	Vendor ID Bit 2	R	0
Bit 1	Vendor ID Bit 1	R	0
Bit 0	Vendor ID Bit 0	R	0

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ....–0.5 to +7.0V

Input Voltage .... –0.5V to V_{DD}+0.5

Storage Temperature (Non-condensing) .... –65°C to +150°C

Max. Soldering Temperature (10 sec) .... +260°C

Junction Temperature .... +150°C

Package Power Dissipation..1Ω

Static Discharge Voltage ....
(per MIL-STD-883, Method 3015) .... > 2000V

Operating Conditions[9] Over which Electrical Parameters are Guaranteed

Parameter	Description	Min.	Max.	Unit
V_{DD_REF}, V_{DD_PCI}, V_{DD_CORE}, V_{DD_3V66}, V_{DD_CPU},	3.3V Supply Voltages	3.135	3.465	V
$V_{DD\_48\ MHz}$	48-MHz Supply Voltage	2.85	3.465	V
T_A	Operating Temperature, Ambient	0	70	°C
C_{in}	Input Pin Capacitance		5	pF
C_{XTAL}	XTAL Pin Capacitance		22.5	pF
C_L	Max. Capacitive Load on USBCLK, REF PCICLK, 3V66		20 30	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

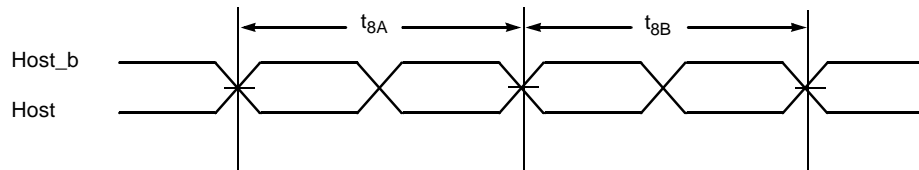| Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Pads. Threshold voltage for crystal pads = V_{DD}/2		2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Pads			0.8	V
V_{OH}	High-level Output Voltage	USB, REF, 3V66	I_{OH} = –1 mA	2.4		V
		PCI	I_{OH} = –1 mA	2.4		V
V_{OL}	Low-level Output Voltage	USB, REF, 3V66	I_{OL} = 1 mA		0.4	V
		PCI	I_{OL} = 1 mA		0.55	V
I_{IH}	Input High Current	$0 \leq V_{IN} \leq V_{DD}$		–5	5	mA
I_{IL}	Input Low Current	$0 \leq V_{IN} \leq V_{DD}$		–5	5	mA
I_{OH}	High-level Output Current	CPU For I_{OH} =6*IRef Configuration	Type X1, V_{OH} = 0.65V	12.9		mA
			Type X1, V_{OH} = 0.74V		14.9	
		REF, DOT, USB	Type 3, V_{OH} = 1.00V	–29		
			Type 3, V_{OH} = 3.135V		–23	
		3V66, DOT, PCI	Type 5, V_{OH} = 1.00V	–33		
			Type 5, V_{OH} = 3.135V		–33	
I_{OL}	Low-level Output Current	REF, DOT, USB	Type 3, V_{OL} = 1.95V	29		mA
			Type 3, V_{OL} = 0.4V		27	
		3V66, PCI	Type 5, V_{OL} =1.95 V	30		
			Type 5, V_{OL} = 0.4V		38	
I_{OZ}	Output Leakage Current	Three-state			10	mA
I_{DD3}	3.3V Power Supply Current	VDD_CORE/VDD3.3 = 3.465V, F_{CPU} = 133 MHz			360	mA
I_{DDPD3}	3.3V Shutdown Current	VDD_CORE/VDD3.3 = 3.465V and @ IREF = 2.32 mA (Byte1, Bit [6] = 0)			25	mA
I_{DDPD3}	3.3V Shutdown Current	VDD_CORE/VDD3.3 = 3.465V and @ IREF = 5.0 mA (Byte1, Bit [6] = 0)			45	mA
I_{DDPD3}	3.3V Shutdown Current	VDD_CORE/VDD3.3 = 3.465V (Byte1, Bit [6] = 1)			1.5	mA

Switching Characteristics[8] Over the Operating Range

| Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle[9]	Measured at 1.5V	45	55	%
t_3	USB, REF, DOT	Falling Edge Rate	Between 2.4V and 0.4V	0.5	2.0	ns
t_3	PCI,3V66	Falling Edge Rate	Between 2.4V and 0.4V	1.0	4.0	V/ns
t_5	3V66[0:1]	3V66-3V66 Skew	Measured at 1.5V		500	ps
t_5	66BUFF[0:2]	66BUFF-66BUFF Skew	Measured at 1.5V		175	ps
t_6	PCI	PCI-PCI Skew	Measured at 1.5V		500	ps
t_7	3V66, PCI	3V66-PCI Clock Jitter	3V66 leads. Measured at 1.5V	1.5	3.5	ns
t_9	3V66	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		250	ps
t_9	USB, DOT	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		350	ps
t_9	PCI	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		500	ps
t_9	REF	Cycle-Cycle Clock Jitter	Measured at 1.5V $t_9 = t_{9A} - t_{9B}$		1000	ps
CPU 1.0V Switching Characteristics						
t_2	CPU	Rise Time	Measured differential waveform from −0.35V to +0.35V	175	467	ps
t_3	CPU	Fall Time	Measured differential waveform from −0.35V to +0.35V	175	467	ps
t_4	CPU	CPU-CPU Skew	Measured at Crossover		150	ps
t_8	CPU	Cycle-Cycle Clock Jitter	Measured at Crossover $t_8 = t_{8A} - t_{8B}$		150	ps
	CPU	Rise/Fall Matching	Measured with test loads[11]		325	mV
V_{oh}	CPU	High-level Output Voltage including overshoot	Measured with test loads[12]	0.92	1.45	V
V_{ol}	CPU	Low-level Output Voltage including undershoot	Measured with test loads[12]	−0.2	0.35	V
$V_{crossover}$	CPU	Crossover Voltage	Measured with test loads[12]	0.51	0.76	V

Notes:
9. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
10. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DD} = 2.5V, duty cycle is measured at 1.25V.
11. Determined as a fraction of 2*(Trp – Trn)/(Trp +Trn) where Trp is a rising edge and Trn is an intersecting falling edge.
12. The 1.0V test load is shown on test circuit page.

Definition and Application of PWRGD# Signal
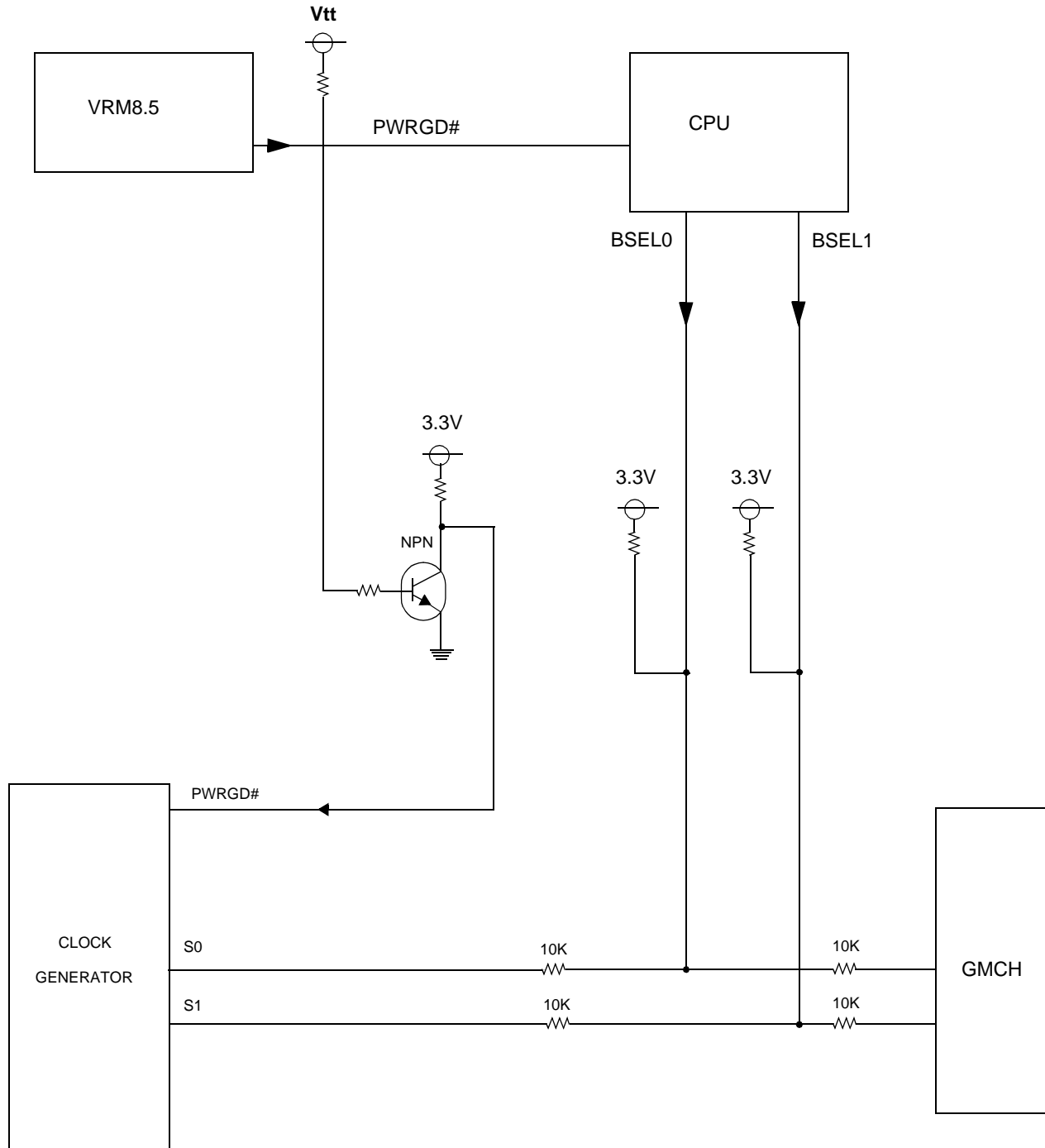
Switching Waveforms

Duty Cycle Timing **(Single-ended Output)**
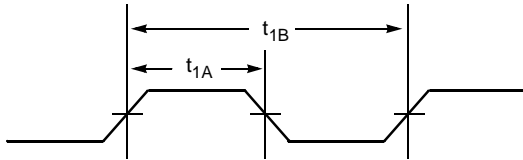
Duty Cycle Timing (CPU Differential Output)
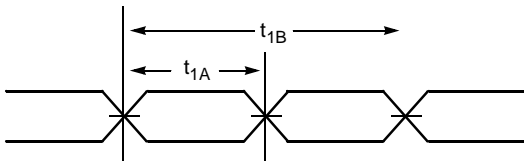
All Outputs Rise/Fall Time
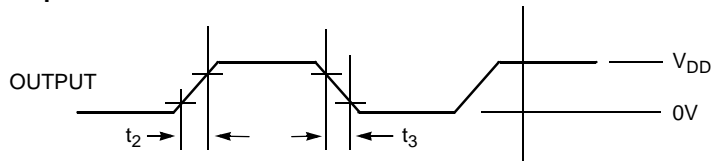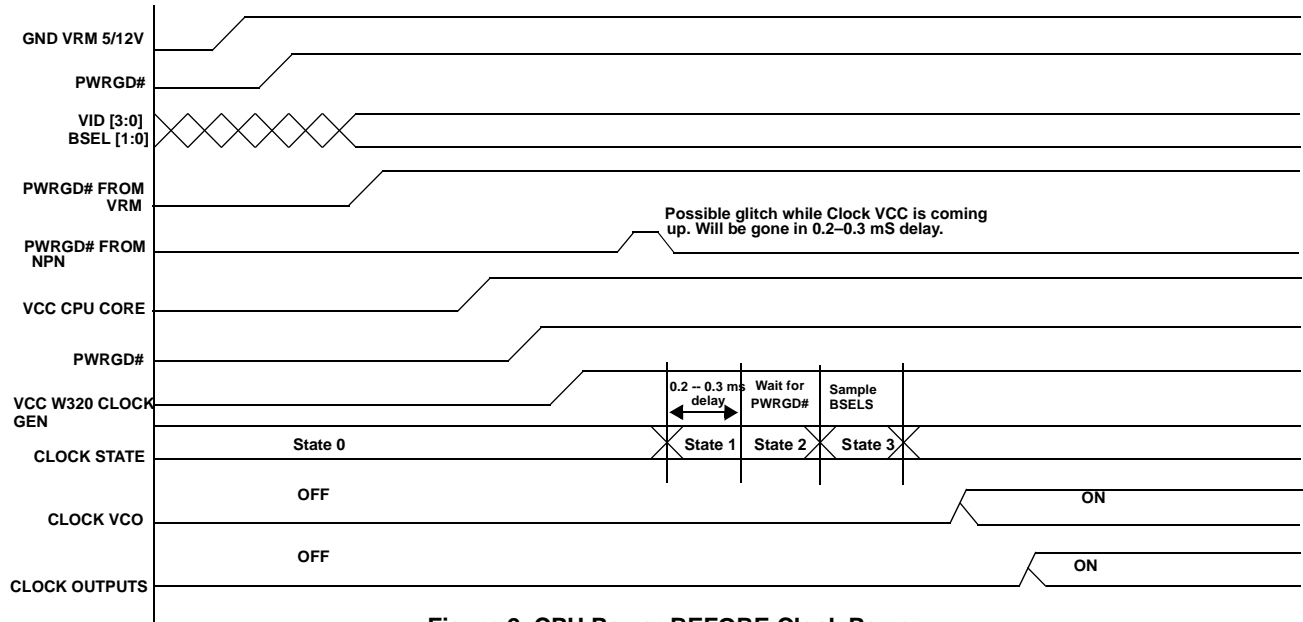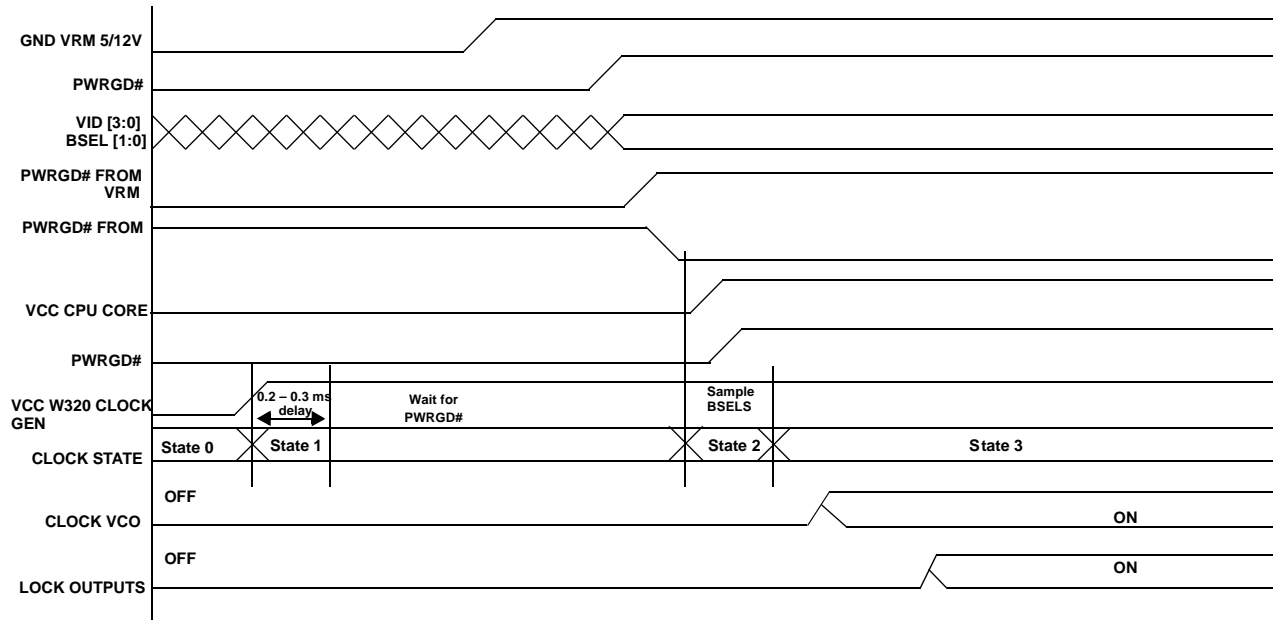

CPU-CPU Clock Skew
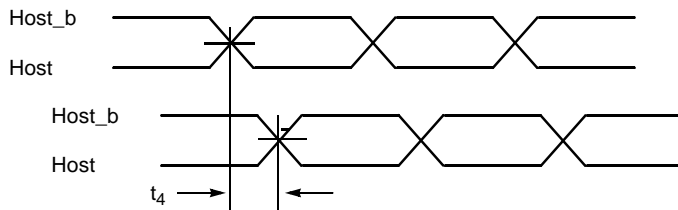
3V66-3V66 Clock Skew
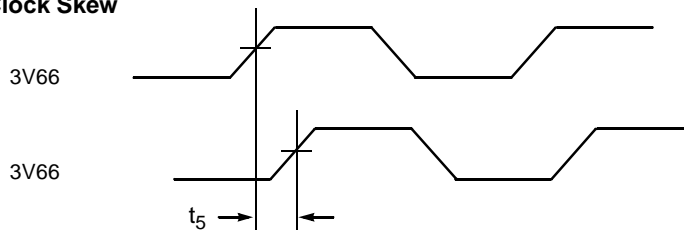
Switching Waveforms (continued)

PCI-PCI Clock Skew

PCI

PCI

t_6
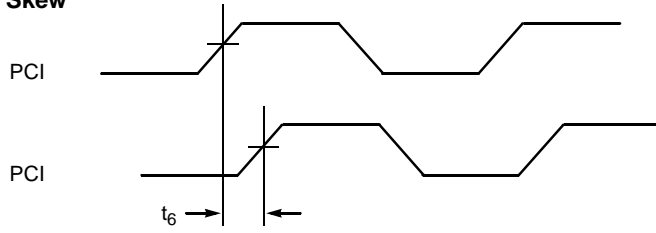
3V66-PCI Clock Skew

3V66

PCI

t_7
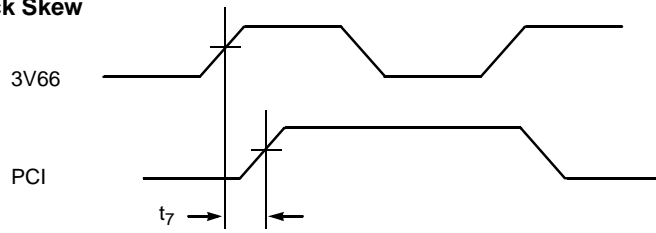
CPU Clock Cycle-Cycle Jitter

t_{8A} t_{8B}

Host_b

Host

Cycle-Cycle Clock Jitter

t_{9A} t_{9B}
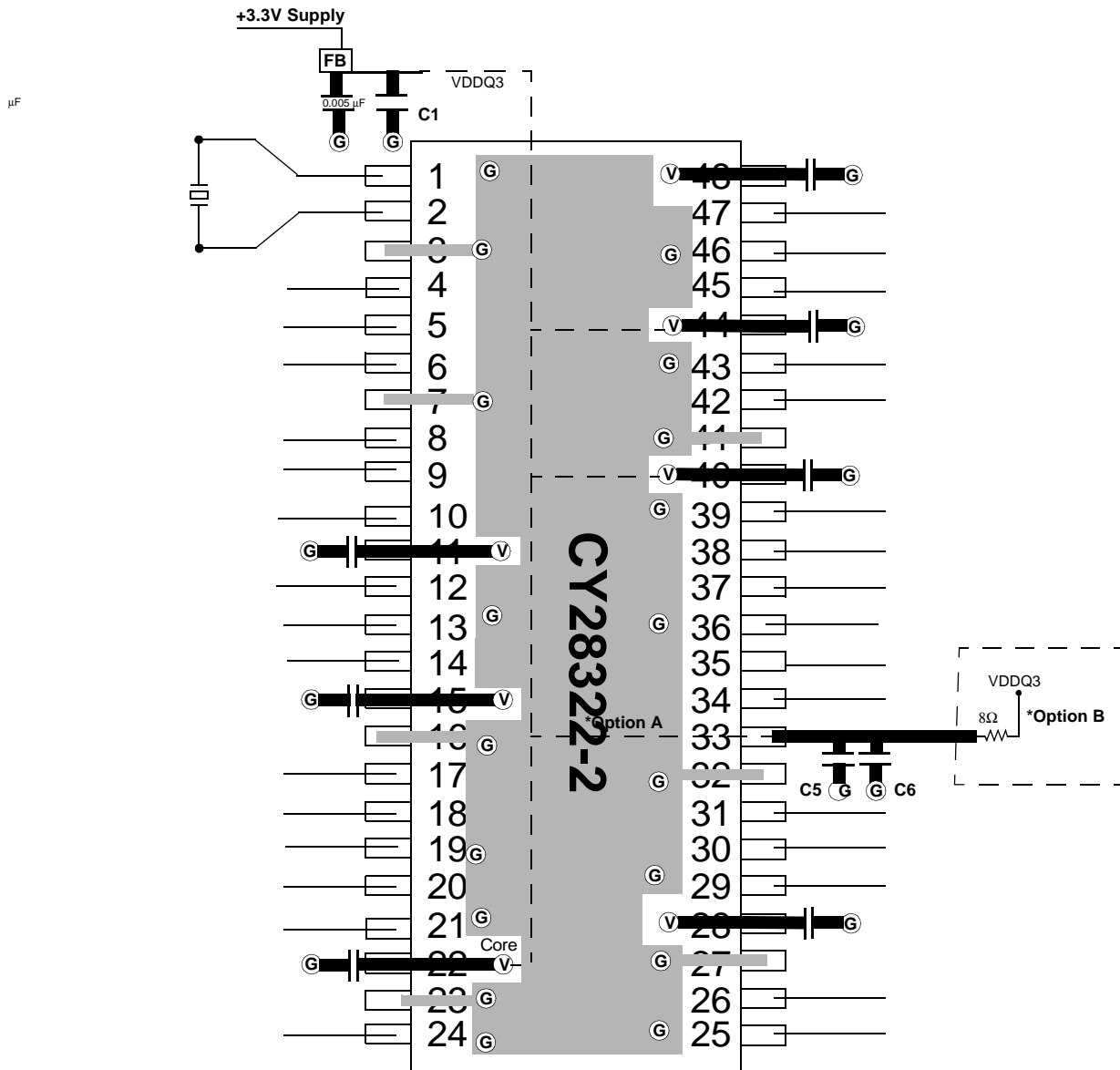
CLK
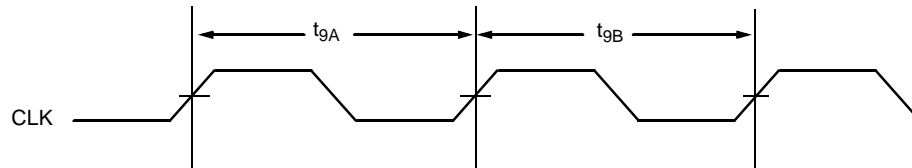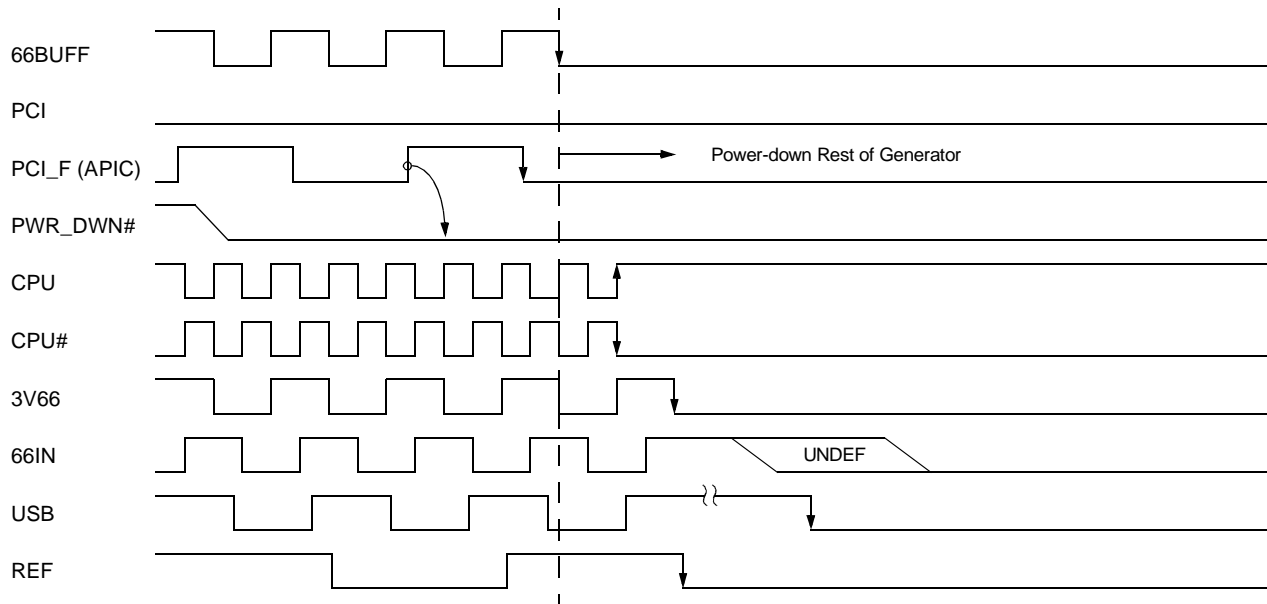
PWRDWN# Assertion

Note: PCI_STOP# asserted LOW

PWRDWN# Deassertion
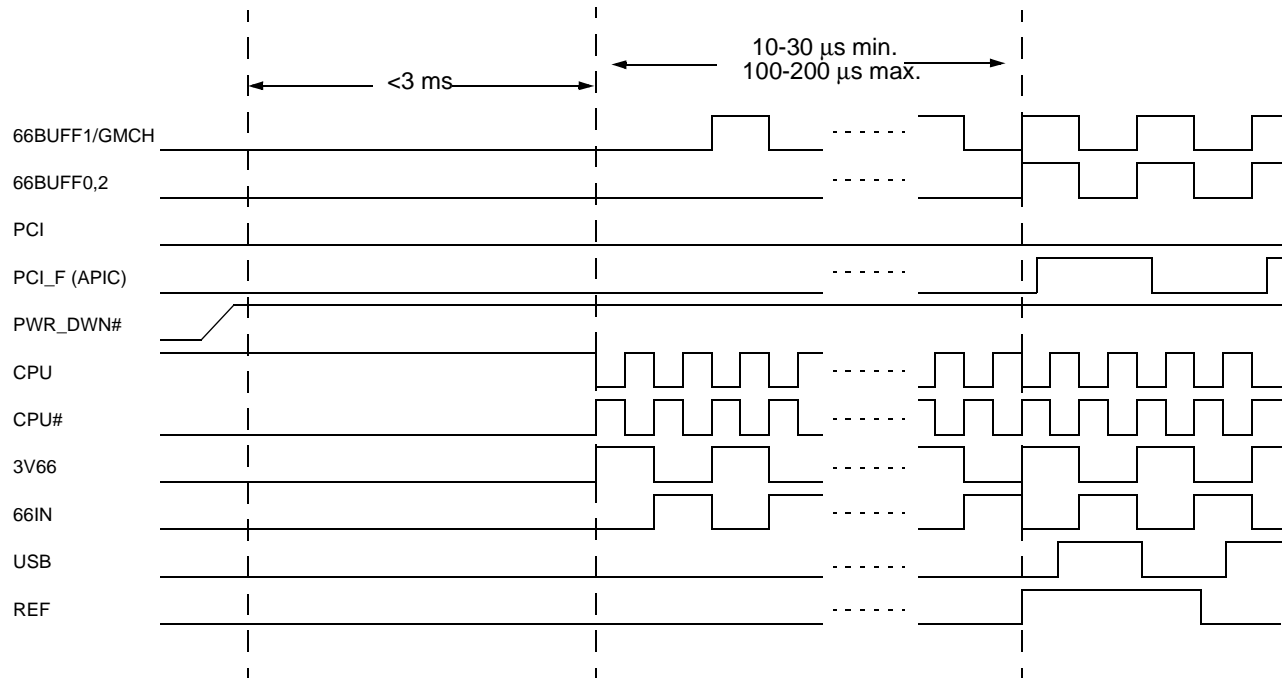
Note: PCI_STOP# asserted LOW

PWRGD# Timing Diagrams

Figure 2. CPU Power BEFORE Clock Power

Figure 3. CPU Power AFTER Clock Power

Layout Example

+3.3V Supply

FB

0.005 μF

μF

VDDQ3

C1

G G

1
2
3 G
4
5
6
7 G
8
9
10
G 11 V
12
13 G
14
G 15 V
16 G
17
18
19 G
20
21 G
Core
G 22 V
23 G
24 G

CY28322-2

*Option A

G
G 48 V G
47
G 46
45
44 V G
G 43
42
G 41
40 V G
39 G
38
37
36 G
35
34
33
32 G
31
30
29 G
28 V G
27 G
26
25 G

C5 G G C6

VDDQ3

8Ω *Option B

FB = Dale ILB1206–300 or 2TDKACB2012L–120 or 2 Murata BLM21B601S Ferrite bead
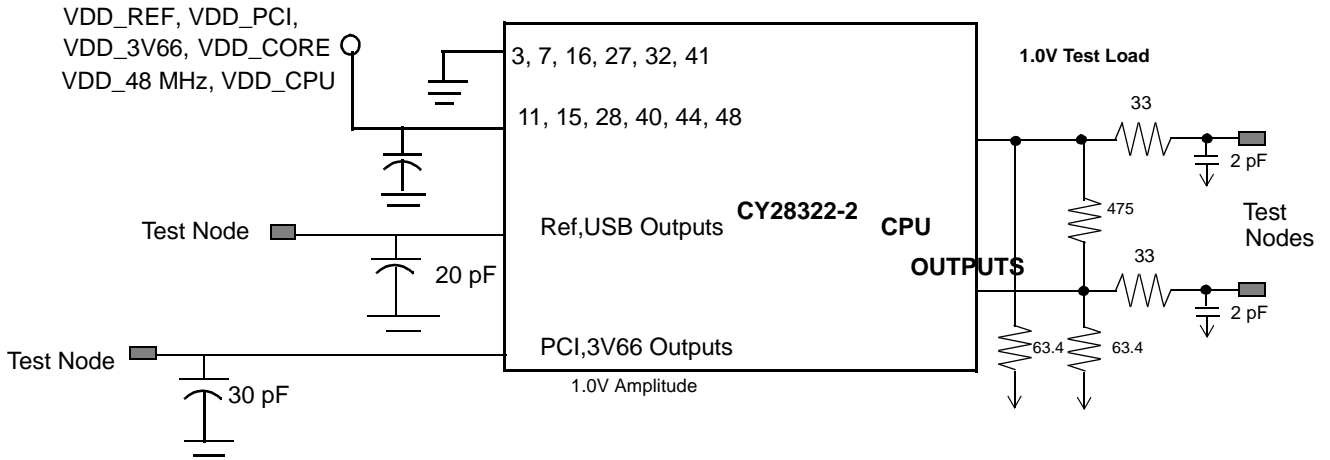
Ceramic Caps C1 = 10–22 μF   C2 = 0.005 μF C5 = 0.1 μF C6 = 10 μF

G = VIA to GND plane layer   V =VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors.

* If on board video uses 48-MHz or Dot clock add the Option B 8Ω series resistor
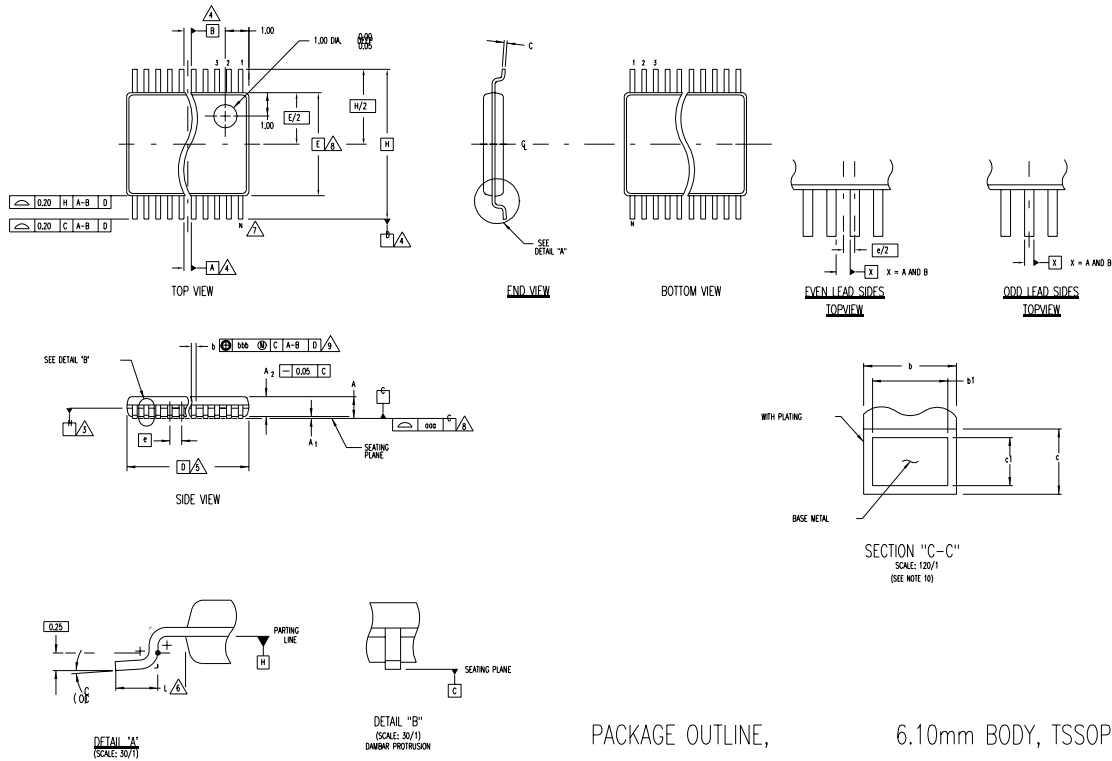**All Bypass cap's on VDD pin = 0.1 μF Low ESR**

Test Circuit

Ordering Information

Ordering Code	Package Type	Operating Range
CY28322ZC-2	48-pin TSSOP	Commercial

Package Diagram

48-pin Thin Shrink Small Outline Package

TOP VIEW

END VIEW

BOTTOM VIEW

EVEN LEAD SIDES TOPVIEW

ODD LEAD SIDES TOPVIEW

SIDE VIEW

SEE DETAIL 'B'

SEATING PLANE

SECTION "C-C"
SCALE: 120/1
(SEE NOTE 10)

WITH PLATING

BASE METAL

DETAIL 'A'
(SCALE: 30/1)

DETAIL "B"
(SCALE: 30/1)
DAMBAR PROTRUSION

PARTING LINE

SEATING PLANE

PACKAGE OUTLINE,   6.10mm BODY, TSSOP

THIS TABLE FOR 0.50MM PITCH

	COMMON DIMENSIONS			NOTE	VARI-ATIONS				
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	N
A			1.10		ED	12.40	12.50	12.60	48
A₁	0.05		0.15		EE	13.90	14.00	14.10	56
A₂	0.80	1.00	1.05		EF*	16.90	17.00	17.10	64
aaa		0.10							
b	0.17		0.27	9	*DESIGNED BUT NOT TOOLED				
b1	0.17	0.20	0.23						
bbb		0.08							
c	0.09		0.20						
c1	0.09	0.127	0.16						
D	SEE VARIATIONS			5					
E	6.00	6.10	6.20	5					
e		0.50 BSC							
H		8.10 BSC							
L	0.50	0.60	0.75	6					
N	SEE VARIATIONS								
θ°	0		8						

ALL DIMENSIONS IN MILLIMETERS

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (.011±0.0005 INCHES) DIE THICKNESS ALLOWABLE IS 0.279±0.0005 INCHES)
2. DIMENSIONING & TOLERANCES PER ASME. Y14.5M-1994.
3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND CONCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DATUMS A-B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
5. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15MM ON D AND 0.25MM ON E PER SIDE.
6. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
9. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.10MM FOR 0.65MM PITCH, 0.08MM FOR 0.50MM PITCH AND 0.07MM FOR 0.40MM PITCH PACKAGES. SEE DETAIL 'B' AND SECTION "C-C".
10. SECTION "C-C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
11. CONTROLLING DIMENSION: MILLIMETERS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153, VARIATIONS DB, DC, DE, ED, EE, AND FE.

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Document Number: 38-07145

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112664	03/01/02	IKA	New Data Sheet
*A	114703	04/29/02	INA	Corrections on some PIN numbers.
*B	122796	12/14/02	RBI	Add Power up Requirements to Operating Conditions Information