



# Fast, Complete 8-/10-Bit A/D Converters with Microprocessor Interface

## AD573/AD673

### 1.1 Scope.

This specification covers the detail requirements for complete 8-bit and 10-bit resolution A/D converters with full microprocessor interface.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD673SD/883B
-2	AD573SD/883B

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000; package outline: D-20.

### 1.3 Absolute Maximum Ratings. (T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>CC</sub> to Digital Common . . . . .	+7V
V <sub>EE</sub> to Digital Common . . . . .	-16.5V
Analog Common to Digital Common . . . . .	±1V
Analog Input to Analog Common . . . . .	±15V
Control Inputs . . . . .	0 to V <sub>CC</sub>
Digital Outputs (High Impedance State) . . . . .	0 to V <sub>CC</sub>
Power Dissipation . . . . .	800mW
Storage Temperature Range . . . . .	-65°C to +150°C
Lead Temperature Range (Soldering 10sec) . . . . .	300°C

### 1.5 Thermal Characteristics.

Thermal Resistance  $\theta_{JC} = 25^\circ\text{C}/\text{W}$   
 $\theta_{JA} = 85^\circ\text{C}/\text{W}$

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Table 1.

Test	Symbol	Device <sup>2</sup>	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition <sup>1</sup>	Units
Relative Accuracy	RA	-1	0.195	0.195	0.195		Unipolar and Bipolar Major Transitions ± 3 Codes	± % of FS max
		-2	0.098	0.195	0.098	0.098		
Differential Nonlinearity <sup>3</sup>	DNL	-1	8	8	8		All codes test Unipolar and Bipolar	Bits min
		-2	10	8	10	10		
Full-Scale Error <sup>4</sup>	A <sub>F</sub>	-1, 2	40	40			Unipolar	± mV max
		-1, 2	20	20			Bipolar	± mV max
Full-Scale Temperature Drift	TCA <sub>F</sub>	-1	0.781		0.781			± % of FS max
		-2	0.488		0.488			
Offset Error	V <sub>OS</sub>	-1	20	20			First Transition	± mV max
		-2	10	20		10		
Offset Temperature Drift	TCV <sub>OS</sub>	-1	0.391		0.391			± % of FS max
		-2	0.195		0.195			
Bipolar Zero Error	B <sub>PZE</sub>	-1	20	20			Low Side MSB Transition Bipolar	± mV max
		-2	10	20		10		
Bipolar Zero Temperature Drift	TCB <sub>PZE</sub>	-1	0.391		0.391		Low Side MSB Transition Bipolar	± % of FS max
		-2	0.195		0.195			
Input Resistance	R <sub>IN</sub>	-1, 2	3	3	3			kΩ min
			7	7	7			kΩ max
Conversion Time <sup>5</sup>	t <sub>C</sub>	-1, 2	10	10	10			μs min
			30	30	30			μs max
Three-State Leakage Current	I <sub>OLT</sub>	-1	40	40	40		V <sub>OH</sub> = 5.0V V <sub>OL</sub> = 0.0V, DB0-DB7	± μA max
		-2	40	40	40		V <sub>OH</sub> = 5.0V V <sub>OL</sub> = 0.0V, DB0-DB9	
Power Supply Rejection Ratio	PSRR	-1	78.1	78.1	78.1		V <sub>CC</sub> = 5V, -15.75V ≤ V <sub>EE</sub> ≤ -14.25V V <sub>CC</sub> = 5V, -12.6V ≤ V <sub>EE</sub> ≤ -11.4V	± mV max
		-2	19.5	78.1	78.1	19.5	V <sub>EE</sub> = -15V, 4.5V ≤ V <sub>CC</sub> ≤ 5.5V	
Power Supply Current	I <sub>CC</sub>	-1, 2	15	15			DR LOW	+ mA max
			15	15			DR HIGH (During Conversion)	
	I <sub>EE</sub>	-1, 2	15	15				- mA max
Digital Input High Voltage	V <sub>IH</sub>	-1, 2	2.0	2.0	2.0		Convert, HBE, LBE, DE	+ V min
Digital Input Low Voltage	V <sub>IL</sub>	-1, 2	0.8	0.8	0.8		Convert, HBE, LBE, DE	+ V max
Digital Input High Current	I <sub>IH</sub>	-1, 2	100	100	100		Convert, HBE, LBE, DE V <sub>IH</sub> = 5.0V	± μA max
Digital Input Low Current	I <sub>IL</sub>	-1, 2	100	100	100		Convert, HBE, LBE, DE V <sub>IL</sub> = 0.0V	± μA max
Digital Output Low Voltage	V <sub>OL</sub>	-1	0.4	0.4	0.4		I <sub>OL</sub> = +3.2mA, DR, DB0-DB7	+ V max
		-2	0.4	0.4	0.4		I <sub>OL</sub> = +3.2mA DR, DB0-DB9	
Digital Output High Voltage	V <sub>OH</sub>	-1	2.4	2.4	2.4		I <sub>OH</sub> = -0.5mA, DB0-DB7	+ V min
		-2	2.4	2.4	2.4		I <sub>OH</sub> = -0.5mA, DB0-DB9	

Test	Symbol	Device	Design Limit @ + 25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition <sup>1</sup>	Units
Convert Pulse Width <sup>5</sup>	$t_{CS}$	- 1, 2	500		500	500		ns min
DR Delay Convert <sup>5</sup>	$t_{DSC}$	- 1, 2	1.5			1.5		$\mu$ s max
Data Valid After $\overline{DE}$ , $\overline{HBE}$ or $\overline{LBE}$ High <sup>6</sup>	$t_{HD}$	- 1, 2	50					ns min
Output Float Delay <sup>6</sup>	$t_{HL}$	- 1, 2	200			200		ns max
Data Access Time <sup>6</sup>	$t_{DD}$	- 1, 2	250			250		ns max

**NOTES**

<sup>1</sup> $V_{CC} = +5V$ ,  $V_{BB} = -15V$ , analog input through 15 $\Omega$  resistor to Pin 13, Unipolar configuration.

$T_A = 25^\circ C$  unless otherwise indicated.

Unipolar configuration Pin 16 (Bipolar Offset Control) is grounded.

Bipolar configuration Pin 16 is not connected.

<sup>2</sup>For - 1 (8-Bit resolution Device), 0.391% of full scale = 1 LSB (least significant bit). For - 2 (10-Bit resolution device), 0.098% of full scale = 1 LSB.

<sup>3</sup>Minimum resolution for which no missing codes are guaranteed.

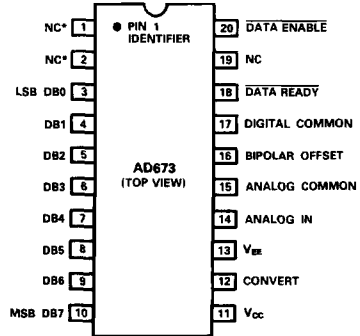
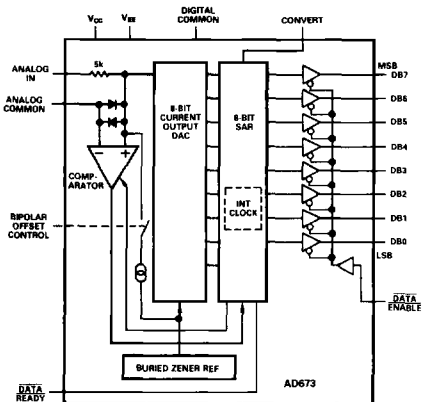
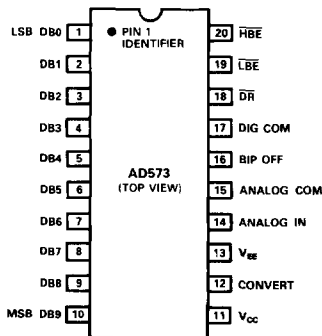
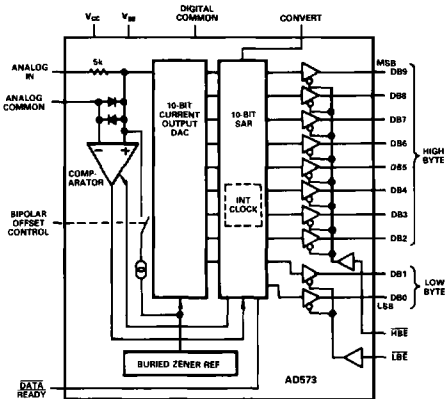
<sup>4</sup>- 1 device full scale error guaranteed trimmable with 500 $\Omega$  potentiometer.

- 2 device full scale error guaranteed trimmable with 200 $\Omega$  potentiometer.

<sup>5</sup>See Figure 1.

<sup>6</sup>See Figures 2 and 3.

### 3.2.1 Functional Block Diagram and Terminal Assignments.



\*PINS 1 & 2 ARE INTERNALLY CONNECTED TO TEST POINTS AND SHOULD BE LEFT FLOATING

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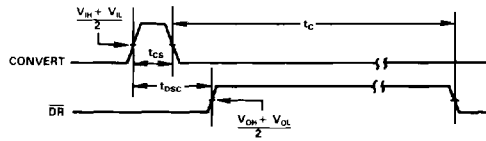


Figure 1. AD573 and AD673 CONVERT Timing

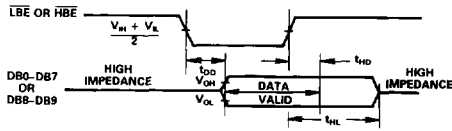


Figure 2. AD573 READ Timing

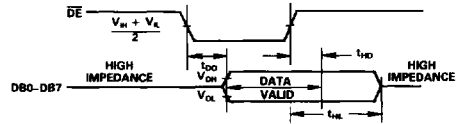


Figure 3. AD673 READ Timing

### 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

### 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

