January 1999 File Number 896.5

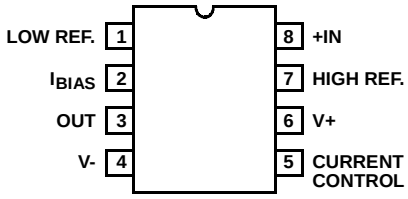
Programmable Schmitt Trigger with Memory, Dual Input Precision Level Detector

The CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high operating current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16V, or a dual power supply with maximum operating voltage of ±8V. It can directly control currents up to 150mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30mA. The CA3098 contains the following major circuit function features (see Block Diagram):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the “high” reference, and the other to compare the input with the “low” reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. Flip-flop: the flip-flop functions as a bistable “memory” element that changes state in response to each trigger command.
3. Driver and output stages: these stages permit the circuit to “sink” maximum peak load currents up to 150mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

Pinout

CA3098
(PDIP)
TOP VIEW



Features

- Programmable Operating Current
- Micropower Standby Dissipation
- Direct Control of Currents Up to 150mA
- Low Input On/Off Current of Less Than 1nA for Programmable Bias Current of 1µA
- Built-in Hysteresis . . . . . 20mV (Max)

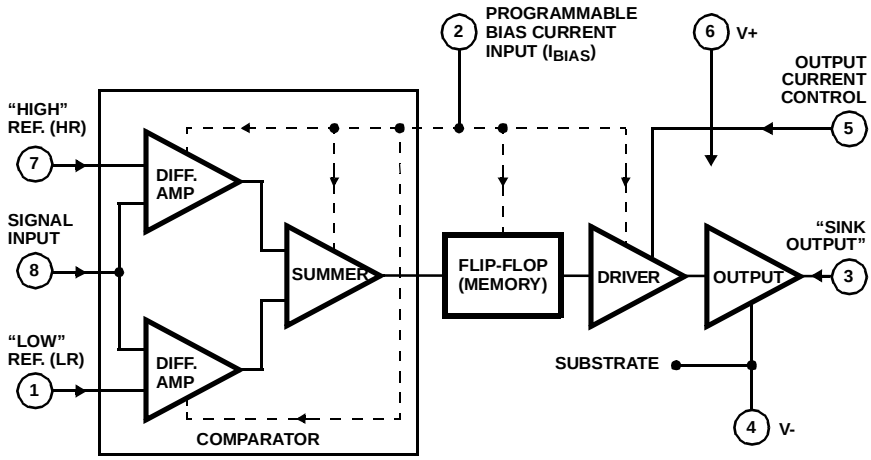
Applications

- Control of Relays, Heaters, LEDs, Lamps, Photosensitive Devices, Thyristors, Solenoids, etc.
- Signal Reconditioning
- Phase and Frequency Modulators
- On/Off Motor Switching
- Schmitt Triggers, Level Detectors
- Time Delays
- Overvoltage, Overcurrent, Overtemperature Protection
- Battery-Operated Equipment
- Square and Triangular-Wave Generators

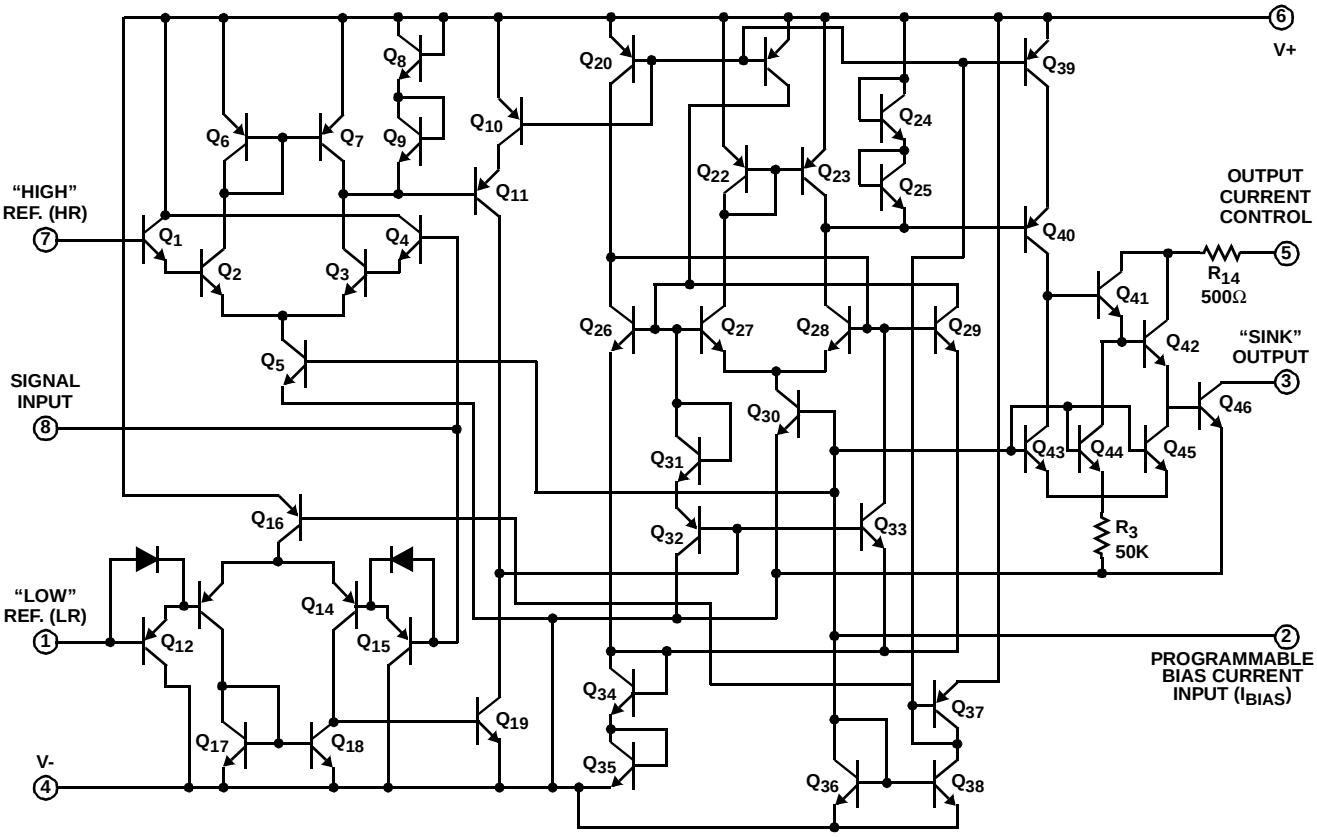
Part Number Information

PART NUMBER	TEMP RANGE (^{o}C)	PACKAGE	PKG. NO.
CA3098E	-55 to 125	8 Ld PDIP	E8.3

Block Diagram



Schematic Diagram



Absolute Maximum Ratings

Supply Voltage Between V+ and V- 16V
Voltage Between High Reference or Sink Output and V- 16V
Differential Input Voltage Between Terminals 8 and 1 . . . . . .10V
and Terminals 7 and 8
Load Current (Terminal 3) (Duty Cycle ≤25%) 150mA
Input Current to Voltage Regulator (Terminal 5) 25mA
Programmable Bias Current (Terminal 2) 1mA
Output Current Control (Terminal 5). 15mA

Operating Conditions

Temperature Range . . . . . -55°C to 125°C
Voltage Range
+IN . . . . . V- to V+
HIGH REF . . . . . (V- +2.0V) to V+
LOW REF . . . . . (V-) to (V+ -2.0V)

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA}
PDIP Package . . . . . 125°C/W
Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_A = 25°C$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA3098 MIN	CA3098 TYP	CA3098 MAX	UNITS
Input Offset Voltage						
"Low" Reference (Figures 2, 5)	$V_{IO(LR)}$	V_{LR} = GND, V_{HR} = V+ to (V- +2V), I_{BIAS} = 100µA	-15	-3	6	mV
"High Reference (Figures 2, 6)	$V_{IO(HR)}$	V_{HR} = GND, V_{LR} = V- to (V+ -2V), I_{BIAS} = 100µA	-10	-1	10	mV
Temperature Coefficient						
"Low" Reference (Figure 7)		-55°C to 125°C	-	4.5	-	µV/°C
"High" Reference (Figure 8)		-55°C to 125°C	-	±8.2	-	µV/°C
Minimum Hysteresis						
Voltage (Figure 9)	$V_{IO(HR-LR)}$	V_{REG} = 0V (Note 1), V+ = 4V, V- = -4V, I_{BIAS} = 1µA	-	3	20	mV
Temperature Coefficient (Figure 10)		-55°C to 125°C	-	6.7	-	µV/°C
Output Saturation Voltage (Figures 11, 12)	$V_{CE(SAT)}$	V_I = 5V, V_{REG} = 6V (Note 1), V+ = 12V, I_{BIAS} = 100µA	-	0.72	1.2	V
Total Supply Current	I_{TOTAL}					
"ON" (Figures 3, 13, 14)		V_I = 6V, V_{REG} > 6V (Note 1), V+ = 16V, I_{BIAS} = 100µA	500	710	800	µA
"OFF" (Figures 3, 13, 14)		V_I = 10V, V_{REG} < 10V (Note 1), V+ = 16V, I_{BIAS} = 100µA	400	560	750	µA
Input Bias Current (Figures 3, 15)	I_{IB}					
$I_{B(PNP)}$		V_I = 16V, V_{REG} < 16V (Note 1), V+ = 16V, I_{BIAS} = 100µA	-	42	100	nA
$I_{B(NPN)}$		V_I = 6V, V_{REG} > 6V (Note 1), V+ = 16V, I_{BIAS} = 100µA	-	28	100	nA
Output Leakage Current	$I_{CE(OFF)}$	Current from Terminal 3 when Q_{46} is "OFF"	-	-	10	µA
Switching Times (Figures 4, 16-27)		I_{BIAS} = 100µA, V+ = 5V, V_{REG} = 2.5V (Note 1)				
Delay Time	t_D		-	900	-	ns
Fall Time	t_F		-	30	-	ns
Rise Time	t_R		-	2000	-	ns
Storage Time	t_S		-	6.5	-	µs
Output Current (Note 2)	I_O		100	-	-	mA

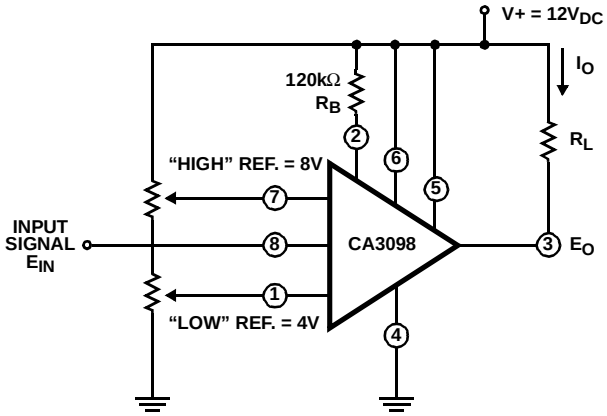
NOTES:
1. For definition of V_{REG} see Figure 3.
2. Continuous (DC) output current must be limited to ≤40mA. For 100mA output current, the duty cycle must be ≤40%.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

General Description of Circuit Operation

When the signal input voltage of the CA3098 is equal to or less than the “low” reference voltage (LR), current flows from an external power supply through a load connected to Terminal 3 (“sink” output). This condition is maintained until the signal input voltage rises to or exceeds the “high” reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the “low” reference voltage.

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{BIAS}) supplied to Terminal 2.

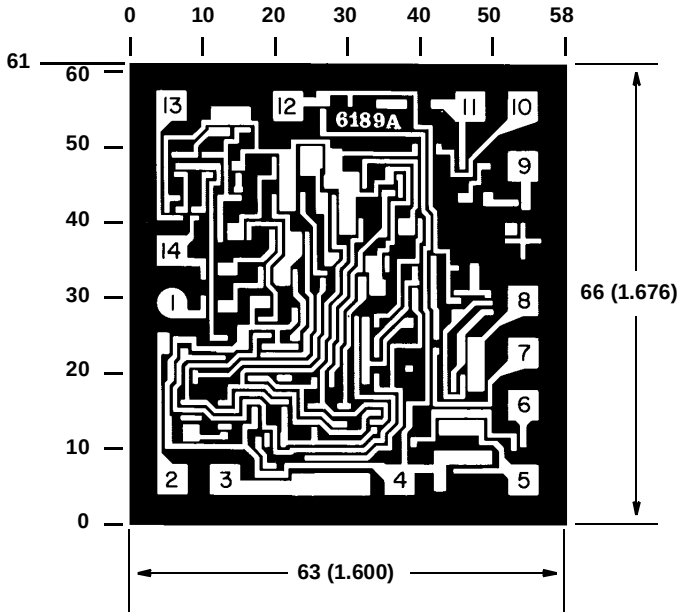
An auxiliary means of controlling the magnitude of load current flow at Terminal 3 is provided by “sinking” current into Terminal 5. Figure 1 highlights the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).



SEQUENCE	INPUT SIGNAL LEVEL	OUTPUT VOLTAGE (V) (TERMINAL 3)
1	$4 \geq E_{IN} > 0$	0
2	$8 \geq E_{IN} > 4$	0
3	$E_{IN} > 8$	12
2	$8 \geq E_{IN} > 4$	12
1	$4 \geq E_{IN} > 0$	0

FIGURE 1. BASIC HYSTERESIS SWITCH (SCHMITT TRIGGER) AND RESULTANT OUTPUT STATES

Metallization Mask Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7mils (0.17mm) larger in both dimensions.

Test Circuits

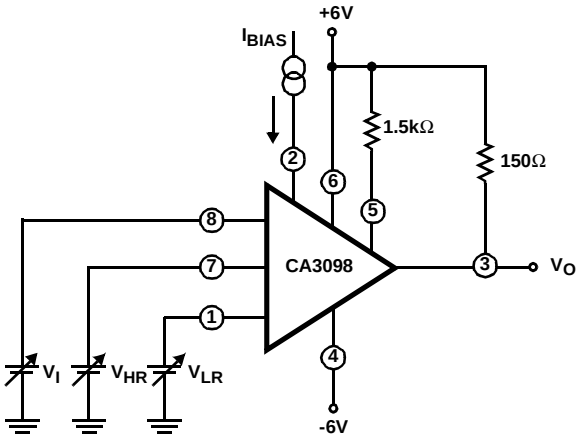


FIGURE 2. INPUT OFFSET VOLTAGE TEST CIRCUIT

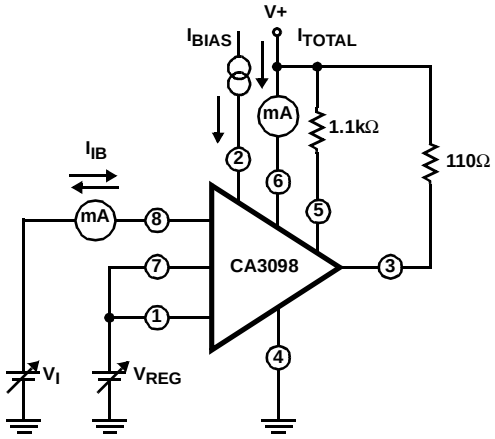
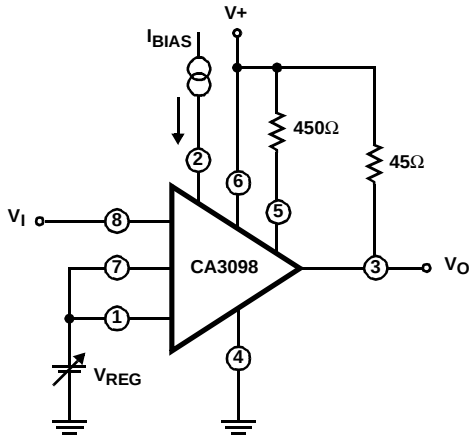


FIGURE 3. TOTAL SUPPLY CURRENT, AND INPUT BIAS CURRENT TEST CIRCUIT



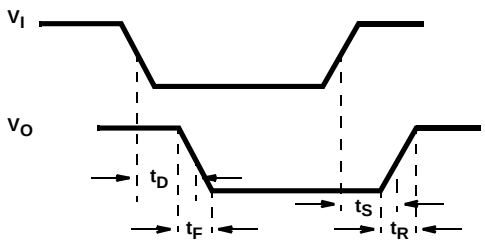


FIGURE 4. SWITCHING TIME TEST CIRCUIT

Typical Performance Curves

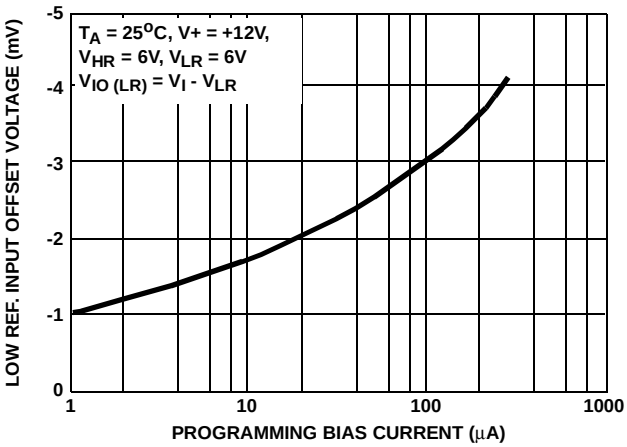


FIGURE 5. INPUT OFFSET VOLTAGE ("LOW" REFERENCE) vs PROGRAMMING BIAS CURRENT

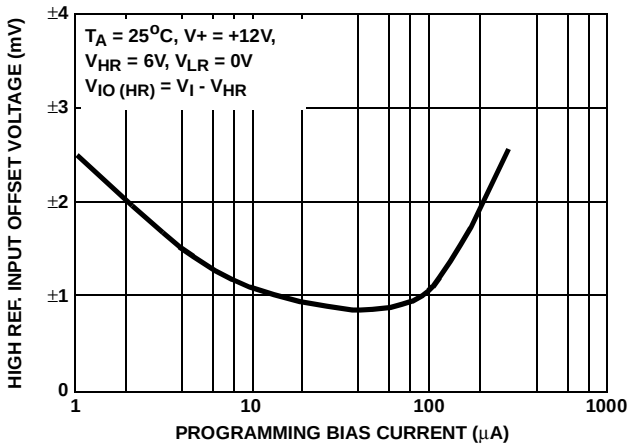


FIGURE 6. INPUT OFFSET VOLTAGE ("HIGH" REFERENCE) vs PROGRAMMING BIAS CURRENT

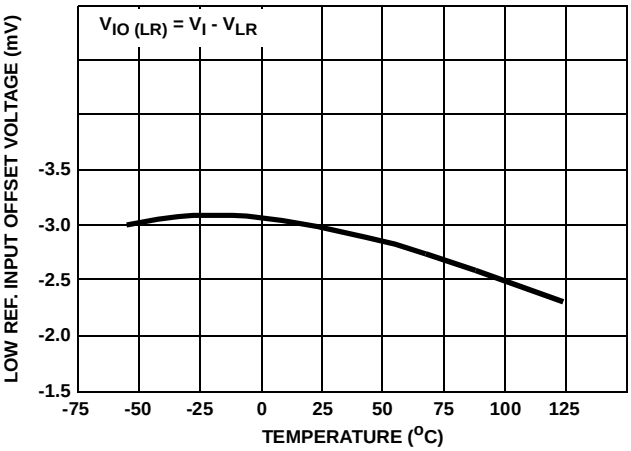


FIGURE 7. INPUT OFFSET VOLTAGE ("LOW" REFERENCE) vs AMBIENT TEMPERATURE

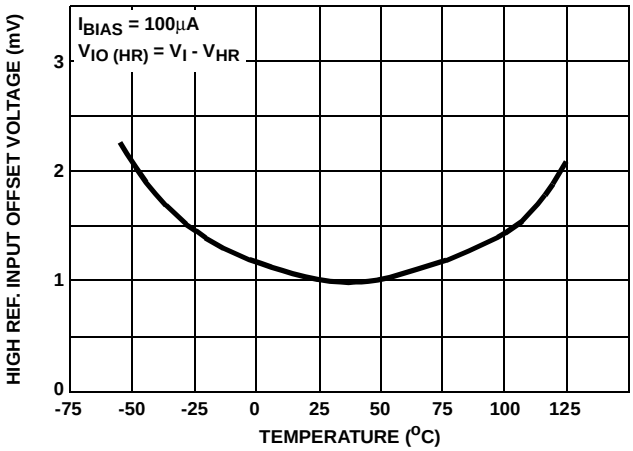


FIGURE 8. INPUT OFFFSET VOLTAGE ("HIGH" REFERENCE) vs AMBIENT TEMPERATURE

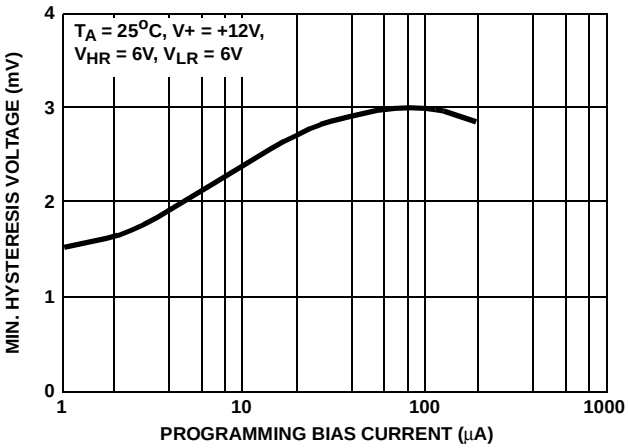


FIGURE 9. MINIMUM HYSTERESIS VOLTAGE vs PROGRAMMING BIAS CURRENT

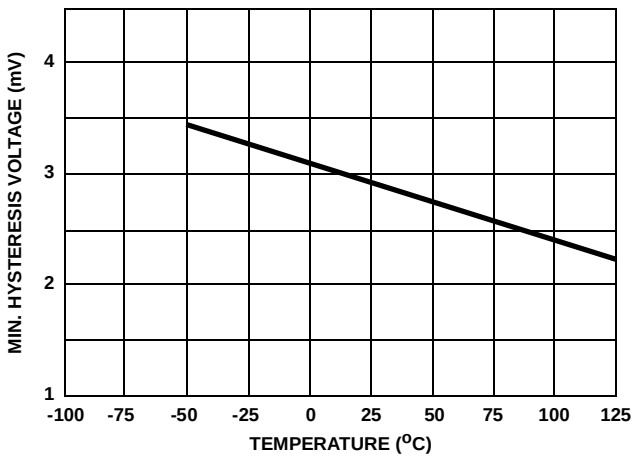


FIGURE 10. MINIMUM HYSTERESIS VOLTAGE vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

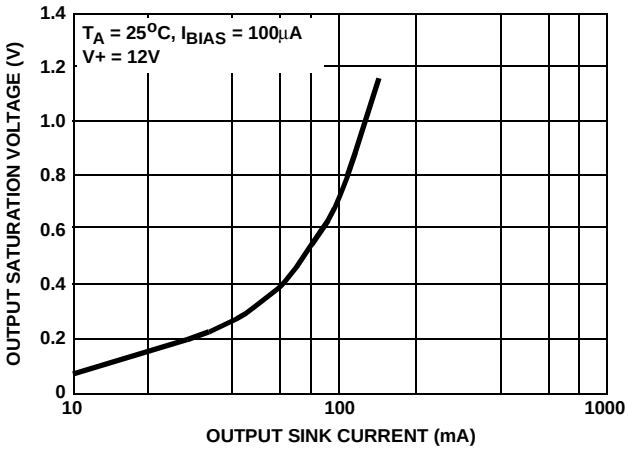


FIGURE 11. OUTPUT SATURATION VOLTAGE vs OUTPUT SINK CURRENT

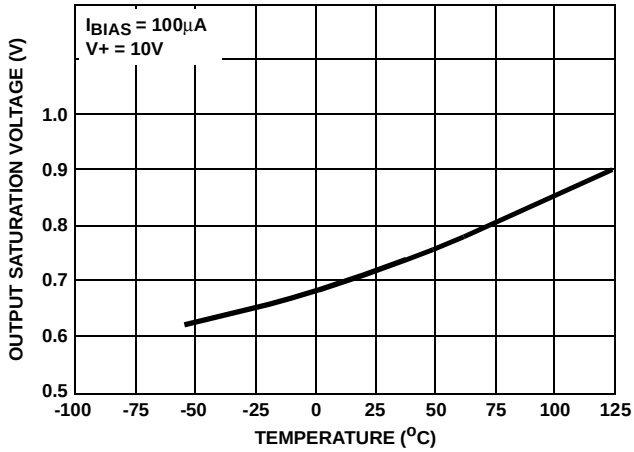
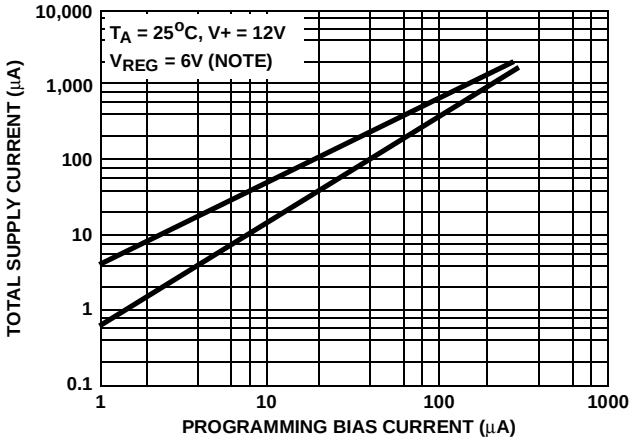


FIGURE 12. OUTPUT SATURATION VOLTAGE vs AMBIENT TEMPERATURE



NOTE: See Figure 3 for definition of V_{REG}

FIGURE 13. TOTAL SUPPLY CURRENT vs PROGRAMMING BIAS CURRENT

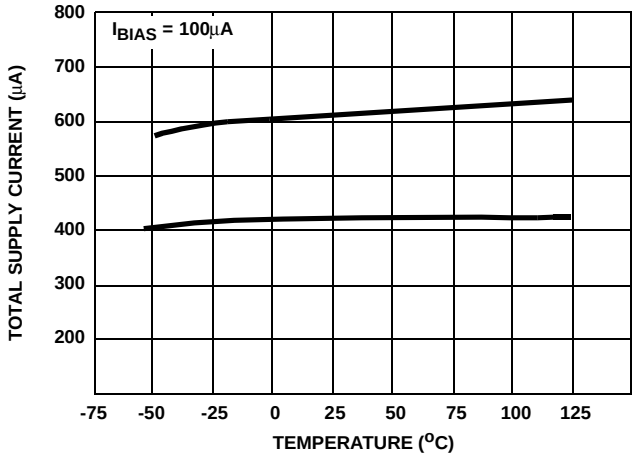
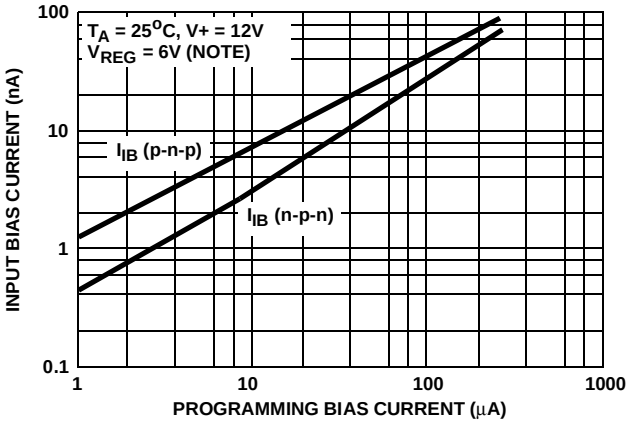


FIGURE 14. TOTAL SUPPLY CURRENT vs AMBIENT TEMPERATURE



NOTE: See Figure 3 for definition of V_{REG}

FIGURE 15. INPUT BIAS CURRENT vs PROGRAMMING BIAS CURRENT

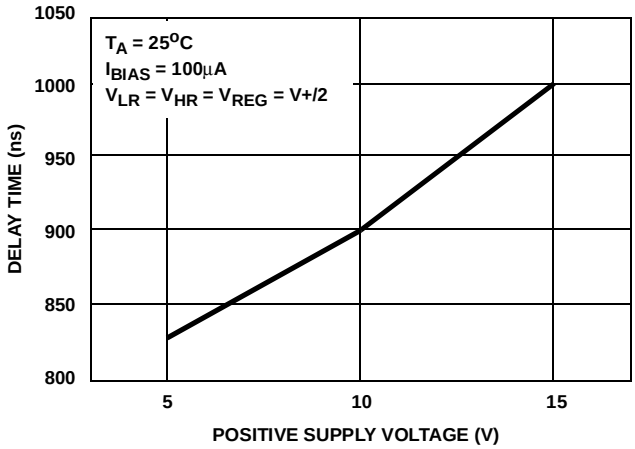


FIGURE 16. DELAY TIME vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

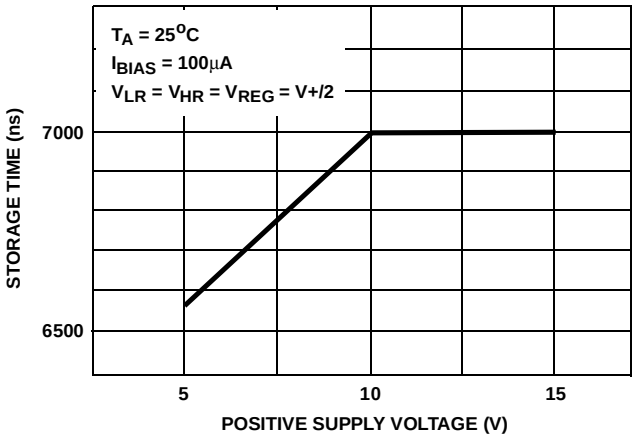


FIGURE 17. STORAGE TIME vs SUPPLY VOLTAGE

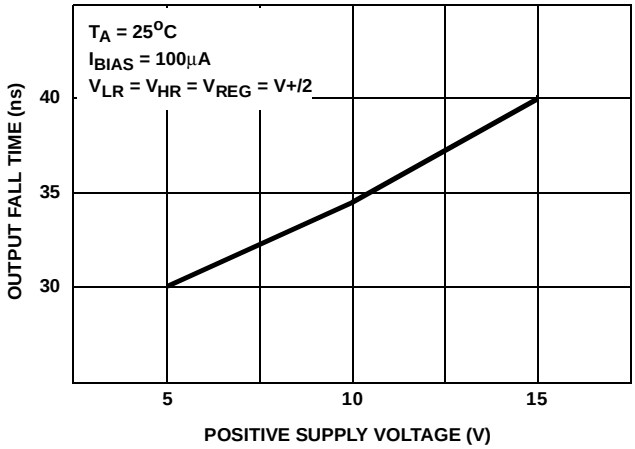


FIGURE 18. OUTPUT FALL TIME vs SUPPLY VOLTAGE

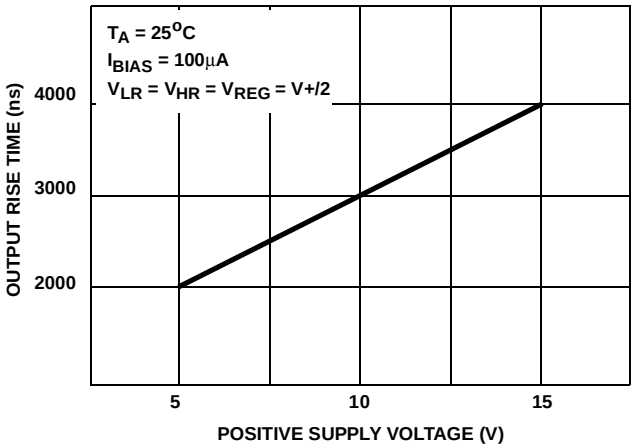


FIGURE 19. OUTPUT RISE TIME vs SUPPLY VOLTAGE

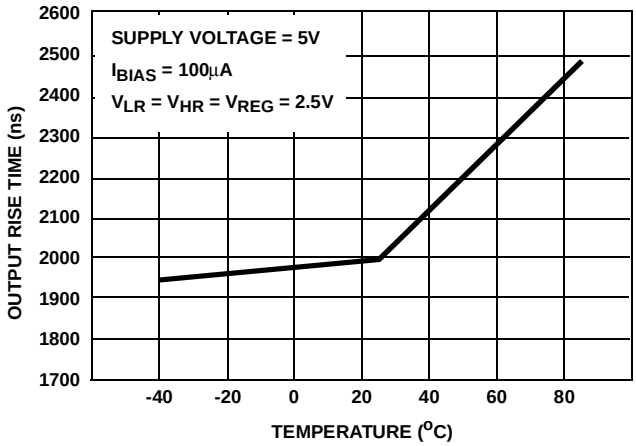


FIGURE 20. OUTPUT RISE TIME vs AMBIENT TEMPERATURE

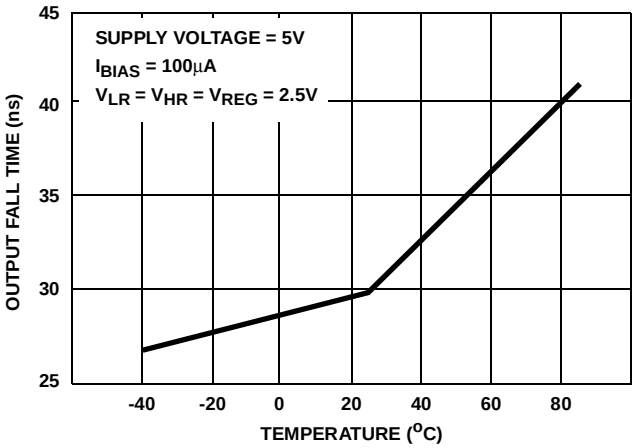


FIGURE 21. OUTPUT FALL TIME vs AMBIENT TEMPERATURE

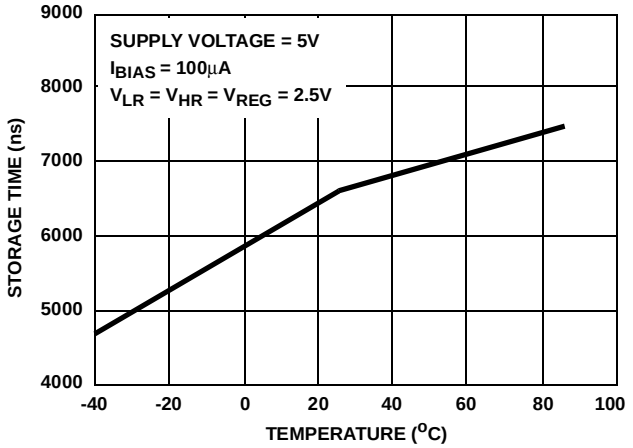


FIGURE 22. STORAGE TIME vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

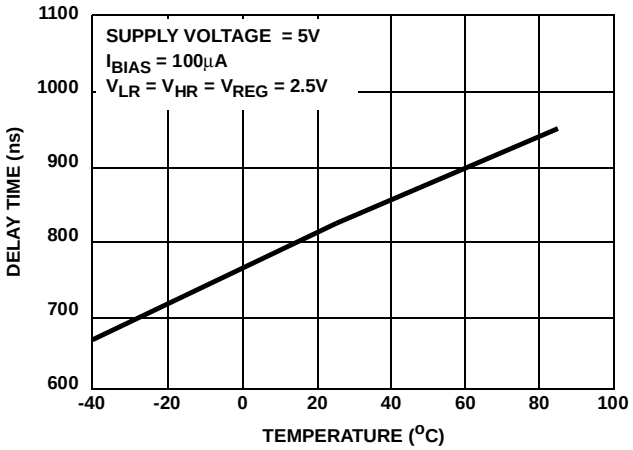


FIGURE 23. DELAY TIME vs AMBIENT TEMPERATURE

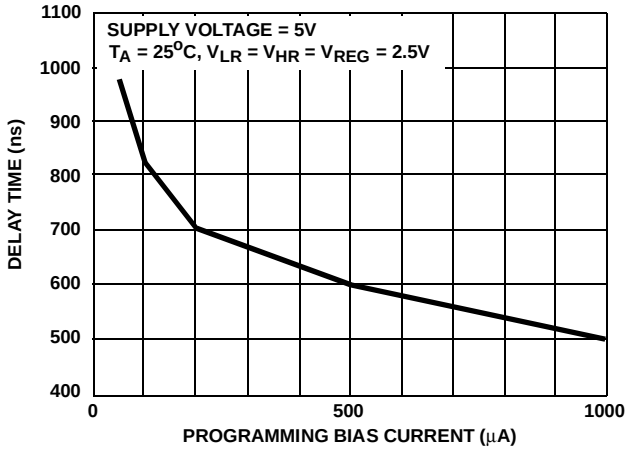


FIGURE 24. DELAY TIME vs PROGRAMMING BIAS CURRENT

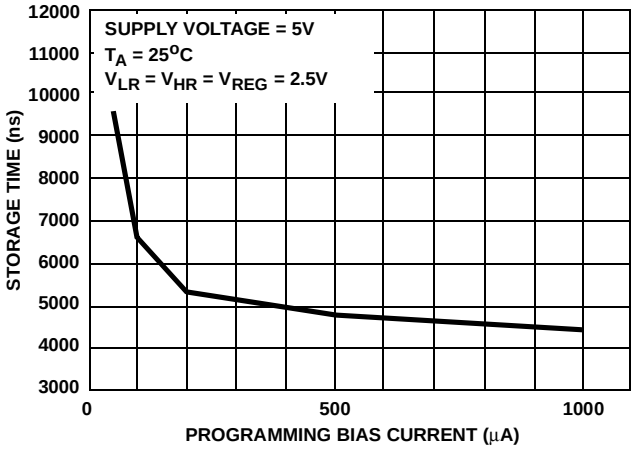


FIGURE 25. STORAGE TIME vs PROGRAMMING BIAS CURRENT

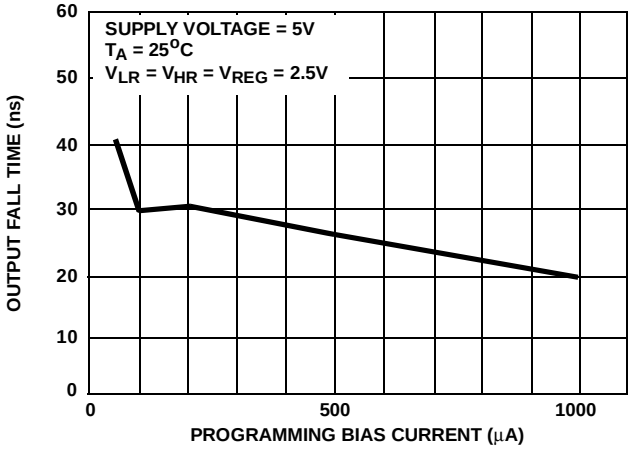


FIGURE 26. OUTPUT FALL TIME vs PROGRAMMING BIAS CURRENT

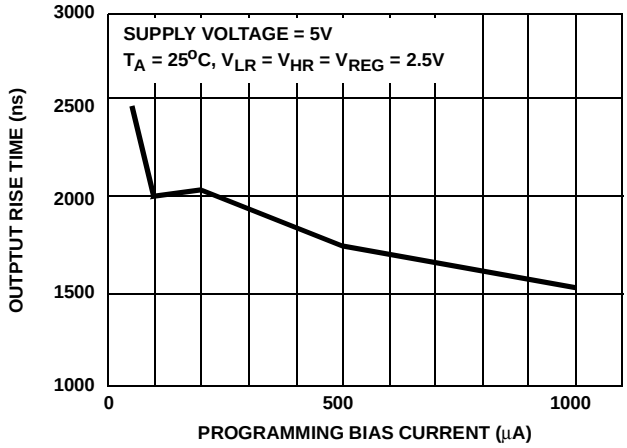


FIGURE 27. OUTPUT RISE TIME vs PROGRAMMING BIAS CURRENT

Typical Applications

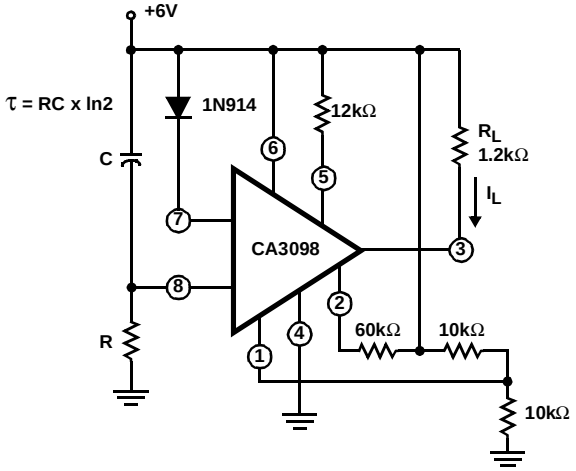


FIGURE 28. TIME DELAY CIRCUIT: TERMINAL 3 "SINKS" AFTER τ SECONDS

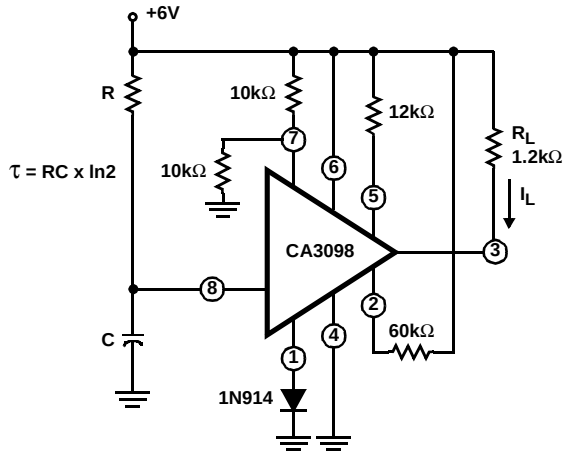


FIGURE 29. TIME DELAY CIRCUIT: "SINK" CURRENT INTERRUPTED AFTER τ SECONDS

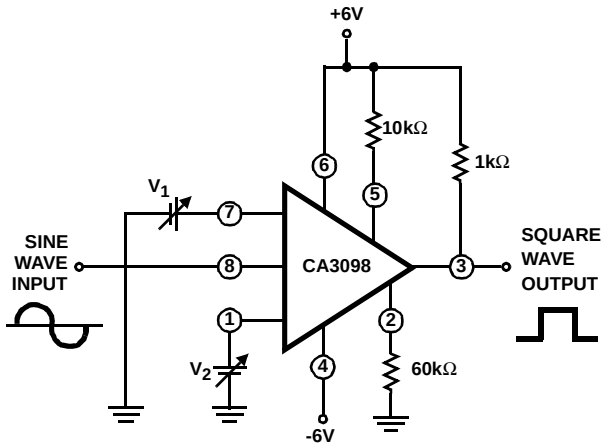


FIGURE 30. SINE WAVE TO SQUARE WAVE CONVERTER WITH DUTY CYCLE ADJUSTMENT (V_1 AND V_2)

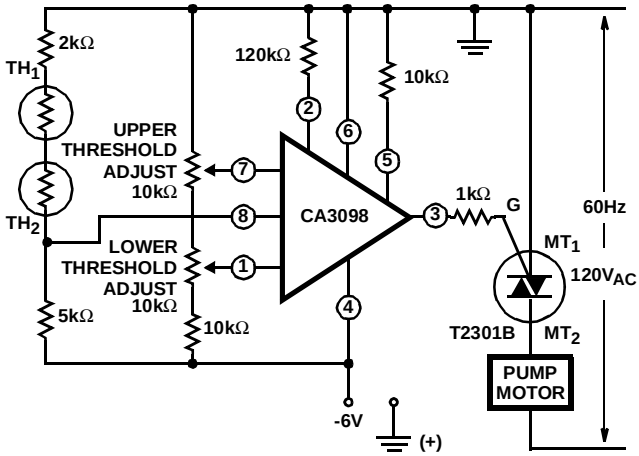
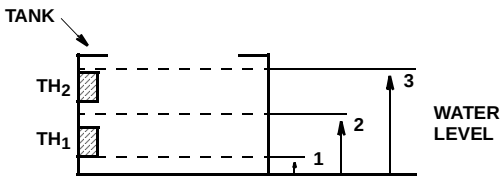


FIGURE 31A. WATER LEVEL CONTROL CIRCUIT



NOTES:

1. Motor pump is "ON" when water level rises above thermistor TH_2.
2. Motor pump remains "ON" until water level falls below thermistor TH_1.
3. Thermistors, operate in self heating mode.

FIGURE 31B. WATER LEVEL DIAGRAM FOR CIRCUIT

FIGURE 31. WATER LEVEL CONTROL APPLICATION

Typical Applications (Continued)

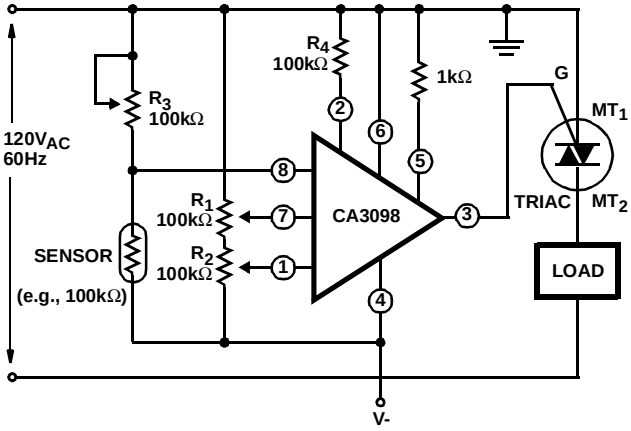
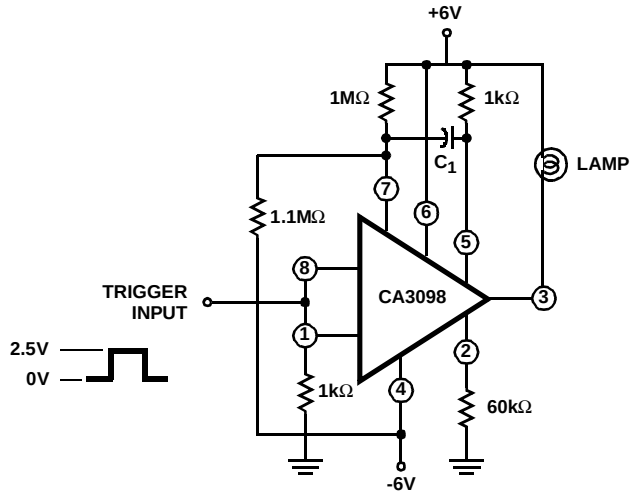


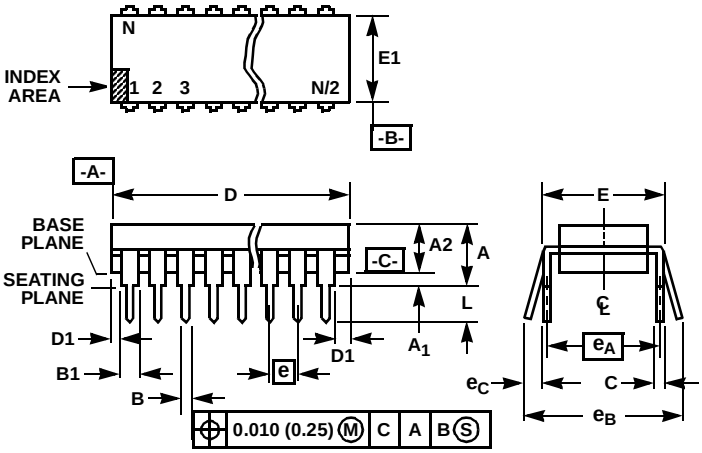
FIGURE 32. OFF/ON CONTROL OF TRIAC WITH PROGRAMMABLE HYSTERESIS



DESIRED t_{ON} (ms)	VALUE OF C_1 (μF)
15	0.01
150	0.1
300	0.2

FIGURE 33. ONE SHOT MULTIVIBRATOR

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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